Dual Channel Isolated Gate-Driver ICs

Hynetek Semiconductor Co., Ltd.

HP3600

FEATURES

Common-mode transient immunity (CMTI) greater than 150 kV/μs
Fast input-to-output propagation (48 ns)
4-A peak source, 6-A peak sink output
Up to 33-V VDD output drive supply
3-V VDD UVLO
-5V handling capability on input stage
Fast clamping of the output under UVLO conditions
Programmable overlap and dead time
Fast disable for power sequencing
SOP-16 package
Operating junction temperature range of –40 °C to 150 °C

APPLICATIONS

Telecom PSU
Data center
Outdoor PSU
OBC
EV charging
Industry automation
Home appliance

GENERAL DESCRIPTION

The HP3600 isolated driver is an isolated dual channel gate driver can be configured as high-side/low-side drivers. The peak source output current is 4.0A and the peak sink output current is 6.0A. Programmable dead time (DT) feature is available. Pulling high the DIS pin shuts down both outputs simultaneously and allows for normal operation when the DIS pin is open or pulled low. As a fail-safe measure, primary-side logic failures force both outputs low.

The VDDA and VDDB supply voltage are up to 33 V. A wide input VDDI range from 3 V to 18 V makes the driver suitable for interfacing with both analog and digital controllers. All the supply voltage pins have under voltage lock-out (UVLO) protection.

The HP3600 has 3.0kVRMS isolation for 1 minute per UL 1577 in SOP-16 package.

High CMTI, low propagation delay makes the HP3600 is suitable for a wide range of isolated MOSFET and SiC or GaN FET gate drive applications.

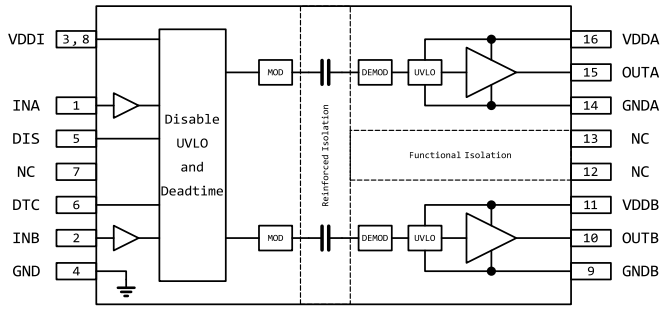

Figure 1 Functional Block Diagram

TYPICAL APPLICATION CIRCUIT

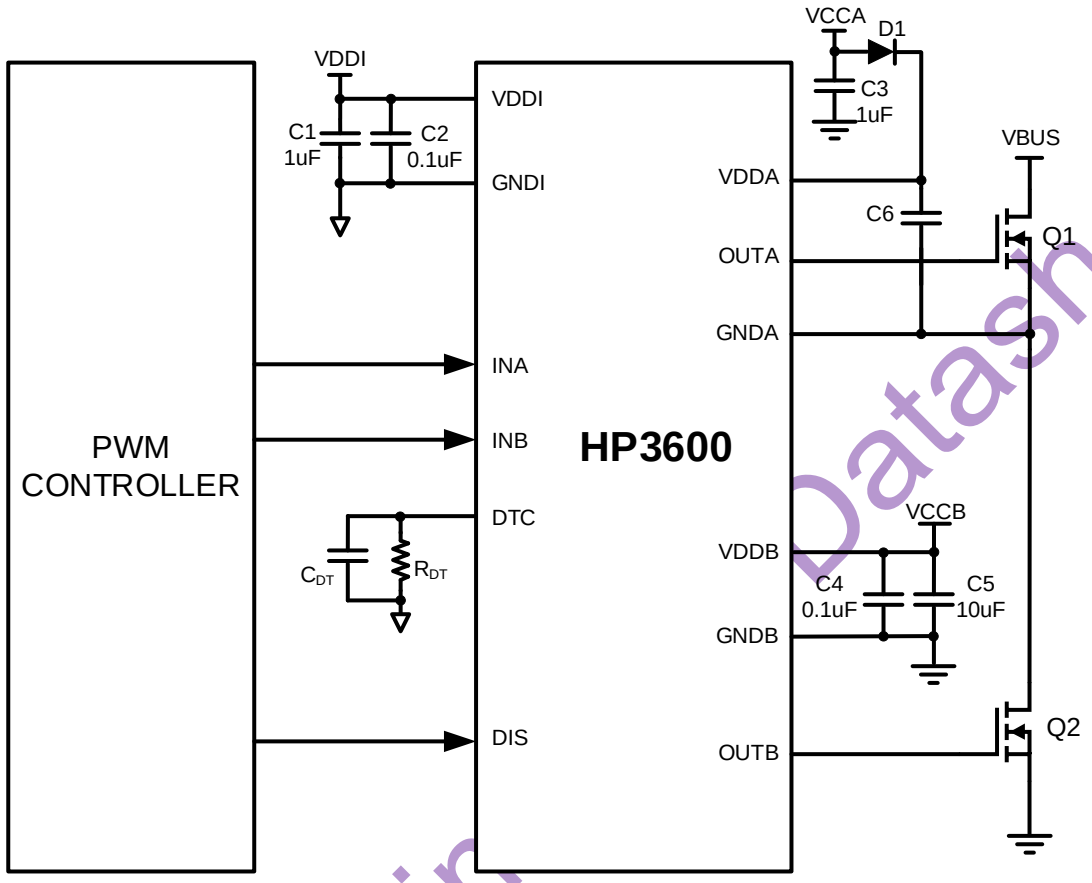

Figure 2. Typical Application Circuit

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REVISION HISTORY

Version	Date	Descriptions
Rev. 0.1	2023/11	Initial version

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

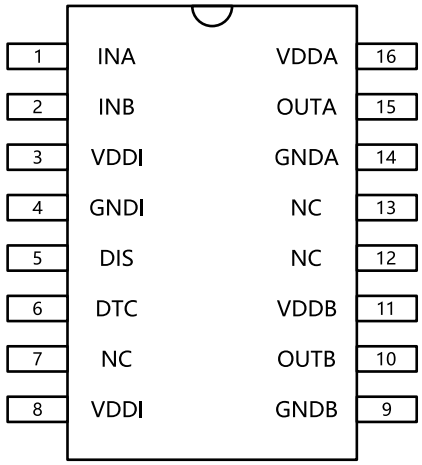


Figure 3 16-Pin SOP-16 Configuration

Table 0-1. Pin Function Descriptions for SOP-16

No.	Pin	Type	Primary Function
1	INA	I	Input signal for A channel. INA input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
2	INB	I	Input signal for B channel. INB input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
3	VDDI	P	Primary-side supply voltage. Locally decoupled to GND using a low ESR/ESL capacitor located as close to the device as possible.
4	GNDI	P	Primary-side ground reference. All signals in the primary side are referenced to this ground.
5	DIS	I	Disables both driver outputs if asserted high, enables if set low or left open. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity. Bypass using a 1 nF low ESR/ESL capacitor close to DIS pin when connecting to a micro controller with distance.
6	DTC	I	Dead time programming input. Connect a resistor between DTC and GNDI to program the dead time. A bypassing capacitor, 2.2nF or greater, is recommended to be put between DTC and GNDI to achieve better noise immunity.
7	NC	-	No Internal connection.
8	VDDI	P	Primary-side supply voltage. This pin is internally shorted to pin 3.
9	GNDB	P	Ground for secondary-side driver B. Ground reference for secondary side B channel.
10	OUTB	O	Output of driver B. Connect to the gate of the B channel FET.
11	VDDB	P	Secondary-side power for driver B. Locally decoupled to VSSB using low ESR/ESL capacitor located as close to the device as possible.
12	NC	-	No Internal connection.
13	NC	-	No Internal connection.

No.	Pin	Type	Primary Function
14	GNDA	P	Ground for secondary-side driver A. Ground reference for secondary side A channel.
15	OUTA	O	Output of driver A. Connect to the gate of the A channel FET.
16	VDDA	P	Secondary-side power for driver A. Locally decoupled to VSSA using a low ESR/ESL capacitor located as close to the device as possible.

SPECIFICATIONS

V_{DDI} = 5 V, 0.1μF capacitor from VDDI to GNDI, V_{DDA} = V_{DDB} =15V, 1μF capacitor from VDDA and VDDB to GNDA and GNDB, T_A = –40°C to +125°C, unless otherwise specified.

Table 0-1. Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
Input supply voltage	V_{DDI}		3		18	V
Input supply quiescent current	I_{DDI}	V_{INA} = 0 V, V_{INB} = 0 V	1.5	2.0	2.5	mA
Input supply operating current	I_{DDI}	F_{sw} = 50 kHz, current per channel, C_{OUT} = 100 pF	1.9	2.0	3.1	mA
Output supply voltage	V_{DDA}/V_{DDB}		3.5		30	V
Output supply quiescent current	I_{VDDA}/I_{VVDB}	V_{INA} = 0 V, V_{INB} = 0 V	0.8	1.3	2	mA
Output supply operating current	I_{VDDA}/I_{VVDB}	F_{sw} = 50 kHz, current per channel, C_{OUT} = 100 pF	1.2	1.7	2.3	mA
VDDA/VDDB UNDER VOLTAGE LOCKOUT (UVLO)						
UVLO turn-on threshold	V_{UVLO_ON}		3.2	3.5	3.8	V
UVLO turn-off threshold	V_{UVLO_OFF}		2.7	3.0	3.3	V
UVLO threshold hysteresis	V_{UVLO_HYST}			0.5		V
VDDI UNDER VOLTAGE LOCKOUT (UVLO)						
UVLO turn-on threshold	V_{DDI_ON}		2.5	2.7	2.9	V
UVLO turn-off threshold	V_{DDI_OFF}		2.3	2.5	2.7	V
UVLO threshold hysteresis	V_{DDI_HYST}			0.2		V
INPUT (INA, INB)						
Input voltage threshold for transition Low to High	V_{INH}		-	1.7	2.1	V
Input voltage threshold for transition High to Low	V_{INL}		0.8	1.1	-	V
Input voltage threshold hysteresis	V_{IN_HYST}		0.4	0.8	1.2	V
Pull down Resistance on VIA,VIB,DIS and PWM	R_{PD}		100	170	280	kΩ
DEAD-TIME						
Dead time	t_{DT}	R_{DTC} = 20 kΩ	160	200	240	ns
OUTPUTS (OUTA, OUTB)						
Peak sourcing output current	I_{SRC_PK}	C_{VDD} = 10 μF, C_{LOAD} = 0.18 μF, F_{sw} = 1 kHz, bench measurement		4.0		A
Peak sinking output current	I_{SNK_PK}	C_{VDD} = 10 μF, C_{LOAD} = 0.18 μF, F_{sw} = 1 kHz, bench measurement		-6.0		A
Output voltage at high state	V_{OHA_ERR}/ V_{OHB_ERR}	V_{VDDA}, V_{VDDB} = 12 V, I_{OUT} = –10 mA, T_A = 25°C		13	24	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output voltage at low state	V_{OLA}/V_{OLB}	V_{VDDA}, V_{VDDB} = 12 V, I_{OUT} = 10 mA, T_A = 25°C		7	14	mV
Switching Characteristics						
Output rise time, 10% to 90% measured points	t_{RISE}	C_{OUT} = 1.0 nF, F_{sw}= 1 kHz, 50% duty cycle		6	15	ns
Output fall time, 90% to 10% measured points	t_{FALL}			4	10	ns
Minimum pulse width	t_{PWmin}	Output off for less than minimum, C_{OUT} = 0 pF			15	ns
INx/DIS to OUTx turn-on / off propagation delay	t_{PD_ON} t_{PD_OFF}			48	68	ns
Pulse width distortion $\lvert t_{PD\_ON} - t_{PD\_OFF} \rvert$	t_{PWD}				20	ns
Propagation delays matching between V_{OUTA}, V_{OUTB}	t_{DM}	F_{sw} = 100 kHz			18	ns
VDDI UVLO Recovery Delay	$t_{UVLO\_REC\_VDDI}$			15	100	µs
VDDA, VDDB UVLO Recovery Delay	$t_{UVLO\_REC\_VDDA/B}$			20	30	µs
High Level Static Common Mode Transient Immunity	$CMTI_H$	V_{CM}=1000V, T_A=25°C	150	200		kV/µs
Low Level Static Common Mode Transient Immunity	$CMTI_L$	V_{CM}=1000V, T_A=25°C	150	200		kV/µs

Table 0-2 SAFETY RELATED CERTIFICATIONS (SOP16)

VDE	UL	CQC	TUV
DIN VDE 0884-17: 2021-10	UL 1577 component recognition program	Certified according to GB4943.1-2022	Certified according to IEC 61010-1: 2010+A1 and IEC 62368-1: 2018
Reinforced Insulation	Single protection, 3000 V_{RMS}	Reinforced insulation, Altitude≤ 5000m, Tropical climate	3000Vrms basic insulation, 400Vrms maximum working voltage
Certification Pending	Certification Pending	Certification Pending	Certification Pending

ABSOLUTE MAXIMUM RATINGS

Table 0-1.

Parameter	Rating
Output supply voltage	
VDDA, VDDB, continuous	-0.3 to 35 V
Output voltage	
OUTA to GNDA, OUTB to GNDB, continuous	-0.3 V to V_{DDx} + 0.3 V
OUTA, OUTB, transient for 200 ns	-3 V to V_{DDx} + 1.5 V
Input supply voltage	
VDDI to GND	-0.3 to 20 V
Input voltage	
INA, INB, DIS, DTC	-7 to V_{DDI} + 0.3 V
Output Channel to Channel internal isolation	1500 V
Junction temperature range	–40 °C to +150 °C
Storage Temperature	-65 °C to 150 °C
Soldering conditions	JEDEC J-STD-020
Electrostatic Discharge (ESD)	
Human body model	3000 V
Changed device model	2000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 0-2. Thermal Resistance

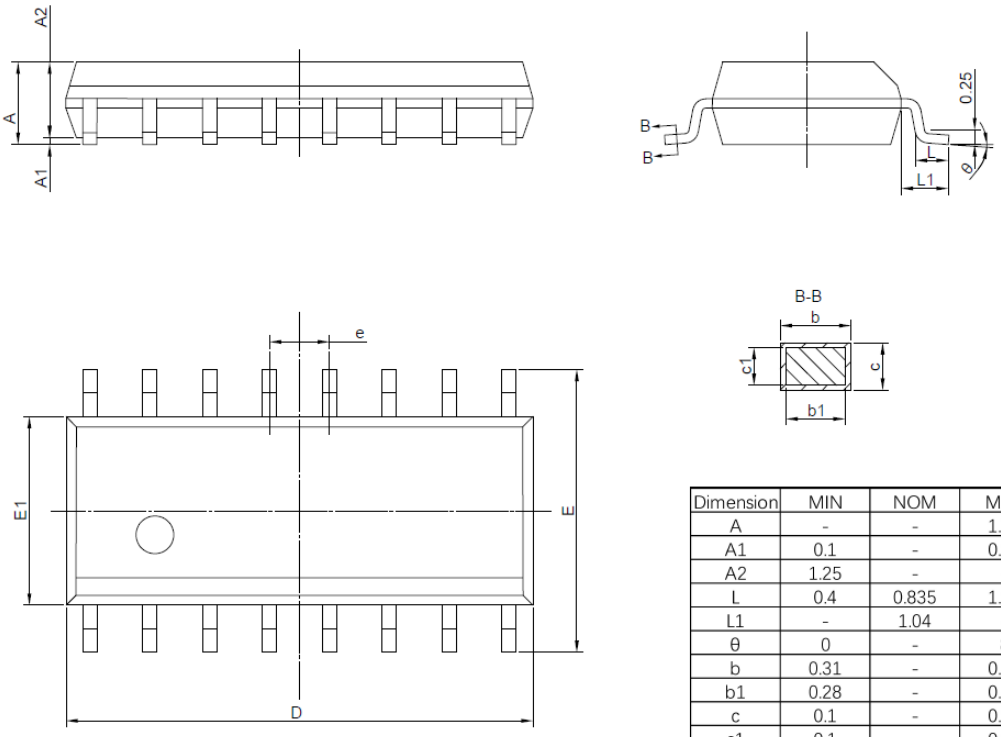
Package Type	θ_{JA}	θ_{JC}	Unit
SOP-16	150	38	°C/W

ESD CAUTION

Electrostatic Discharge Sensitive Device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE OUTLINE DIMENSIONS



Dimension	MIN	NOM	MAX
A	-	-	1.75
A1	0.1	-	0.25
A2	1.25	-	-
L	0.4	0.835	1.27
L1	-	1.04	-
θ	0	-	8
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.1	-	0.25
c1	0.1	-	0.25
D	9.8	9.9	10
E	5.8	6	6.2
E1	3.8	3.9	4
e	1.02	1.27	1.52
Unit : mm			

Figure 4. SOP-16 Package Outline Dimensions

ORDERING GUIDE

Device ID	Package Type	Tj Temp (℃)	Package Option	Package Qty
HP3600-AB001-SP16R	SOP-16	-40 ~ 150	T&R	3000ea

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