High Efficiency, 16V/12A Synchronous Step Down Regulator

General Description

The SY81012 develops a high efficiency synchronous step-down DC/DC regulator capable of delivering 12A current. The device integrates high-side power switch and low-side synchronous rectifier with very low $R_{DS(ON)}$ to minimize the conduction loss. It provides accurate regulation for a variety of loads with an accurate ±1% voltage reference (V_{REF}) over T_J= -40°C to 125°C.

The SY81012 operates over a wide input voltage range from 2.7V to 16V. The DC/DC regulator adopts the instant PWM architecture to achieve fast transient responses for high step down applications. Cycle-by-cycle current limit, hiccup over current protection and thermal shutdown protect the device during an over current condition

Ordering Information

SY81012 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY81012VDC	QFN3×4-19	

Applications

- Power Module
- Telecom and Networking Systems
- Servers
- LCD-TV/Net-TV/3DTV
- Set Top Box
- Notebook
- High Power AP

Features

- Wide Input Voltage Range:
  - 3.6V to 16V if VCC is Supplied by Internal LDO
  - 2.7V to 16V if VCC is Supplied by External 3.3V DC Source
- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 12.6mΩ/4.3mΩ
- 0.6V ±1% Voltage Reference Over Temperature Range (T_J = -40°C to 125°C)
- Adopt Constant-on-time Architecture and Frequency Lock Loop
- Instant PWM Architecture to Achieve Fast Transient Response.
- 600kHz, 800kHz and 1000kHz Switching Frequency Operation Selected by MODE Pin
- PFM/FCCM Light Load Operation Mode Selected by MODE pin.
- Programmable Bottom Valley Limit by ILMT pin
- Reliable Protection Mode: Auto-Recovery Mode for UVP, UVLO, OTP and OVP
- Cycle-by-cycle Valley Current Limit and Peak Current Limit
- Cycle-by-cycle Reverse Current Limit
- Internal Soft-start Limits the Inrush Current
- Programmable Soft-start Time by SS Pin
- Smooth Soft-start with Output Pre-biased Function
- Adjustable Input Voltage UVLO by EN Pin
- Power Good Indicator
- Differential Output Voltage Remote Sense
- Output Discharge Function
- RoHS Compliant and Halogen Free
- Compact Package: QFN3×4-19

Typical Application

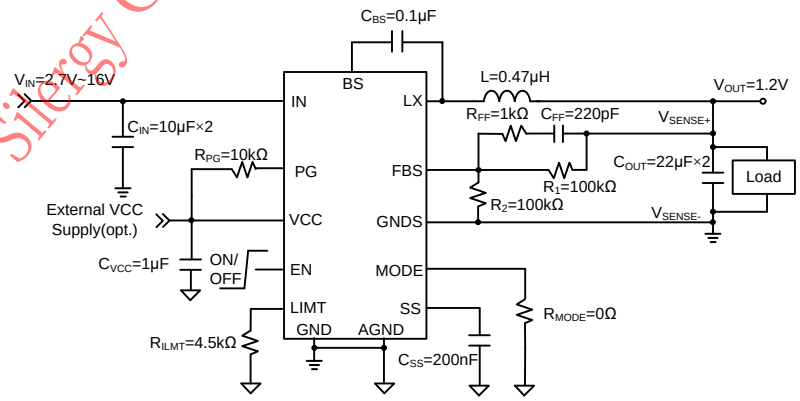


Figure1. Typical Application Circuit

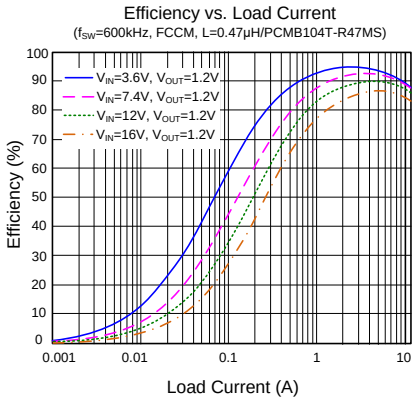
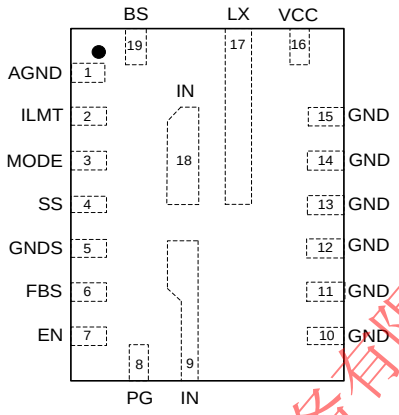


Figure2. Efficiency vs. Load Current

Pinout (top view)



(QFN3×4-19)

Top Mark: **DAY*xyz*** (Device code: **DAY**, ***x=year code, y=week code, z= lot number code***)

Pin No	Pin Name	Pin Description
1	AGND	Analog ground.
2	ILMT	Bottom MOSFET current limit set pin. Connect a resistor to AGND to set the inductor valley current limit value.
3	MODE	Operation mode selection. Program MODE to select FCCM/PFM, and the operating switching frequency.
4	SS	External soft-start Voltage pin. Soft-start time can be adjusted by adding an appropriate external capacitor between this pin and AGND pin. IC actual soft-start time is determined by the slower ramp between internal SS voltage and external SS voltage.
5	GNDS	Remote sense negative input. Connect this pin directly to the negative side of the voltage sense point. Short to GND if remote sense is not used.
6	FBS	Remote sense positive input. Connect to the center point of resistor divider.
7	EN	Enable pin. Pull low to disable the device and pull high to enable the device. Can be used to set the input voltage on and off threshold (adjust UVLO) by using two additional resistors. Do not leave this pin floating.
8	PG	Power good Indicator. Open drain output when the output voltage is within 93.5% to 120% of regulation point.
9, 18	IN	Input pin. Decouple this pin to GND pin with at least a 20μF ceramic capacitor.
10, 11, 12, 13, 14, 15	GND	Power GND.
16	VCC	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Decouple this pin to GND with at least one 1μF ceramic capacitor. Make one Kelvin connection from VCC capacitor negative plate to the AGND pin.
17	LX	Inductor pin. Connect this pin to the switching node of inductor.
19	BS	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS and the LX pin.

Block Diagram

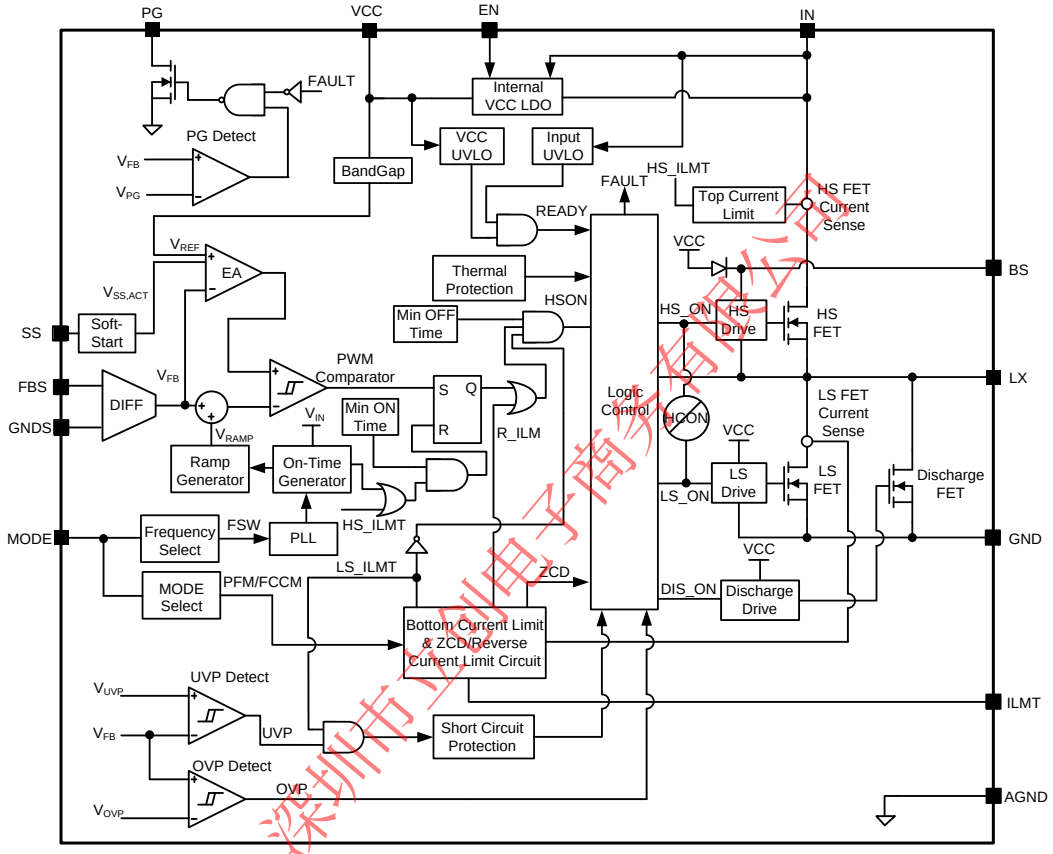


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 18V
ILMT, EN, MODE, SS, LX Voltage ---------- -0.3V to V_{IN}+0.3V
Dynamic LX Voltage in 25ns Duration ---------- GND-5V to V_{IN}+5V
BS ---------- V_{LX}-0.3V to V_{LX}+4V
FBS, GNDS, AGND, VCC, PG Voltage ---------- -0.3V to 4V
Maximum Power Dissipation, $P_{D, MAX}$ @ T_A=25°C, QFN3×4-19 ---------- 4W
Package Thermal Resistance (Note2)
θ_{JA} ---------- 25°C/W
θ_{JC} ---------- 5°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.7V to 16V
Output Voltage ---------- 0.6V to 5.5V
VCC Bias External Voltage ---------- 3.12V to 3.6V
EN Supply Voltage ---------- 0V to V_{IN}
Maximum Output Current ---------- 12A
Maximum Output Current Limit ---------- 14A
Maximum Inductor Peak Current ---------- 17A
Junction Temperature Range ---------- -40°C to 125°C

Electrical Characteristics

(V_{IN} = 12V, T_J = -40°C to +125°C. Typical values are at T_J = 25°C, unless otherwise specified. The values are guaranteed by test, design or statistical correlation)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.7		16	V
Output Voltage Range	V_{OUT}		0.6		5.5	V
Input UVLO Rising Threshold	$V_{IN,UVLO}$		2.52	2.6	2.68	V
Input UVLO Hysteresis	$V_{IN,HYS}$			200		mV
VCC UVLO Rising Threshold	$V_{VCC,UVLO}$				2.5	V
VCC UVLO Hysteresis	$V_{VCC,HYS}$			100		mV
VCC Regulator Output Voltage	V_{CC}	I_{VCC}=0mA	3.1	3.25	3.4	V
VCC Load Regulation	$V_{CC,REG}$	I_{VCC}=25mA		1.8		%V_{CC}
Quiescent Current	I_Q	V_{EN}=2V, V_{FBS} = 0.65V, PFM mode, No Switching		650	850	μA
Shutdown Current	I_{SHDN}	V_{EN}=0V, T_J=25°C		3	5	μA
Feedback Reference Voltage	V_{REF}	-40°C <T_J< 125°C	0.594	0.600	0.606	V
Error Amplifier Offset	V_{OS}	(Note 4)	-3		3	mV
FBS Input Current	I_{FBS}	V_{EN}=2V, V_{FBS} = 1V	-50	0	50	nA
SS Charging Current	I_{SS1}	V_{SS}=0V		42		μA
SS Pull Down Current	I_{SS2}	V_{SS}=1V		34		mA
Minimum Soft-Start Time	$t_{SS,MIN}$	C_{SS}=1nF (Note 4)		1		ms
Top FET $R_{DS(ON)}$	$R_{DS(ON)1}$	V_{BS-LX} = 3.3V, T_J=25°C		12.6	18.9	mΩ
Bottom FET $R_{DS(ON)}$	$R_{DS(ON)2}$	V_{CC} = 3.3V, T_J=25°C		4.3	6.5	mΩ
EN Rising Threshold	$V_{EN,R}$		1.16	1.21	1.26	V
EN Threshold Hysteresis	$V_{EN,HYS}$			0.23		V
EN Input Current	I_{EN}	V_{EN}=2V		0		μA
Discharge FET Resistance	R_{DIS}			60		Ω
Top FET Current Limit	$I_{LMT,TOP}$		14	15.5	17	A
Bottom FET Reverse Current Limit	$I_{LMT,RVS}$		3.5	4.5	6.6	A
Reverse Current Limit Blank Time	$t_{RCL,BLK}$	(Note 4)	40	60		ns
ILMT Pin Output Voltage	V_{ILMT}		0.77	0.8	0.83	V
I_{ILMT} to $I_{LMT,BOT}$ Ratio	$I_{ILMT}/I_{LMT,BOT}$	$I_{LMT,BOT}$ >5A	12	13.3	14.6	μA/A
Output OVP Threshold	V_{OVP}		110	120	130	%V_{REF}
Output UVP Threshold	V_{UVP}		45	50	55	%V_{REF}
Output UVP Delay	$t_{UVP,DLY}$	(Note 4)		20		μs
UVP/OCP Hiccup ON Time	$t_{HICCUP,ON}$	C_{SS}=1nF (Note 4)		3		ms
UVP/OCP Hiccup OFF Time	$t_{HICCUP,OFF}$	C_{SS}=1nF (Note 4)		15		ms

Power Good Threshold	V_{PG}	V_{FBS} falling, PG high to low	76	79	82.5	$\%V_{REF}$
		V_{FBS} rising, PG low to high	88	93.5	97	$\%V_{REF}$
		V_{FBS} rising, PG high to low	110	120	130	$\%V_{REF}$
		V_{FBS} falling, PG low to high	100	103.5	107.5	$\%V_{REF}$
Power Good Leakage Current	$I_{PG,LKG}$	PG voltage is 3.3V		3	5	μA
Power Good Delay	$t_{PG,R}$	V_{FBS} falling, PG low to high (Note 4)		0.8		ms
	$t_{PG,F}$	V_{FBS} rising, PG high to low (Note 4)		20		μs
Power Good Sink Current Capability	$V_{PG,LOW}$	V_{EN} = 2V, V_{FBS} = 0V, I_{PG}=10mA			0.4	V
Power Good Output Low Voltage	$V_{PG,L}$	V_{IN}=0V, Pull PG to 3.3V through 100kΩ Resistor		550	750	mV
		V_{IN}=0V, Pull PG to 3.3V through 10kΩ Resistor		660	850	mV
Min ON Time	$t_{ON,MIN}$	I_{OUT}=3A (Note 4)		55		ns
Min OFF Time	$t_{OFF,MIN}$	I_{OUT}=3A (Note 4)		150		ns
Switching Frequency	f_{SW}	R_{MODE}=0Ω, I_{OUT}=0A, FCCM, V_{OUT}=1V, T_J=25°C	500	600	700	kHz
		R_{MODE}=30.1kΩ, I_{OUT}=0A, FCCM, V_{OUT}=1V, T_J=25°C	710	800	890	kHz
		R_{MODE}=60.4kΩ, I_{OUT}=0A, FCCM, V_{OUT}=1V, T_J=25°C	900	1000	1100	kHz
Thermal Shutdown Temperature	T_{SD}	T_J rising (Note 4)	140	160		˚C
Thermal Shutdown Hysteresis	T_{HYS}	(Note 4)		30		˚C

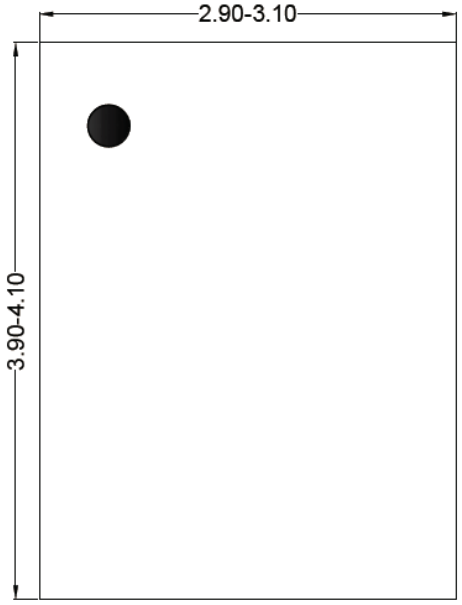
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note2: Package thermal resistance is measured in the natural convection at T_A=25˚C on a 8.5cm×8.5cm size four-layer Silergy Evaluation Board.

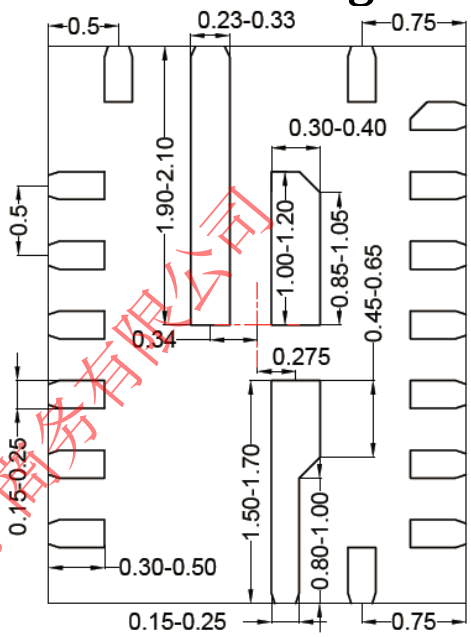
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Guaranteed by design.

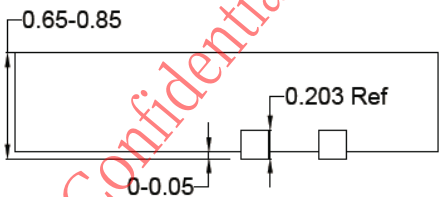
QFN3×4-19 Package Outline Drawing



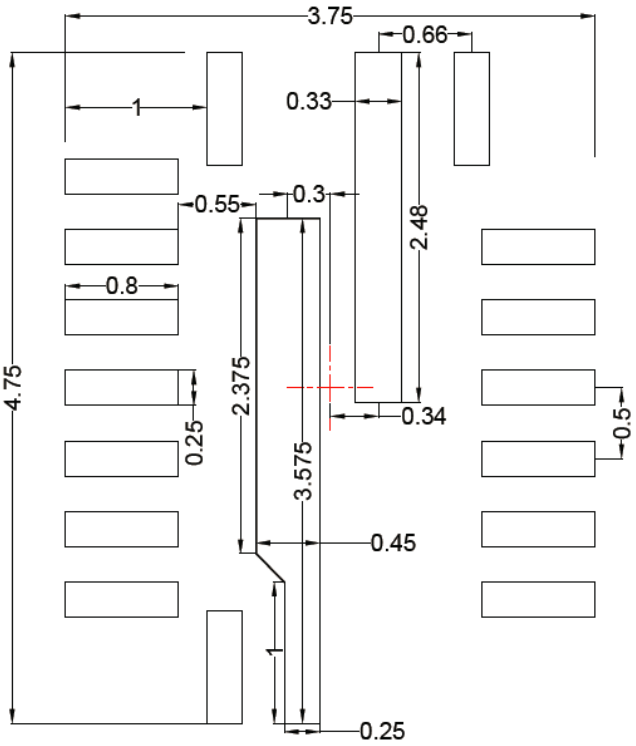
Top view



Bottom view



Front view

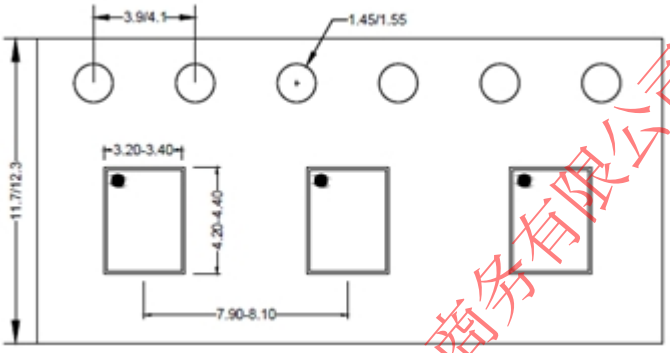


Recommended PCB layout
(Reference only)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr.
2, center line refers chip body center.

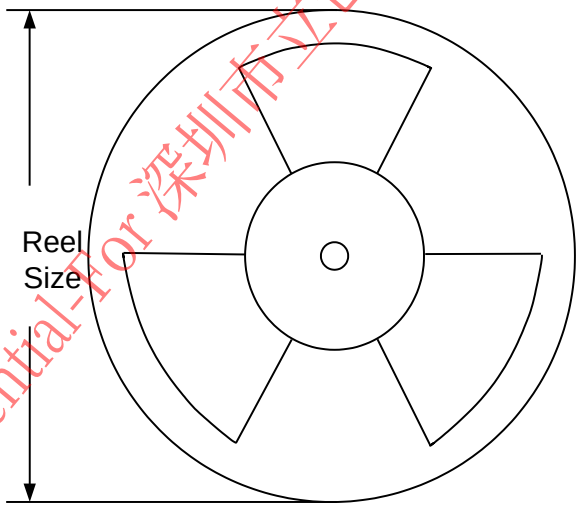
Taping & Reel Specification

1. Taping orientation for packages



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×4	12	8	13"	400	400	5000

3. Others: NA