SY7215A

High Efficiency, 15A Synchronous Step Up Regulator with Accurate Output Current Limit

General Description

SY7215A develops a high efficiency synchronous Boost regulator with programmable output current limit. The IC adopts adaptive constant OFF time and current mode control. The integrated low $R_{DS(ON)}$ switches minimize the conduction loss.

SY7215A features cycle by cycle peak current limit, output short circuit protection and true shutdown. The IC also provides enable control and power good indicator for system sequence control. Low output voltage ripple and small external inductor and capacitor size are achieved with programmable pseudo-constant frequency.

Features

- Input Range: 3-16V
- Programmable Pseudo-constant Frequency
- Low $R_{DS(ON)}$ Internal Switch
  Main FET: 9mΩ
  Rectified FET: 12mΩ
  Disconnection FET: 12mΩ
- True Shutdown Function
- Programmable Output Current Limit
- Internal Soft-start Limits the Inrush Current
- Input Voltage UVLO
- Over Temperature Protection
- Over Voltage Protection
- Output Short Circuit Protection
- Minimum ON Time: 100ns typical
- Minimum OFF Time: 120ns typical
- RoHS Compliant and Halogen Free
- Compact Package:QFN4×4-18

Ordering Information

SY7215 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY7215ARDC	QFN4×4-18	----

Applications

- Power Bank
- High Power AP

Typical Applications

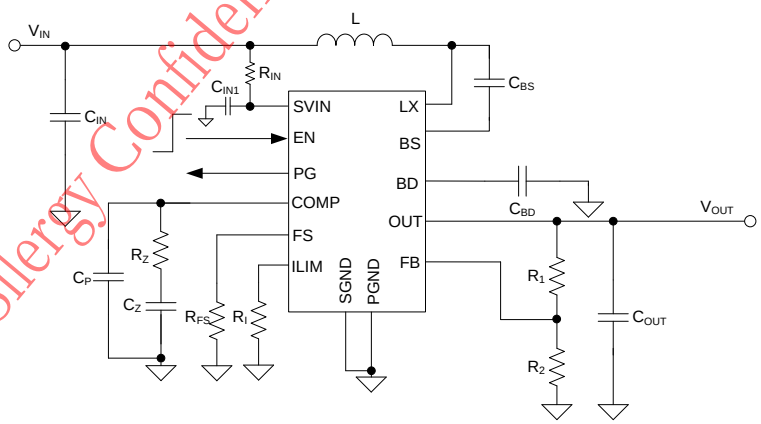


Figure1. Schematic Diagram

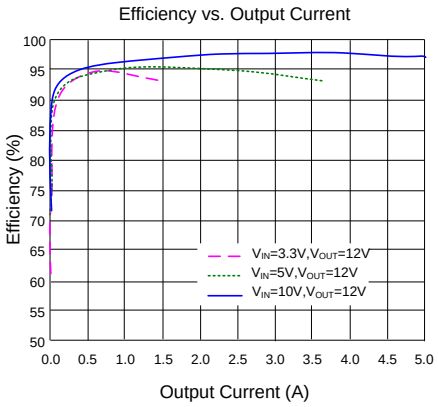
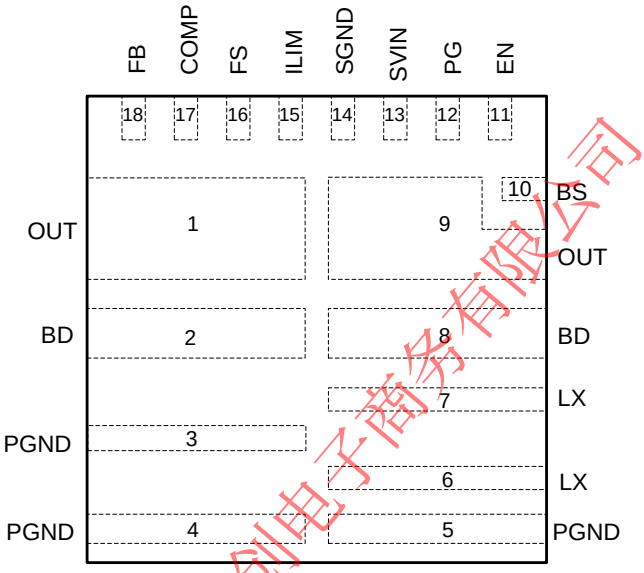


Figure2. Efficiency vs. Output Current

Pinout (top view)



(QFN4×4-18)

Top mark: **BET*xyz*** (Device code: BET, ***x=year code, y=week code, z= lot number code***)

Pin Name	QFN4x4-18	Pin Description
SVIN	13	IC power supply input pin. Decouple this pin to SGND pin with 1μF ceramic cap.
SGND	14	Signal ground pin.
PGND	3,4,5	Power ground pin.
LX	6,7	Inductor node. Connect an inductor from power input to LX pin.
FB	18	Feedback pin. Connected to the center of resistor voltage divider to program the output voltage: V_{OUT}=1V×(R1/R2+1)
EN	11	Enable control. Pull high to turn on the IC. Do not leave it floating.
ILIM	15	Output current limit program pin. Connect a resistor R_{LIM} from this pin to SGND to program output current limitation threshold. I_{LIM}(A)=15(V)/ R_{LIM}(kΩ)
OUT	1,9	Boost converter output pin.
BD	2,8	Connected to the Drain of internal Disconnect FET. Bypass at least 4.7μF ceramic cap to PGND.
BS	10	Boot-strap pin. Supply rectified FET's gate driver. Decouple this pin to LX with 0.1μF ceramic cap.
FS	16	Switching frequency setting pin. Connect a resistor from this pin to ground to program the switching frequency. F_{SW}(kHz)=1.4×10^6/R_{FS}(Ω)$^{0.645}$.
PG	12	Power good indicator. Open drain output, pull low when the output < 90% of regulation voltage, high impendence otherwise.
COMP	17	Loop compensation pin. Connect a RC network across this pin and ground to stabilize the control loop.

Block Diagram

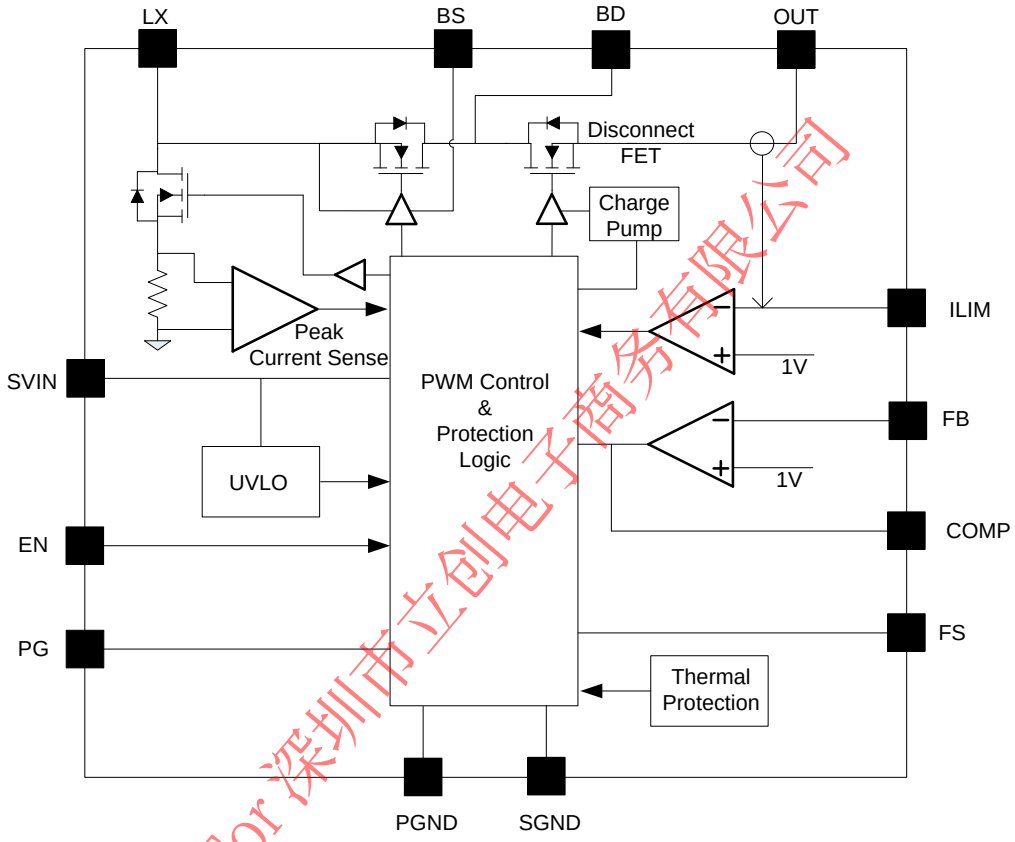


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

SVIN, LX, EN, ILIM, OUT, BD, BS, FS, PG, COMP ---------- -0.3V to 18V
FB ---------- 4V
BS-LX ---------- 4V
Power Dissipation, P_D @ T_A = 25°C QFN4×4-18 ---------- 3.4W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 30°C/W
θ_{JC} ---------- 3.2°C/W
Junction Temperature Range ---------- -40°C to 125°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

SVIN ---------- 3V to 16V
Junction Temperature Range ---------- - 40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} =5V, V_{OUT}=12V, I_{OUT}=100mA, T_A = 25°C unless otherwise specified)

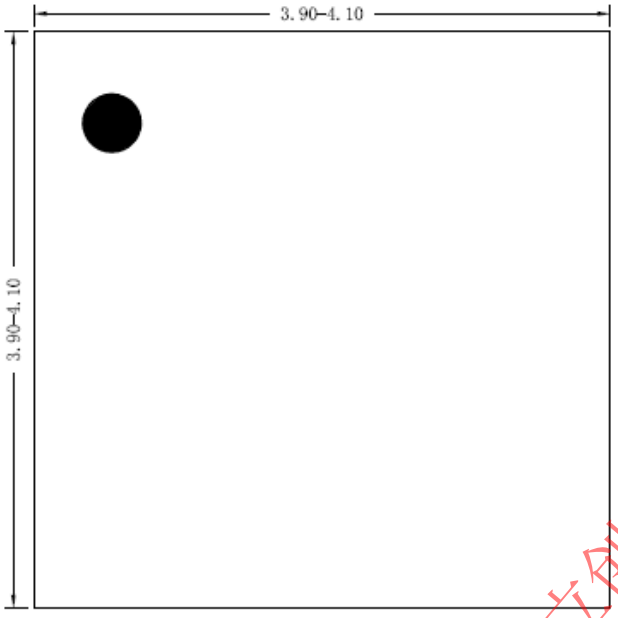
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		3		16	V
Output Voltage Range	V_{OUT}		V_{IN}×1.1		16	V
Output OVP Threshold	V_{FB_OVP}	V_{FB} Rising	110%	115%	120%	V_{REF}
Quiescent Current	I_Q	V_{OUT}=13V			230	μA
Shutdown Current	I_{SHDN}	EN=0			5	μA
FB Leakage Current	I_{FB}		-50		50	nA
Main N-FET RON	$R_{DS(ON)\_M}$			9		mΩ
Rectified N-FET RON	$R_{DS(ON)\_R}$			12		mΩ
Disconnect N-FET RON	$R_{DS(ON)\_D}$			12		mΩ
Main N-FET Current Limit	$I_{LIM,PEAK}$		15		20	A
Switching Frequency	F_{SW}	R_{FS}=390kΩ		345		kHz
Switching Frequency Programmable Range			250		1000	kHz
Feedback Reference Voltage	V_{REF}		0.985	1	1.015	V
IN UVLO Rising Threshold	$V_{IN,UVLO}$				2.85	V
UVLO Hysteresis	$V_{HYS,UVLO}$			0.2		V
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Output Current Limit	I_{LIM}	R_{LIM}=15kΩ		1		A
Output Current Limit Programmable Range	$I_{LIM,OUT}$	V_{OUT}<=5V	1		5	A
		V_{OUT}>5V	1		4	A
Minimum ON Time	$t_{ON,MIN}$			100		ns
Minimum OFF Time	$t_{OFF,MIN}$			120		ns
Error Amplifier Trans-conductance	g_m			100		μS
Current Sense Gain	R_i			75		mΩ
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

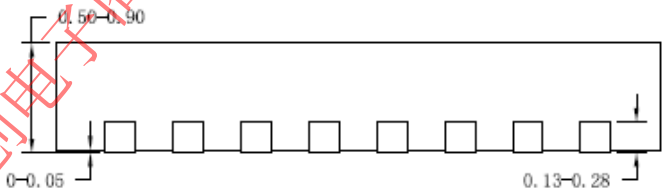
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a two-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

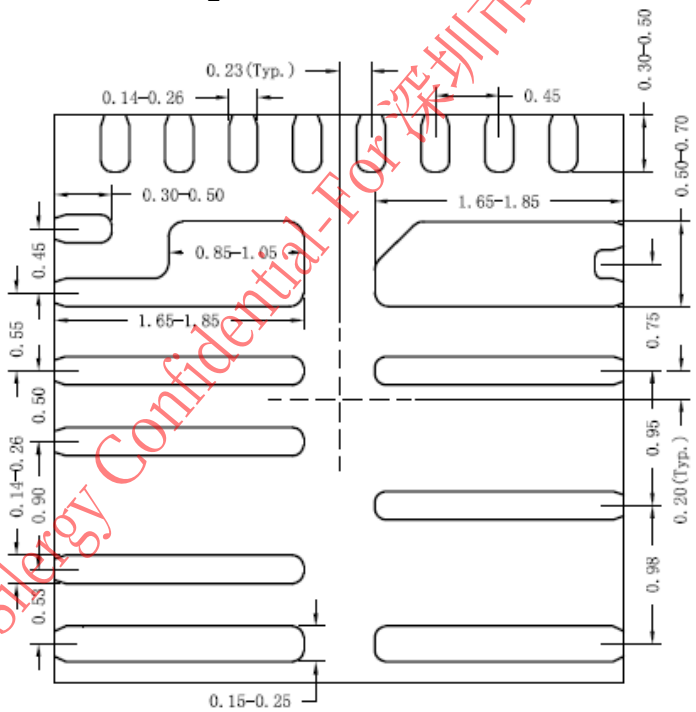
QFN4×4-18 Package Outline & PCB layout design



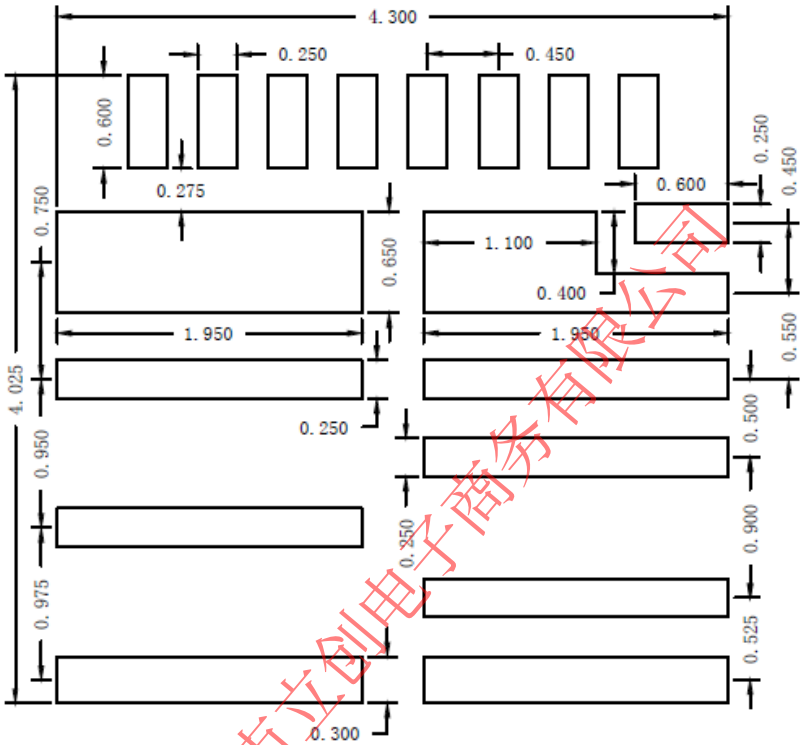
Top View



Side View



Bottom View



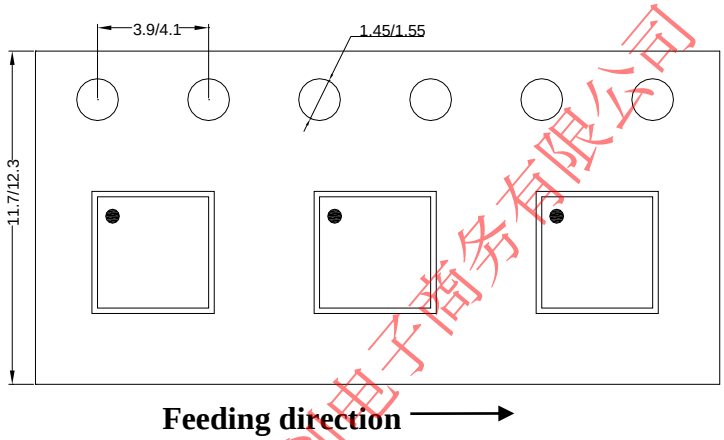
Recommended PCB layout (Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr**

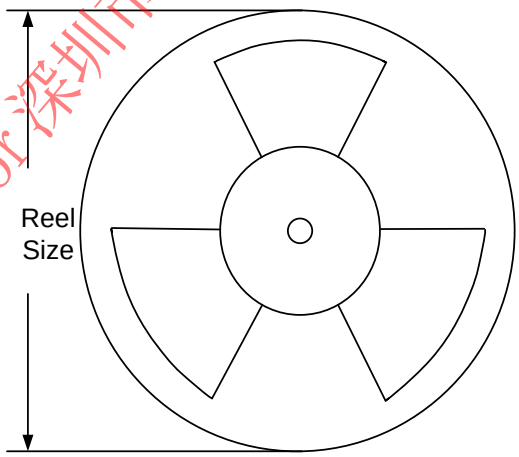
Taping & Reel Specification

1. Taping orientation

QFN4×4



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN4×4	12	8	13"	400	400	5000

3. Others: NA