## Features

- Transient protection for high-speed data lines
  - IEC 61000-4-2 (ESD) ±25kV (Air)
    ±17kV (Contact)
  - IEC 61000-4-4 (EFT) 40A (5/50 ns)
  - Cable Discharge Event (CDE)
- Package optimized for high-speed lines
- Ultra-small package (2.5mm×1.0mm×0.55mm)
- Protects four data lines
- Low capacitance: 1.0pF (Typical)
- Low leakage current: 0.1μA @ $V_{RWM}$ (Maximum)
- Low clamping voltage
- Each I/O pin can withstand over 1000 ESD strikes for ±8kV contact discharge
- ROHS compliant

## Applications

- Serial ATA
- PCI Express
- Desktops, Servers and Notebooks
- MDDI Ports
- USB 2.0/3.0/3.1 Power and Data Line Protection
- Display Ports
- High Definition Multi-Media Interface (HDMI)
- Digital Visual Interfaces (DVI)

## Mechanical Characteristics

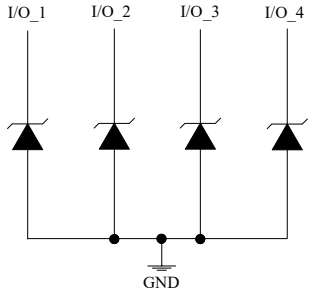
- DFN-10L package
- Flammability Rating: UL 94V-0
- Marking: Part number
- Packaging: Tape and Reel

## Description

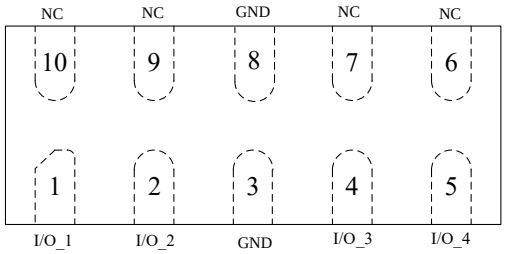
TT0334VPX is an ultra-low capacitance Transient Voltage Suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With typical capacitance 1.0pF only, TT0334VPX is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD), Level 4 (±15kV air, ±8kV contact discharge), IEC 61000-4-4 (electrical fast transient - EFT) (40A, 5/50 ns), very fast charged device model (CDM) ESD and cable discharge event (CDE), etc.

TT0334VPX uses ultra-small DFN-10L package. Each TT0334VPX device can protect four high-speed data lines. The combined features of ultra-low capacitance, ultra-small size and high ESD robustness make TT0334VPX ideal for high-speed data ports and high-frequency lines (e.g., HDMI & DVI) applications. The low clamping voltage of the TT0334VPX guarantees a minimum stress on the protected IC.

## Circuit Diagram




## Pin Configuration



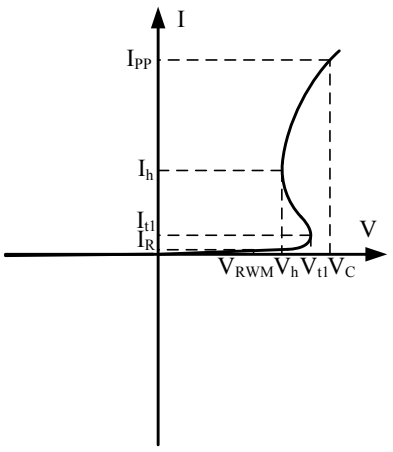

DFN-10L
(Top View)

## Absolute Maximum Rating

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $I_{PP}$ | Peak Pulse Current(tp=8/20us) | 10 | A |
| $V_{ESD}$ | ESD per IEC 61000-4-2(Air)<br>ESD per IEC 61000-4-2 (Contact) | ±25<br>±17 | kV |
| $T_{OPT}$ | Operating Temperature | -55/+125 | °C |
| $T_{STG}$ | Storage Temperature | -55/+150 | °C |

## Electrical Characteristics (T = 25°C)

| Symbol | Parameter |
|---|---|
| $V_{RWM}$ | Nominal Reverse Working Voltage |
| $I_R$ | Reverse Leakage Current @ $V_{RWM}$ |
| $V_{t1}$ | Trigger Voltage |
| $I_{t1}$ | Trigger Current @ $V_{t1}$ |
| $V_h$ | Holding Voltage |
| $I_h$ | Holding Current @ $V_h$ |
| $V_C$ | Clamping Voltage @ $I_{PP}$ |
| $I_{PP}$ | Maximum Peak Pulse Current |
| $V_F$ | Forward Voltage @ $I_F$ |
| $C_{ESD}$ | Parasitic Capacitance |

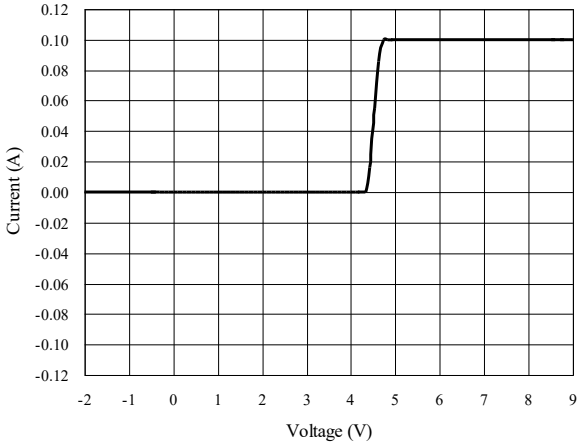


Uni-Directional TVS

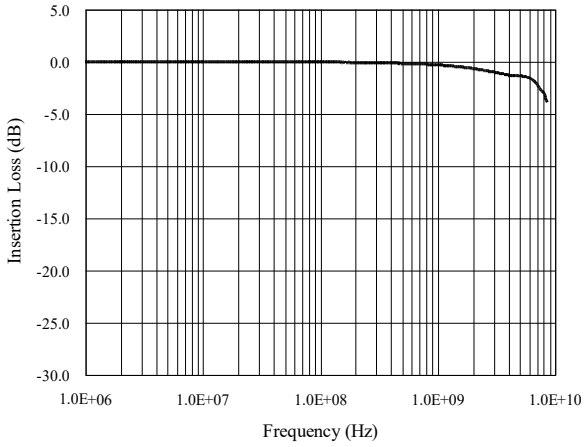
| Symbol | Test Condition | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $V_{RWM}$ | | | | 3.3 | V |
| $I_R$ | $V_{RWM}$ = 3.3V, T = 25°C | | 0.01 | 0.1 | μA |
| $V_{t1}$ | $I_{t1}$ = 1μA | 6.0 | | 7.5 | V |
| $V_h$ | $I_h$ = 10mA | 3.5 | | 5.0 | V |
| $V_C$ | Any I/O to Ground<br>$I_{PP}$ = 4A, $t_p$ = 8/20μs | | | 8.0 | V |
| $V_C$ | $I_{PP}$=8.0A, $t_p$ =100ns (1) | | 7.0 | | V |
| | $I_{PP}$=16.0A, $t_p$= 100ns (1) | | 8.0 | | V |
| $R_{dyn}$ | IEC61000-4-2 0-6KV, T=25°C<br>Contact, I/O to GND | | 0.3 | | Ω |
| $C_{ESD}$ | $V_R$ = 0V, f = 1MHz<br>Between I/O and GND | | 1.0 | | pF |
| $C_{ESD}$ | $V_R$ = 0V, f = 1MHz<br>Between I/O and I/O | | 0.5 | | pF |

*Notes:(1)Measurements performed using a 100ns Transmission Line Pulse(TLP) system.*

## Voltage Sweeping of I/O to GND

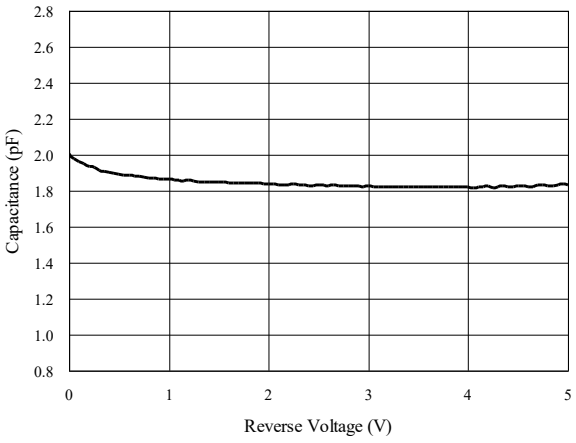



## Insertion Loss S21 of I/O to GND

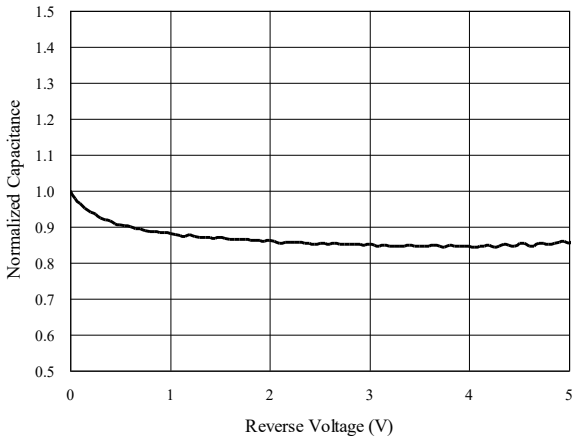



## Capacitance *vs.* Voltage of I/O to GND (f = 1MHz)

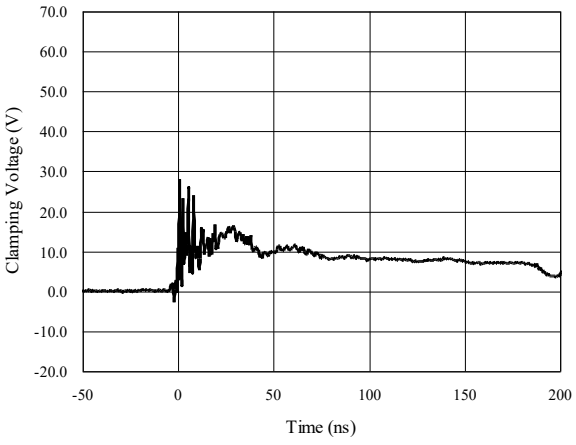
Capacitance *vs.* Reverse Voltage



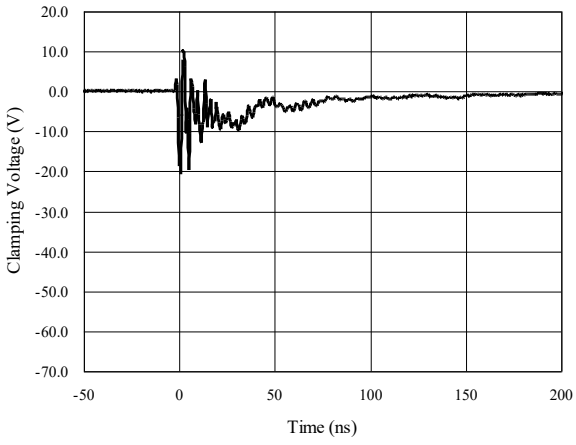

Normalized Capacitance *vs.* Reverse Voltage




## ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)




## ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)



# Application Information

## Pin Connection in PCB

TT0334VP provides ESD protection for four data lines simultaneously. The pin connection is shown in the figure below.

Four parallel data lines, from inner IC to I/O port connector, could connect to TT0334VPX four I/O pins directly. Pin 3&8 of TT0334VPX is the GND pin, which should connect to the GND of PCB. The wire should be as short as possible in order to minimize the parasitic inductance.

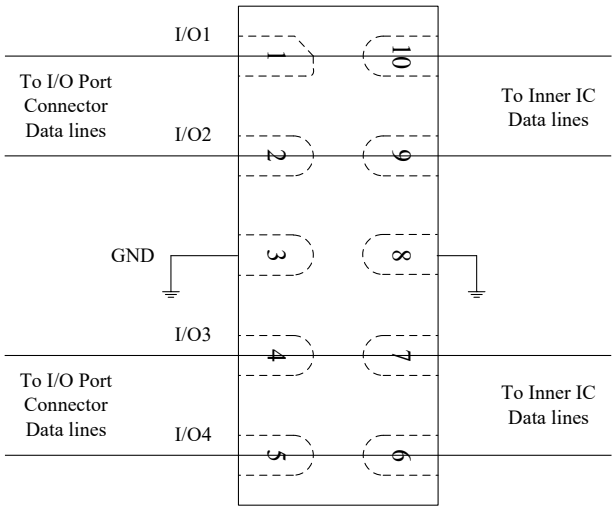



Figure 1 TT0334VP pin connection in PCB

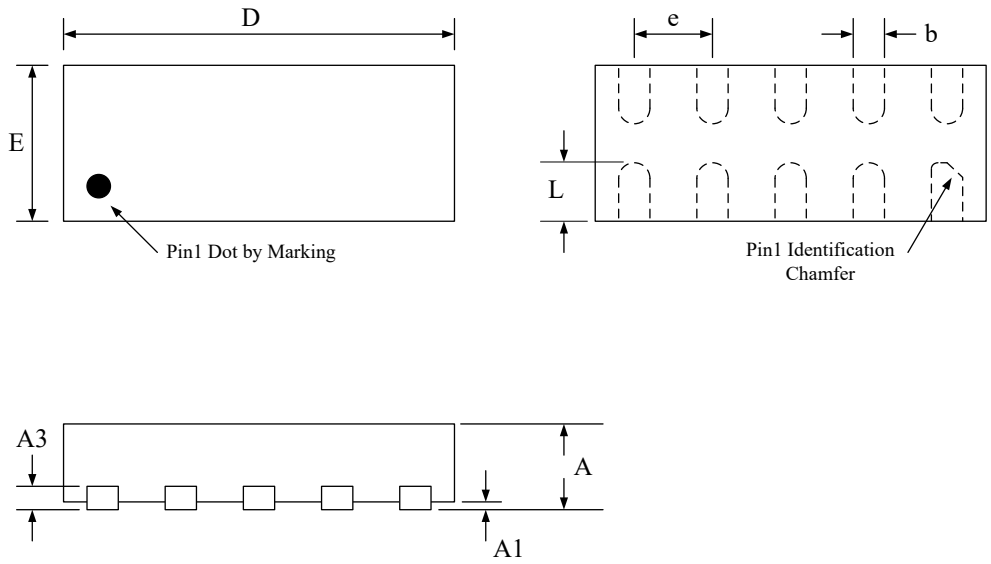
## PCB Layout Guidelines

For optimum ESD protection and the whole circuit performance, the following PCB layout guidelines are recommended:

- TT0334VPX GND pin to the PCB GND rail path should be as short as possible. It could reduce the ESD transient return path to GND.
- The vias connecting TT0334VPX GND pins to the PCB GND should be wide.
- Place TT0334VPX as close to the connector port as possible. It could reduce the parasitic inductance and restrict ESD coupling into adjacent traces.
- Avoid running critical signals near board edges.

## Package Outline

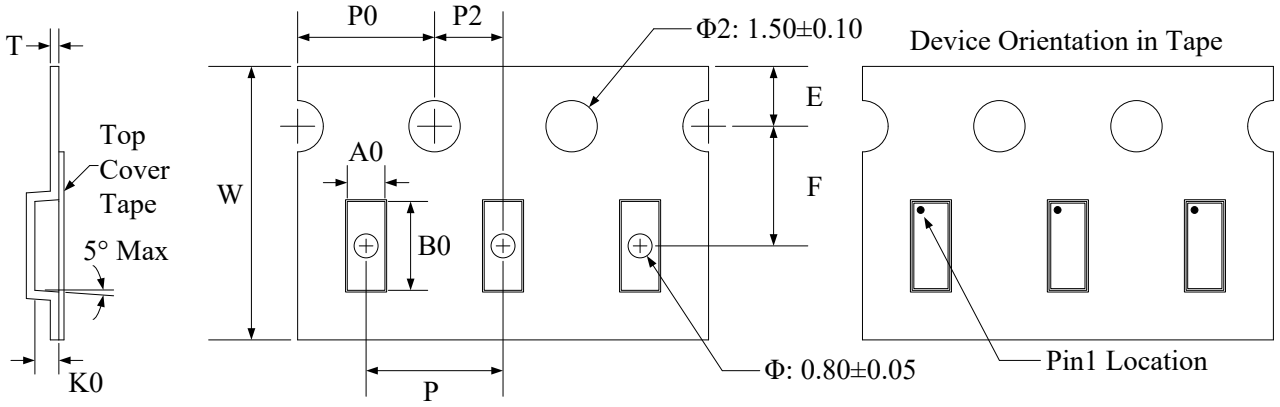
- ❑ DFN-10L package
- ❑ Thermally-Enhanced
- ❑ MSL-1 Level




Package Dimensions (Controlling dimensions are in millimeters)

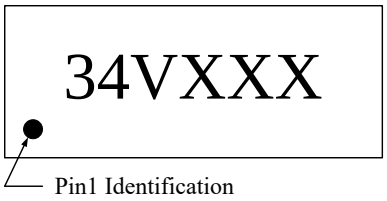
| Symbol | Dimensions (mm) | | Dimensions (Inches) | |
|---|---|---|---|---|
| | Minimum | Maximum | Minimum | Maximum |
| A | 0.500 | 0.600 | 0.020 | 0.024 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.15REF. | | 0.006REF. | |
| b | 0.150 | 0.250 | 0.006 | 0.010 |
| D | 2.450 | 2.550 | 0.096 | 0.100 |
| E | 0.950 | 1.050 | 0.037 | 0.041 |
| e | 0.500 BSC | | 0.020 BSC | |
| L | 0.300 | 0.400 | 0.012 | 0.016 |

## Tape and Reel Specification




| Symbol | W | A0 | B0 | K0 | E | F | P | P0 | P2 | T |
|---|---|---|---|---|---|---|---|---|---|---|
| Dimensions (mm) | 8.00+0.3 -0.1 | 1.23±0.05 | 2.7±0.05 | 0.7±0.05 | 1.75±0.1 | 3.5±0.05 | 4.0±0.1 | 4.0±0.1 | 2.0±0.05 | 0.25±0.02 |

## Marking Codes




## Ordering Information

| Part Number | Working Voltage | Quantity Per Reel | Reel Size |
|---|---|---|---|
| TT0334VPX | 3.3V | 3,000 | 7 Inch |

**Note:**

(1) "34V" is part number fixed.

(2) "XXX"is the last 3 characters of the wafer's Lot No.