Features

- Transient protection for high-speed data lines
  - IEC 61000-4-2 (ESD) ±25kV (Air)
  - ±17kV (Contact)
  - IEC 61000-4-4 (EFT) 40A (5/50 ns)
  - Cable Discharge Event (CDE)
- Package optimized for high-speed lines
- Ultra-small package (4.1mm×2.0mm×0.55mm)
- Protects six data lines
- Low capacitance: 0.25pF Typical(I/O-GND)
- Low leakage current: 0.1μA @ V_{RWM} (Typical)
- Low clamping voltage
- Each I/O pin can withstand over 1000 ESD strikes for ±8kV contact discharge

Description

TT0506STX is an ultra-low capacitance Transient Voltage Suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With typical capacitance of 0.25pF only, TT0506STX is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD), Level 4 (±15kV air, ±8kV contact discharge), IEC 61000-4-4 (electrical fast transient - EFT) (40A, 5/50 ns), very fast charged device model (CDM) ESD and cable discharge event (CDE), etc.

TT0506STX uses ultra-small DFN4120-10L package. Each TT0506STX device can protect six high-speed data lines The combined features of ultra-low capacitance, ultra-small size and high ESD robustness make TT0506STX ideal for high-speed data ports and high-frequency lines (e.g., HDMI & DVI) applications. The low clamping voltage of the TT0506STX guarantees a minimum stress on the protected IC.

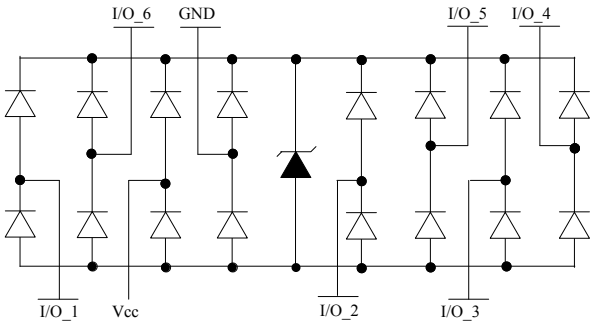
Applications

- Serial ATA
- PCI Express
- Desktops, Servers and Notebooks
- MDDI Ports
- USB 2.0/3.0 Power and Data Line Protection
- Display Ports
- High Definition Multi-Media Interface (HDMI)
- Digital Visual Interfaces (DVI)

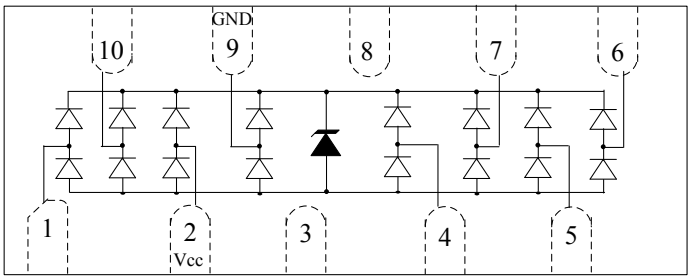
Mechanical Characteristics

- DFN4120-10L package
- Flammability Rating: UL 94V-0
- Marking: Part number
- Packaging: Tape and Reel

Circuit Diagram



Pin Configuration



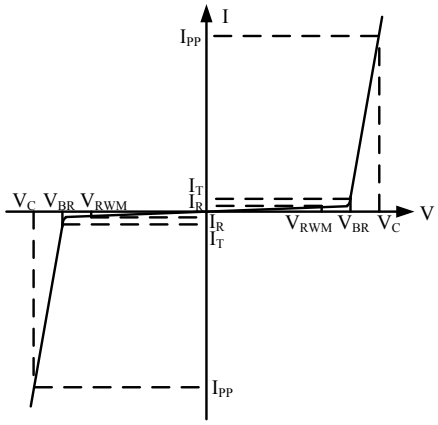
DFN4120-10L
(Top View)

Absolute Maximum Rating

Symbol	Parameter	Value	Units
V_{ESD}	ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	±25 ±17	kV
T_{OPT}	Operating Temperature	-55/+125	°C
T_{STG}	Storage Temperature	-55/+150	°C

Electrical Characteristics (T = 25°C)

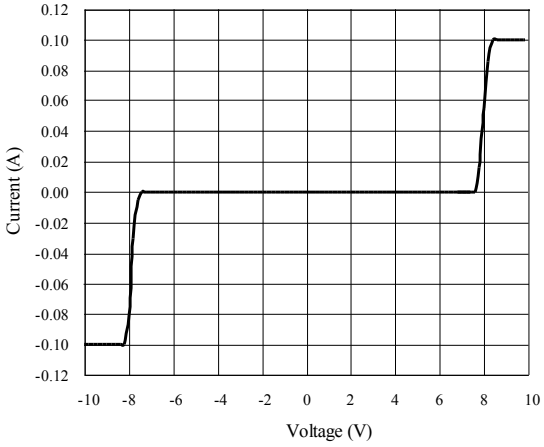
Symbol	Parameter
V_{RWM}	Nominal Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Reverse Breakdown Voltage @ I_T
I_T	Test Current for Reverse Breakdown
V_C	Clamping Voltage @ I_{PP}
I_{PP}	Maximum Peak Pulse Current
C_{ESD}	Parasitic Capacitance
V_R	Reverse Voltage
f	Small Signal Frequency
I_F	Forward Current
V_F	Forward Voltage @ I_F



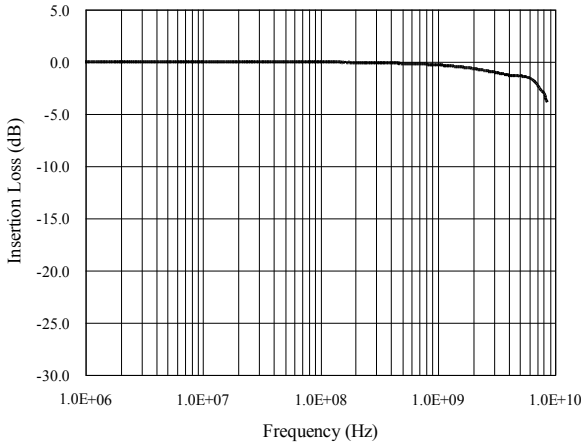
Bi-Directional TVS

Symbol	Test Condition	Minimum	Typical	Maximum	Units
V_{RWM}				5.0	V
I_R	V_{RWM} = 5V, T = 25°C Between I/O and GND		0.1	1.0	μA
V_{BR}	I_T = 1mA Between I/O and GND	7.0	9.0	11.0	V
V_C	I_{PP} = 1A, t_p = 8/20μs Between I/O and GND			12	V
C_{ESD}	V_R = 0V, f = 1MHz Between I/O and GND		0.25	0.35	pF
C_{ESD}	V_R = 0V, f = 1MHz Between I/O and I/O		0.25	0.35	pF

Voltage Sweeping of I/O to GND

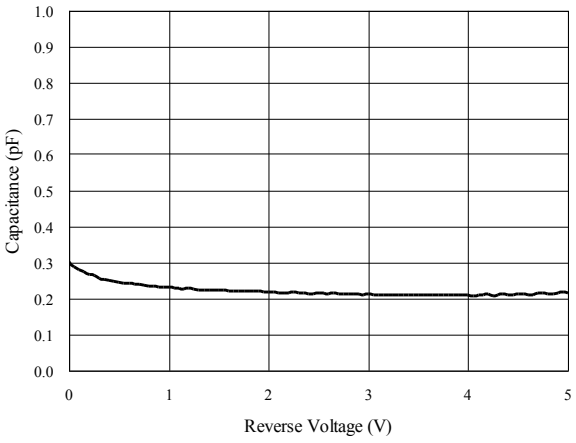


Insertion Loss S21 of I/O to GND

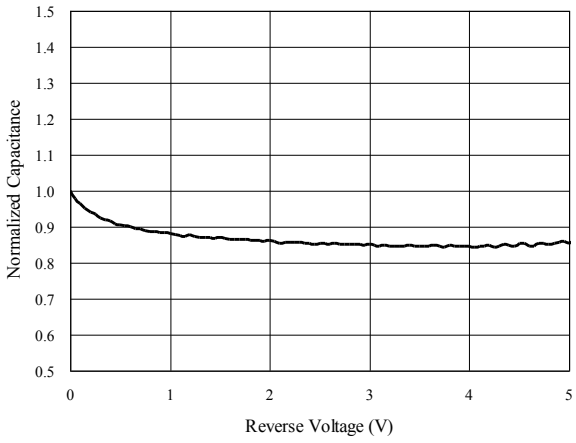


Capacitance *vs.* Voltage of I/O to GND (f = 1MHz)

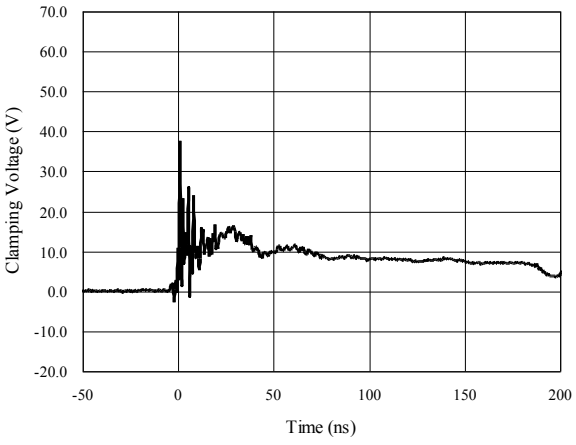
Capacitance *vs.* Reverse Voltage



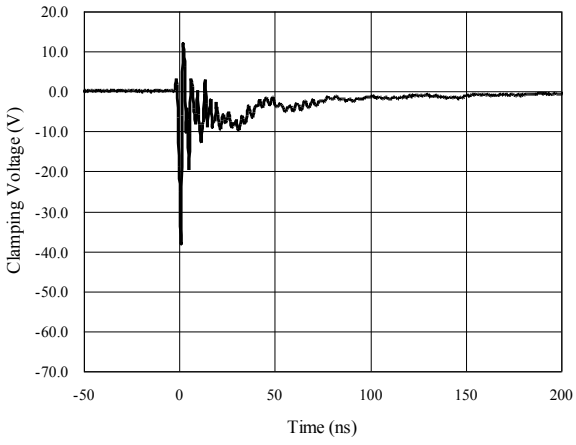
Normalized Capacitance *vs.* Reverse Voltage



ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)



ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)



Application Information

Pin Connection in PCB

TT0506STX provides ESD protection for six data lines simultaneously. The pin connection is shown in the figure below.

Four parallel data lines, from inner IC to I/O port connector, could connect to TT0506STX six I/O pins directly. Pin 9 of TT0506STX is the GND pin, which should connect to the GND of PCB. The wire should be as short as possible in order to minimize the parasitic inductance.

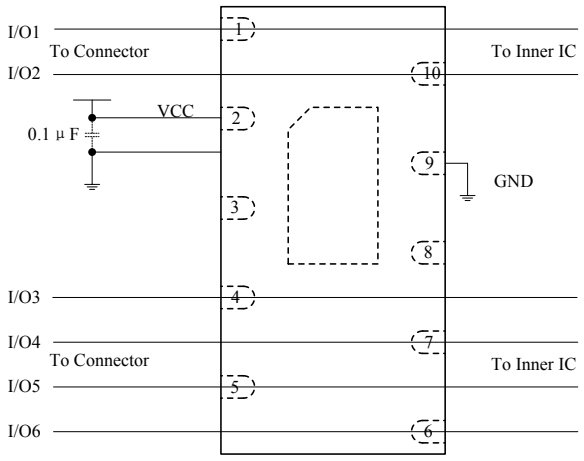


Figure 1 TT0506STX pin connection in PCB providing data lines and power rail line protection.

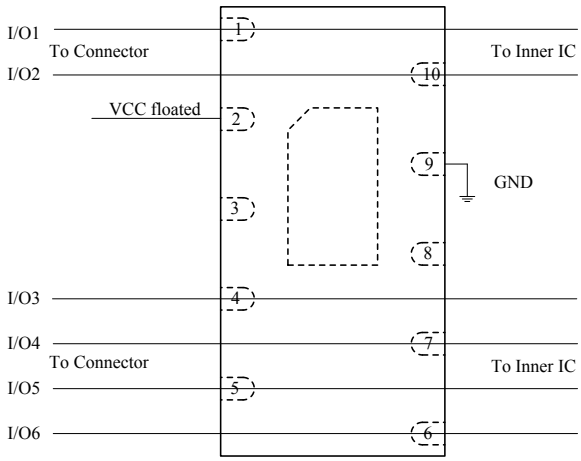


Figure 2 TT0506STX pin connection in PCB providing data line protection. VCC pin is left as floating when no VCC rail is presented in PCB.

PCB Layout Guidelines

For optimum ESD protection and the whole circuit performance, the following PCB layout guidelines are recommended:

- TT0506STX GND pin to the PCB GND rail path should be as short as possible. It could reduce the ESD transient return path to GND.
- The vias connecting TT0506STX GND pins to the PCB GND should be wide.
- Place TT0506STX as close to the connector port as possible. It could reduce the parasitic inductance and restrict ESD coupling into adjacent traces.
- Avoid running critical signals near board edges.

Application Information

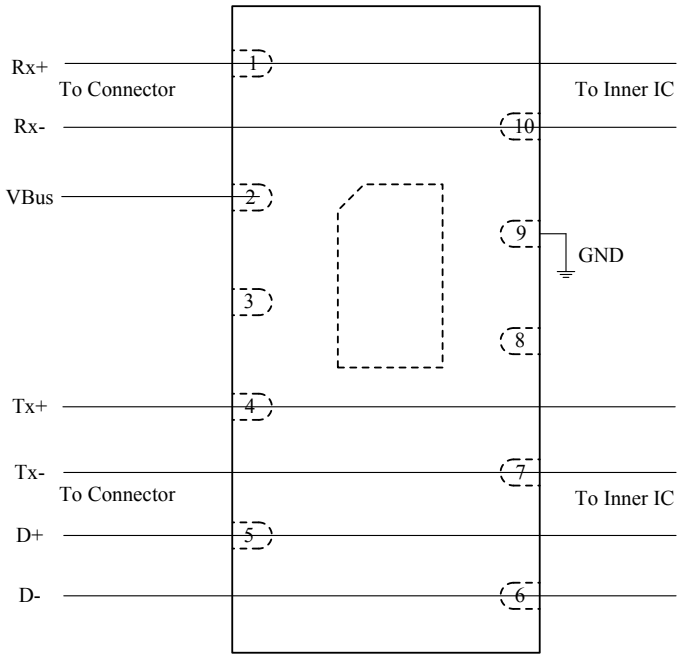
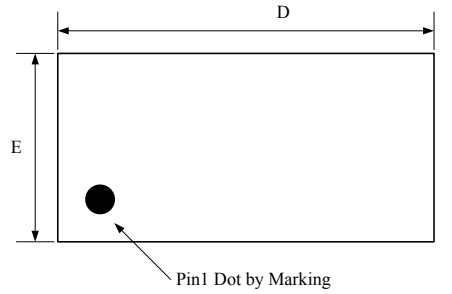


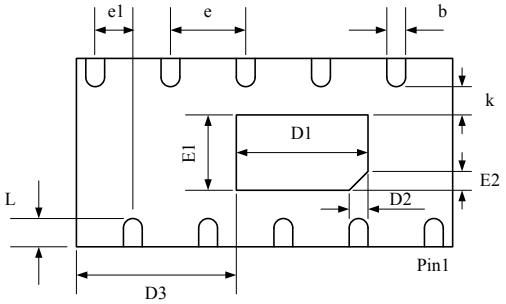
Figure3 TT0506STX pin connection for USB3.0 protection.

Package Outline

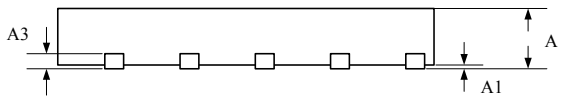
- ❑ DFN4120-10L package
- ❑ Thermally-Enhanced
- ❑ MSL-1 Level



Top View



Bottom View

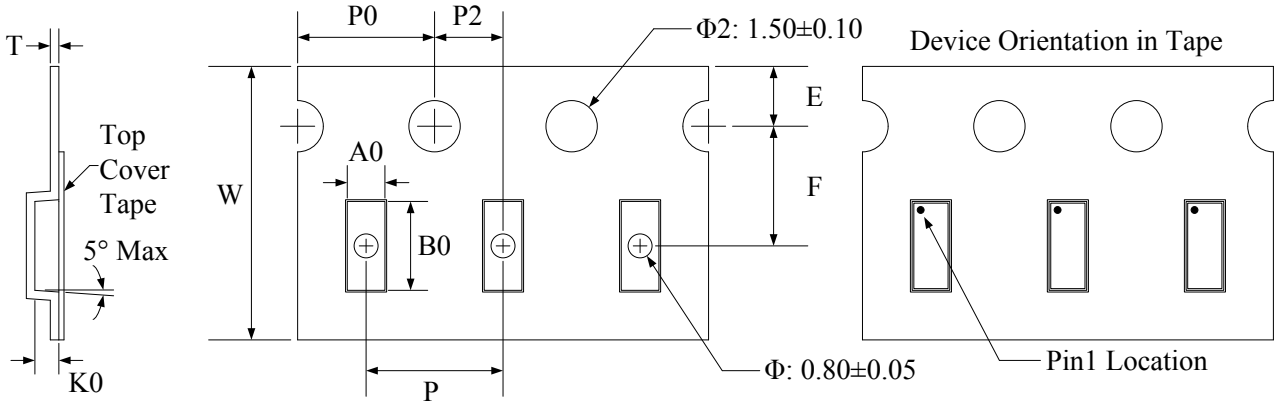


Side View

Package Dimensions (Controlling dimensions are in millimeters)

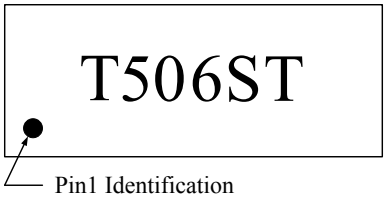
Symbol	Dimensions (mm)		Dimensions (Inches)	
	Minimum	Maximum	Minimum	Maximum
A	0.450	0.550	0.018	0.022
A1	0.000	0.050	0.000	0.002
A3	0.152REF.		0.006REF	
D	4.050	4.150	0.159	0.163
E	1.950	2.050	0.077	0.081
D1	1.300	1.500	0.051	0.059
E1	0.700	0.900	0.028	0.035
D3	1.650	1.850	0.065	0.073
D2	0.200REF		0.008REF	
E2	0.200REF		0.008REF	
k	0.200MIN		0.008MIN	
b	0.150	0.250	0.006	0.010
e	0.800TYP		0.031TYP	
e1	0.350	0.450	0.014	0.018
L	0.250	0.350	0.010	0.014

Tape and Reel Specification



Symbol	W	A0	B0	K0	E	F	P	P0	P2	T
Dimensions (mm)	8.00+0.3 -0.1	1.23±0.05	2.7±0.05	0.7±0.05	1.75±0.1	3.5±0.05	4.0±0.1	4.0±0.1	2.0±0.05	0.25±0.02

Marking Codes



Ordering Information

Part Number	Working Voltage	Quantity Per Reel	Reel Size
TT0506STX	5V	3,000	7 Inch

Note:

(1) "T506ST" is part number, fixed.