Features

- Transient protection for high-speed data lines
  IEC61000 -4-2 (ESD) ±30kV (Air)
  ±30kV (Contact)
  IEC 61000-4-5 (Lightning) 4.0A (8/20μs)
- Cable Discharge Event (CDE)
- Array of surge rated diodes with internal TVS diode
- Small package saves board space
- Protects four I/O lines
- Low capacitance: 0.3pF@0V(Typical)(I/O-I/O)
  0.6pF@0V(Typical)(I/O-GND)
- Low leakage current: 0.1μA @ VRWM (Typical)
- Low clamping voltage
- Each I/O pin can withstand over 1000 ESD strikes for ±8kV contact discharge

Applications

- HDMI 1.4/2.0, USB 3.0/3.1, MDDI, SATA ports
- Monitors and flat panel displays
- Set-top box
- Video graphics cards
- Digital Video Interface (DVI)
- Notebook computers

Mechanical Characteristics

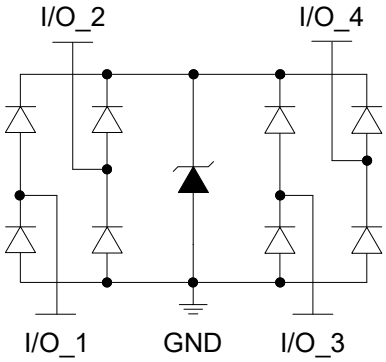
- Package: DFN2510-10L
- Marking: Part number
- Packaging: Tape and Reel
- ROHS compliant

Description

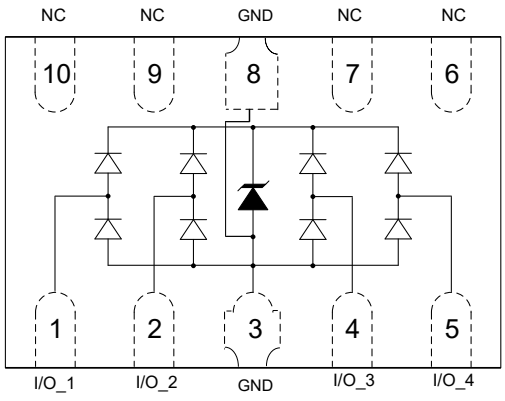
TT0514TPX is an ultra-low capacitance Transient Voltage Suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With typical capacitance of 0.6pF only, is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC61000-4-2 (ESD), Level 4 (±15kV air, ±8kV contact discharge), IEC61000-4-4 (electrical fast transient-EFT) (40A, 5/50ns), very fast charged device model (CDM) ESD and cable discharge event (CDE), etc.

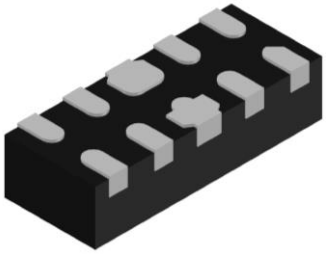
The TT0514TPX comes in a RoHS compliant and Halogen Free 2.5mm x 1.0mm x 0.55mm DFN2510-10L package. This device incorporates eight surge rated, ultra-low capacitance steering diodes and a TVS in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground.

Circuit Diagram



Pin Configuration





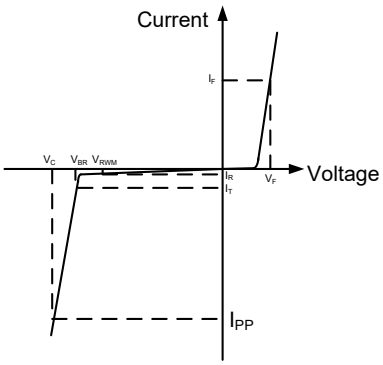
DFN2510-10L
(Bottom View)

DFN2510-10L
(Top View)

Absolute Maximum Rating

Symbol	Parameter	Value	Units
I_{PP}	Peak Pulse Current (8/20μs)	4	A
P_{PK}	Peak Pulse Power (8/20μs)	40	W
V_{ESD}	ESD per IEC61000-4-2 (Air) ESD per IEC61000-4-2 (Contact)	±30 ±30	kV
T_{OPT}	Operating Temperature	-55/+125	°C
T_{STG}	Storage Temperature	-55/+150	°C

Electrical Characteristics (T = 25°C)

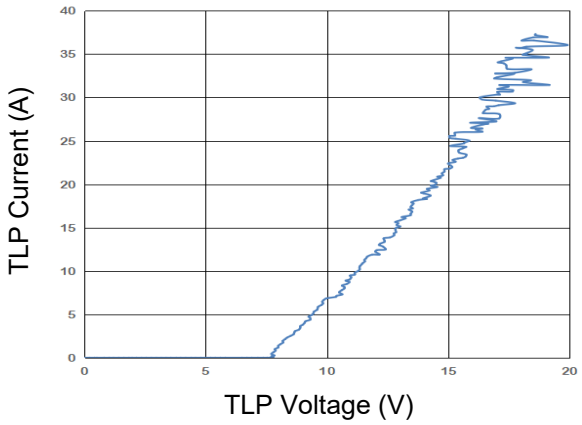
Symbol	Parameter	Diagram
V_{RWM}	Nominal Reverse Working Voltage	
I_R	Reverse Leakage Current @ V_{RWM}	
V_{BR}	Reverse Breakdown Voltage @ I_T	
I_T	Test Current for Reverse Breakdown	
V_C	Clamping Voltage @ I_{PP}	
I_{PP}	Maximum Peak Pulse Current	
C_{ESD}	Parasitic Capacitance	
I_F	Forward Current	
V_F	Forward Voltage @ I_F	

Symbol	Test Condition	Minimum	Typical	Maximum	Units
V_{RWM}				5.0	V
I_R	V_{RWM} = 5V, T = 25°C Between I/O and GND		0.1	1.0	μA
V_{BR}	I_T = 1mA Between I/O and GND	6.0	8.0	10.0	V
VC	I_{PP} = 4A, t_p = 8/20μs Between I/O and GND		10.0		V
V_C	I_{PP} = 8.0A, t_p=100ns(1)		10.7		V
	I_{PP} = 16.0A, t_p=100ns(1)		13.2		V
R_{dyn}	I_{PP} = 12.0A, t_p = 100ns(1)		0.3		Ω
C_{ESD}	V_R = 0V, f = 1MHz Between I/O and GND		0.6		pF
C_{ESD}	V_R = 0V, f = 1MHz Between I/O and I/O		0.3		pF

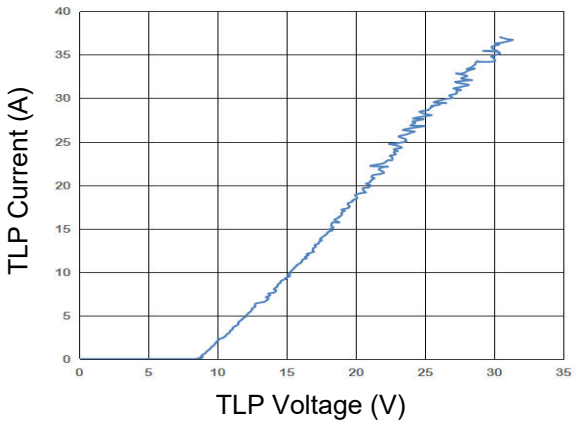
Notes:(1)Measurements performed using a 100ns Transmission Line Pulse(TLP) system,Between I/O and GND.

Typical Performance Characteristics

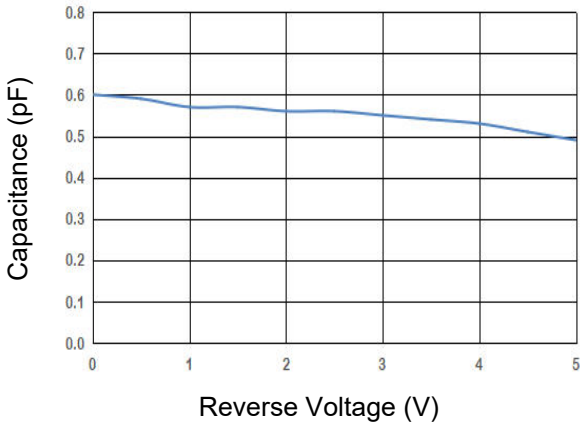
TLP Measurement of I/O to GND



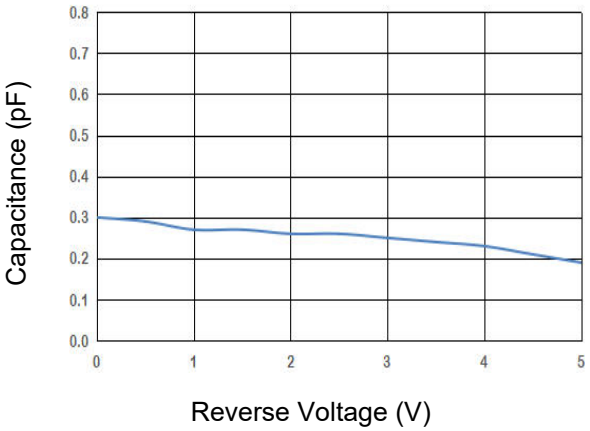
TLP Measurement of I/O to I/O



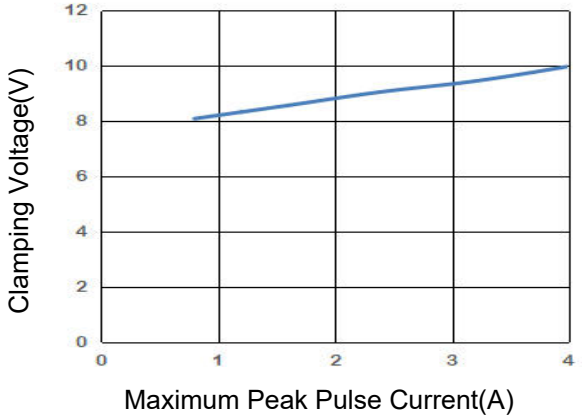
Capacitance vs Reverse Voltage IO to GND



Capacitance vs Reverse Voltage IO to IO

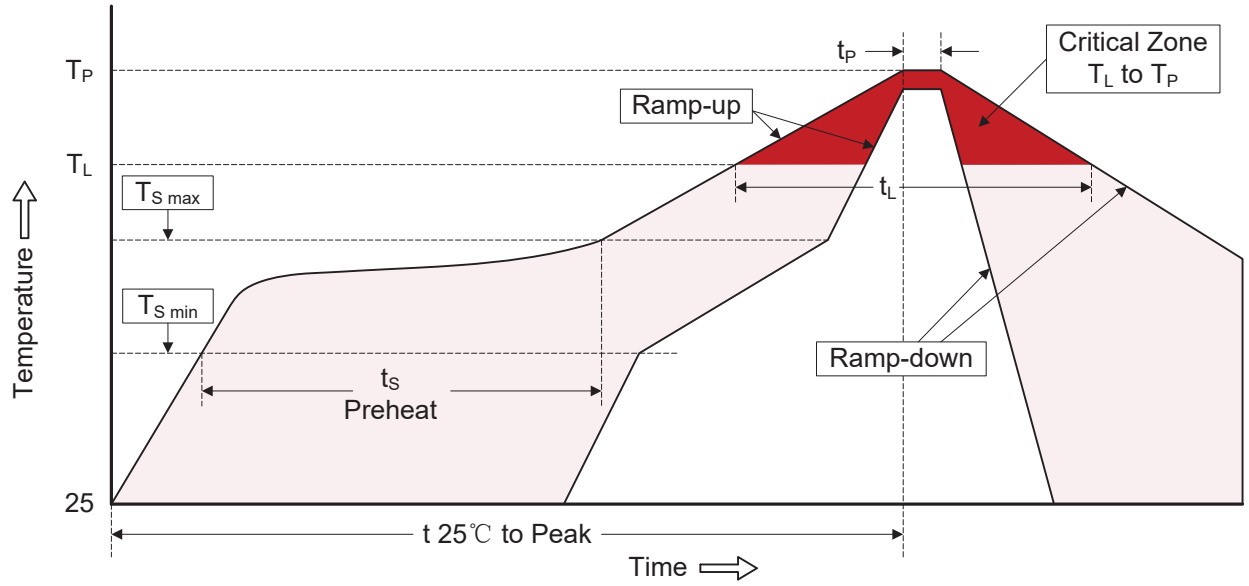


8/20us Current IO to GND



Recommended Soldering Conditions

Reflow Soldering



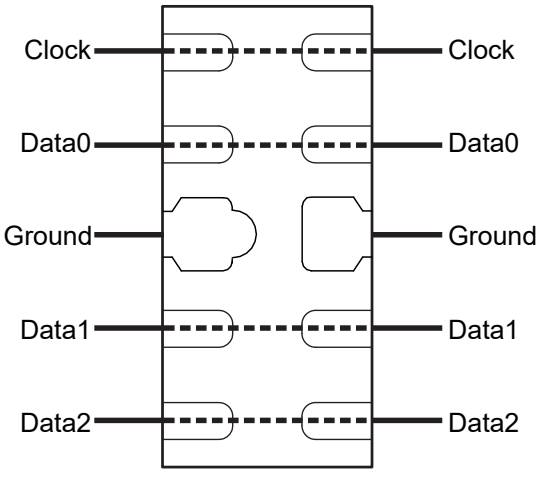
Recommended Conditions

Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3℃/second max.
Preheat -Temperature Min ($T_{S\ min}$) -Temperature Max ($T_{S\ max}$) -Time (min to max) (ts)	 150℃ 200℃ 60-180 seconds
$T_{S\ max}$ to T_L -Ramp-up Rate	 3℃/second max.
Time maintained above: -Temperature (T_L) -Time (t_L)	 217℃ 60-150 seconds
Peak Temperature (T_P)	260℃
Time within 5℃ of actual Peak Temperature (t_P)	20-40 seconds
Ramp-down Rate	6℃/second max.
Time 25℃ to Peak Temperature	8 minutes max.

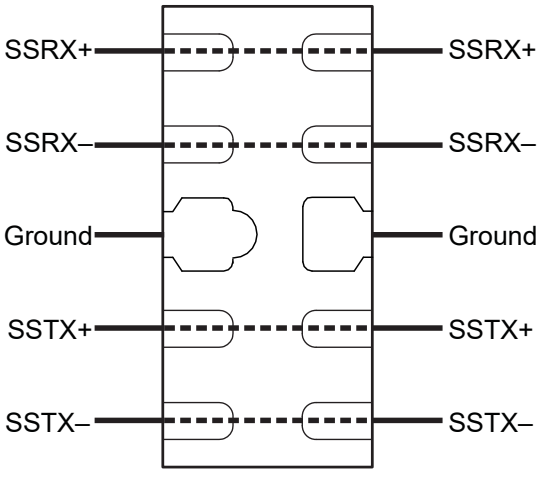
High Speed PCB Layout Guidelines

Printed circuit board layout is the key to achieving the highest level of surge immunity on power and data lines. The location of the protection devices on the PCB is the simplest and most important design rule to follow. The TT0514TPX devices should be located as close as possible to the noise source. The TT0514TPX device should be placed on all data and power lines that enter or exit the PCB at the I/O connector. In most systems, surge pulses occur on data and power lines that enter the PCB through the I/O connector. Placing the TT0514TPX devices as close as possible to the noise source ensures that a surge voltage will be clamped before the pulse can be coupled into adjacent PCB traces. In addition, the PCB should use the shortest possible traces. A short trace length equates to low impedance, which ensures that the surge energy will be dissipated by the TT0514TPX device. Long signal traces will act as antennas to receive energy from fields that are produced by the ESD pulse. By keeping line lengths as short as possible, the efficiency of the line to act as an antenna for ESD related fields is reduced. Minimize interconnecting line lengths by placing devices with the most interconnect as close together as possible. The protection circuits should shunt the surge voltage to either the reference or chassis ground. Shunting the surge voltage directly to the IC's signal ground can cause ground bounce. The clamping performance of TVS diodes on a single ground PCB can be improved by minimizing the impedance with relatively short and wide ground traces. The PCB layout and IC package parasitic inductances can cause significant overshoot to the TVS's clamping voltage. The inductance of the PCB can be reduced by using short trace lengths and multiple layers with separate ground and power planes. One effective method to minimize loop problems is to incorporate a ground plane in the PCB design.

The TT0514TPX ultra-low capacitance TVS is designed to protect four high speed data transmission lines from transient over-voltages by clamping them to a fixed reference. The low inductance and construction minimizes voltage overshoot during high current surges. When the voltage on the protected line exceeds the reference voltage the internal steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. The TT0514TPX is designed for ease of PCB layout by allowing the traces to run underneath the device. The pinout of the TT0514TPX is designed to simply drop onto the IO lines of a High Definition Multimedia Interface (HDMI 1.4/2.0) or USB 3.0/3.1 design without having to divert the signal lines that may add more parasitic inductance. Pins 1, 2, 4 and 5 are connected to the internal TVS devices and pins 6, 7, 9 and 10 are no connects. The no connects was done so the package can be securely soldered onto the PCB surface.

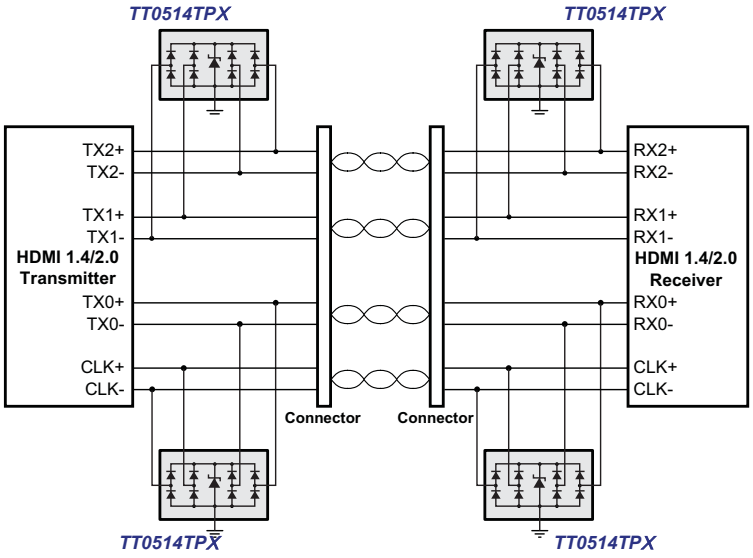


Flow Through Layout for HDMI 1.4/2.0

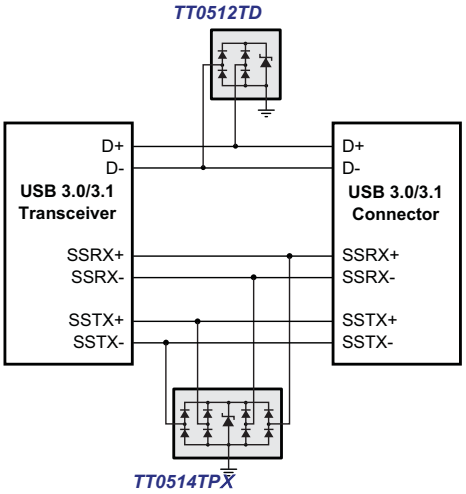


Flow Through Layout for USB 3.0/3.1

Application Information

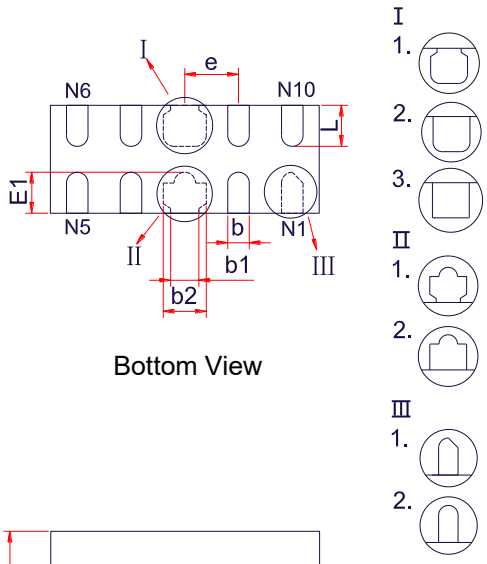


HDMI 1.4/2.0 Ports

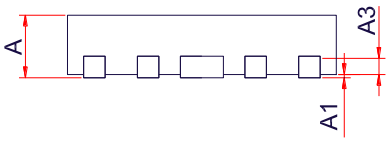


USB 3.0/3.1 Ports

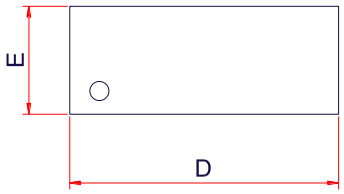
Package Outline, DFN2510-10L



Bottom View

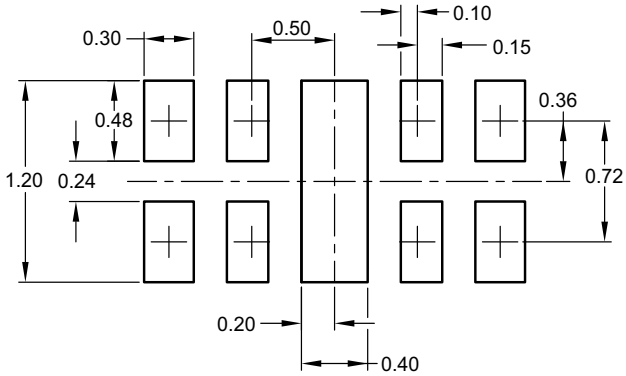


Side View



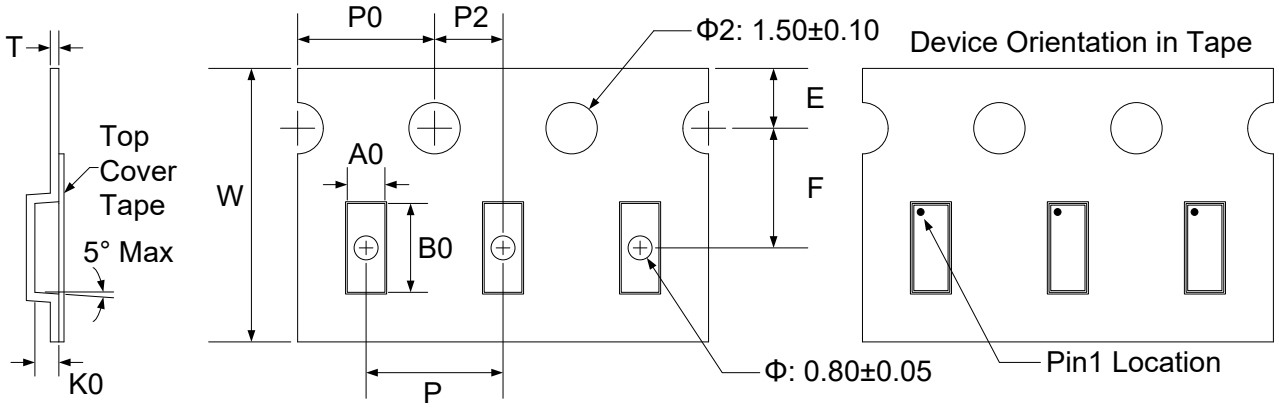
Top View

RECOMMENDED LAND PATTERN



Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.45	0.52	0.60
A1	0.00	0.02	0.05
A3		0.15Ref	
D	2.40	2.50	2.60
E	0.90	1.00	1.10
E1		0.50Ref	
b	0.15	0.20	0.25
b1	0.13	0.18	0.23
b2	0.35	0.40	0.45
e		0.50BSC	
L	0.28	0.39	0.50

Tape and Reel Specification



Symbol	W	A0	B0	K0	E	F	P	P0	P2	T
Dimensions (mm)	8.00+0.3 -0.1	1.23±0.05	2.7±0.05	0.7±0.05	1.75±0.1	3.5±0.05	4.0±0.1	4.0±0.1	2.0±0.05	0.25±0.02

Marking Codes

Note:

(1) "1" is part number, fixed.

(2) "XXXX" is the identification number.

Ordering Information

Part Number	Working Voltage	Quantity Per Reel	Reel Size
TT0514TPX	5V	3,000	7 Inch