SY81020

High Efficiency, 16V/20A Synchronous Step Down Regulator

General Description

The SY81020 is a high-efficiency synchronous step-down DC-DC regulator featuring internal power and synchronous rectifier switches capable of delivering 20A of continuous output current over a wide input voltage range, from as low as 2.9V up to 16V. The output voltage is adjustable from 0.6V to 5.5V.

Silergy's proprietary Instant-PWM™ fast-response, constant-on-time (COT) PWM control method supports high input/output voltage ratios (low duty cycles) and responds to load transients within ~100ns while maintaining a near-constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation, even with low ESR ceramic output capacitors.

The stable internal reference (V_{REF}) provides ±1% accuracy over T_J= -40°C to 125°C, and the differential input sense configuration allows the feedback sensing at the most relevant load point.

Internal 7.5mΩ power and 2.4mΩ synchronous rectifier switches provide excellent efficiency for a wide range of applications, especially for low output voltages and low duty cycles. Cycle-by-cycle current limit, input under-voltage lock-out, internal soft-start, output under- and over-voltage protection, and thermal shutdown provide safe operation in all operating conditions.

The SY81020 is available in a compact QFN3x4 package.

Ordering Information

SY81020 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY81020VDC	QFN3×4-19	

Features

- Wide Input Voltage Range:
  - 2.9V to 16V if VCC is Supplied by External Source
  - 3.6V to 16V if VCC is Supplied by VIN
- Internal 7.5mΩ Power Switch and 2.4mΩ Synchronous Rectifier
- Accurate Feedback Set Point: 0.6V ±1%
- Differential Remote Sense
- Fast Transient Response
- 600kHz, 800kHz and 1000kHz Operating Frequency
- Selectable Automatic High-efficiency Discontinuous Operating Mode at Light Loads
- Programmable Valley Current Limit
- Reliable Built-in Protections:
  - Automatic Recovery for Input Under-voltage (UVLO), Output Under-voltage (UVP) and Over-temperature (OTP) Conditions
  - Cycle-by-cycle Valley and Peak Current Limit (OCP)
  - Cycle-by-cycle Reverse Current Limit
- Internal and Adjustable Soft-start to Limits Inrush Current
- Smooth Pre-biased Startup
- Power Good Output Monitor for Under-voltage and Over-voltage

Applications

- Telecom and Networking Systems
- Servers
- High Power Access Points
- Storage Systems
- Cellular Base Stations

Typical Application

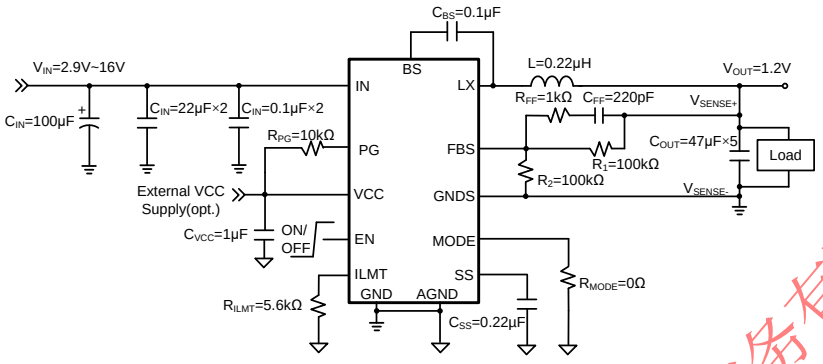


Figure1. Typical Application Circuit

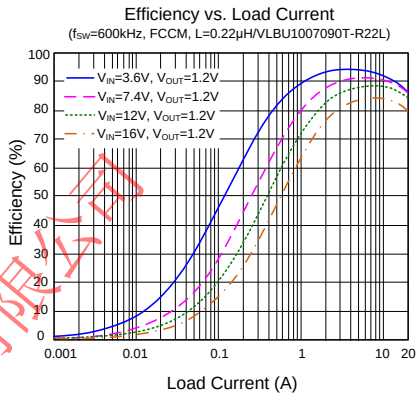
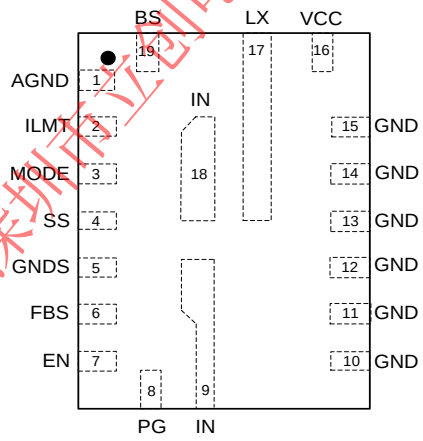


Figure2. Efficiency vs. Load Current

Pinout (top view)



(QFN3×4-19)

Top Mark: DBA*xyz* (Device code: DBA, ***x=year code, y=week code, z= lot number code***)

Pin No	Pin Name	Pin Description
1	AGND	Analog ground.
2	ILMT	Bottom MOSFET current limit set pin. Connect a resistor to AGND to set the inductor valley current limit value.
3	MODE	Operation mode selection. Program MODE to select FCCM/PFM, and the operating switching frequency.
4	SS	External soft-start Voltage pin. Soft-start time can be adjusted by adding an appropriate external capacitor between this pin and AGND pin. IC actual soft-start time is determined by the slower ramp between internal SS voltage and external SS voltage.
5	GNDS	Remote sense negative input. Connect this pin directly to the negative side of the voltage sense point. Short to GND if remote sense is not used.
6	FBS	Remote sense positive input. Connect to the center point of resistor divider.
7	EN	Enable pin. Pull low to disable the device and pull high to enable the device. Can be used to set the input voltage on and off threshold (adjust UVLO) by using two additional resistors. Do not leave this pin floating.

8	PG	Power good Indicator. Open drain output when the output voltage is within 92.5% to 120% of regulation point.
9, 18	IN	Input pin. Decouple this pin to GND pin with at least a 30µF ceramic capacitor.
10, 11, 12, 13, 14, 15	GND	Power GND.
16	VCC	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuits. Decouple this pin to GND with at least a 1µF ceramic capacitor. Make one good Kelvin connection from AGND to VCC capacitor GND connection. Use short, direct connections and avoid the use of vias. May be driven by an external bias supply. See Detailed Description.
17	LX	Inductor pin. Connect this pin to the switching node of inductor.
19	BS	Boot-strap pin. Supply high side gate driver. Connect a 0.1µF ceramic capacitor between the BS and the LX pin.

Block Diagram

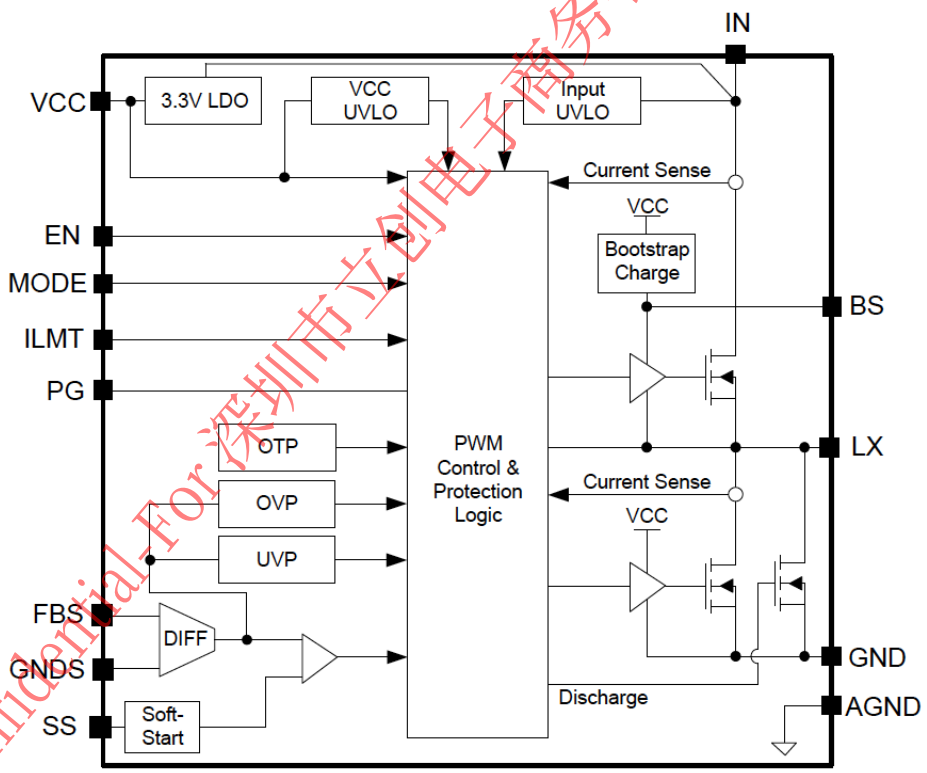


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 18V
ILMT, SS ---------- -0.3V to 4V
EN, MODE, LX Voltage---------- -0.3V to V_{IN}+0.3V
Dynamic LX Voltage in 25ns Duration ---------- GND-5V to V_{IN}+5V
BS ---------- V_{LX}-0.3V to V_{LX}+4V
FBS, GNDS, AGND, VCC, PG Voltage ---------- -0.3V to 4V
Maximum Power Dissipation, $P_{D, MAX}$ @ T_A=25°C, QFN3×4-19 ---------- 4.2W
Package Thermal Resistance (Note2)
θ_{JA} ---------- 24°C/W
θ_{JC} ---------- 4.5°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.9V to 16V
Output Voltage ---------- 0.6V to 5.5V
VCC Bias External Voltage ---------- 3.12V to 3.6V
EN Supply Voltage ---------- 0V to V_{IN}
Maximum Output Current ---------- 20A
Maximum Output Current Limit ---------- 24A
Maximum Inductor Peak Current ---------- 28A
Junction Temperature Range ---------- -40°C to 125°C

Electrical Characteristics

(V_{IN} = 12V, T_J = -40°C to +125°C. Typical values are at T_J = 25°C, unless otherwise specified. The values are guaranteed by test, design or statistical correlation)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.9		16	V
Output Voltage Range	V_{OUT}		0.6		5.5	V
Input UVLO Rising Threshold	$V_{IN,UVLO}$		2.6	2.75	2.9	V
Input UVLO Hysteresis	$V_{IN,HYS}$			200		mV
VCC UVLO Rising Threshold	$V_{VCC,UVLO}$				2.5	V
VCC UVLO Hysteresis	$V_{VCC,HYS}$			100		mV
VCC Regulator Output Voltage	V_{CC}	I_{VCC}=0mA	3.15	3.3	3.45	V
VCC Load Regulation	$V_{CC,REG}$	I_{VCC}=25mA		1.4		%V_{CC}
Quiescent Current	I_Q	V_{EN}=2V, V_{FBS} = 0.65V, PFM mode, No Switching		550	850	μA
Shutdown Current	I_{SHDN}	V_{EN}=0V, T_J=25°C		2	5	μA
Feedback Reference Voltage	V_{REF}	-40°C <T_J< 125°C	0.594	0.600	0.606	V
Error Amplifier Offset	V_{OS}	(Note 4)	-3		3	mV
FBS Input Current	I_{FBS}	V_{EN}=2V, V_{FBS} = 1V	-50	0	50	nA
SS Charging Current	I_{SS1}	V_{SS}=0V		46		μA
SS Pull Down Current	I_{SS2}	V_{SS}=1V		38		mA
Minimum Soft-Start Time	$t_{SS,MIN}$	C_{SS}=1nF (Note 4)		1		ms
Top FET $R_{DS(ON)}$	$R_{DS(ON)1}$	V_{BS-LX} = 3.3V, T_J=25°C		7.5	11.3	mΩ
Bottom FET $R_{DS(ON)}$	$R_{DS(ON)2}$	V_{CC} = 3.3V, T_J=25°C		2.4	3.6	mΩ
Top FET Leakage	$I_{TOP, LKG}$	V_{EN}=0V, V_{DS}=12V		0.01	8	μA
Bottom FET Leakage	$I_{BOT, LKG}$	V_{EN}=0V, V_{DS}=12V		0.04	32	μA
EN Rising Threshold	$V_{EN,R}$		1.18	1.23	1.28	V
EN Threshold Hysteresis	$V_{EN,HYS}$			0.2		V
EN Input Current	I_{EN}	V_{EN}=2V		0		μA
Discharge FET Resistance	R_{DIS}			120		Ω
Top FET Current Limit	$I_{LMT,TOP}$		25.5	28	33	A
Bottom FET Reverse Current Limit	$I_{LMT,RVS}$		9	13	16	A

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reverse Current Limit Blank Time	$t_{RCL,BLK}$	(Note 4)	40	60		ns
ILMT Pin Output Voltage	V_{ILMT}		1.15	1.2	1.25	V
I_{ILMT} to $I_{LMT,BOT}$ Ratio	$I_{ILMT}/I_{LMT,BOT}$	$I_{LMT,BOT}$ >5A	9	10	11	μA/A
Output OVP Threshold	V_{OVP}		110	120	130	$\%V_{REF}$
Output UVP Threshold	V_{UVP}		47	52	57	$\%V_{REF}$
Output UVP Delay	$t_{UVP,DLY}$	(Note 4)		20		μs
UVP/OCP Hiccup ON Time	$t_{HICCUP,ON}$	C_{SS}=1nF (Note 4)		3		ms
UVP/OCP Hiccup OFF Time	$t_{HICCUP,OFF}$	C_{SS}=1nF (Note 4)		12		ms
Power Good Threshold	V_{PG}	V_{FBS} falling, PG high to low	77	81	85	$\%V_{REF}$
		V_{FBS} rising, PG low to high	88.5	92.5	96.5	$\%V_{REF}$
		V_{FBS} rising, PG high to low	110	120	130	$\%V_{REF}$
		V_{FBS} falling, PG low to high	102	106	110	$\%V_{REF}$
Power Good Leakage Current	$I_{PG,LKG}$	PG voltage is 3.3V		3	5	μA
Power Good Delay	$t_{PG,R}$	Low to high (Note 4)		0.8		ms
	$t_{PG,F}$	High to low (Note 4)		20		μs
Power Good Sink Current Capability	$V_{PG,LOW}$	V_{EN} = 2V, V_{FBS} = 0V, I_{PG}=10mA			0.4	V
Power Good Output Low Voltage	$V_{PG,L}$	V_{IN}=0V, Pull PG to 3.3V through 100kΩ Resistor		550	750	mV
		V_{IN}=0V, Pull PG to 3.3V through 10kΩ Resistor		660	850	mV
Min ON Time	$t_{ON,MIN}$	I_{OUT}=3A (Note 4)		60		ns
Min OFF Time	$t_{OFF,MIN}$	I_{OUT}=3A (Note 4)		180		ns
Switching Frequency	f_{SW}	R_{MODE}=0Ω, I_{OUT}=0A, FCCM, V_{OUT}=1V, T_J=25°C	510	600	690	kHz
		R_{MODE}=30.1kΩ, I_{OUT}=0A, FCCM, V_{OUT}=1V, T_J=25°C	690	800	910	kHz
		R_{MODE}=60.4kΩ, I_{OUT}=0A, FCCM, V_{OUT}=1V, T_J=25°C	900	1000	1100	kHz
Thermal Shutdown Temperature	T_{SD}	T_J rising (Note 4)		160		˚C
Thermal Shutdown Hysteresis	T_{HYS}	(Note 4)		30		˚C

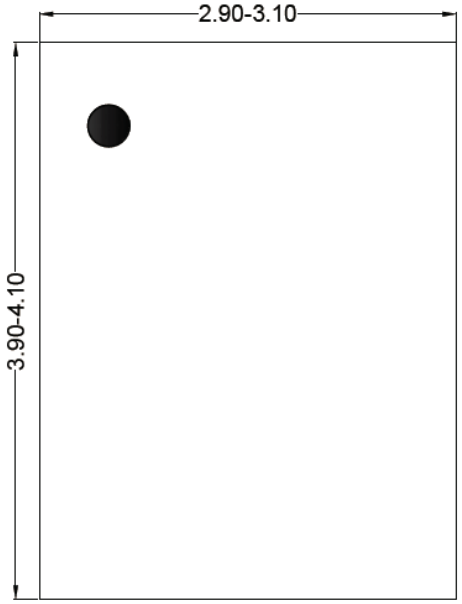
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note2: Package thermal resistance is measured in the natural convection at T_A=25˚C on a 8.5cm×8.5cm size four-layer Silergy Evaluation Board.

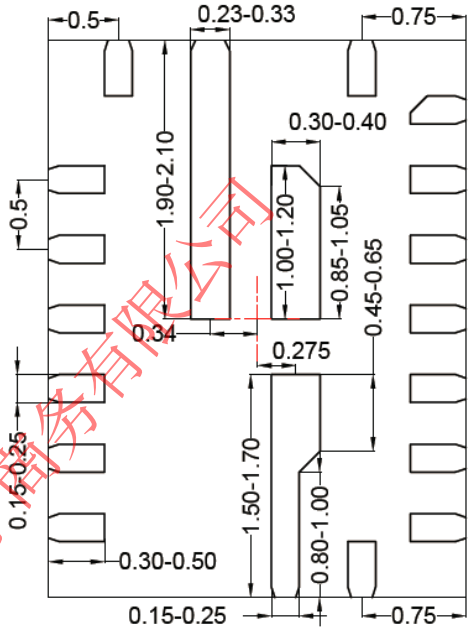
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Guaranteed by design.

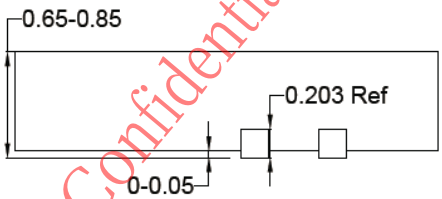
QFN3×4-19 Package Outline Drawing



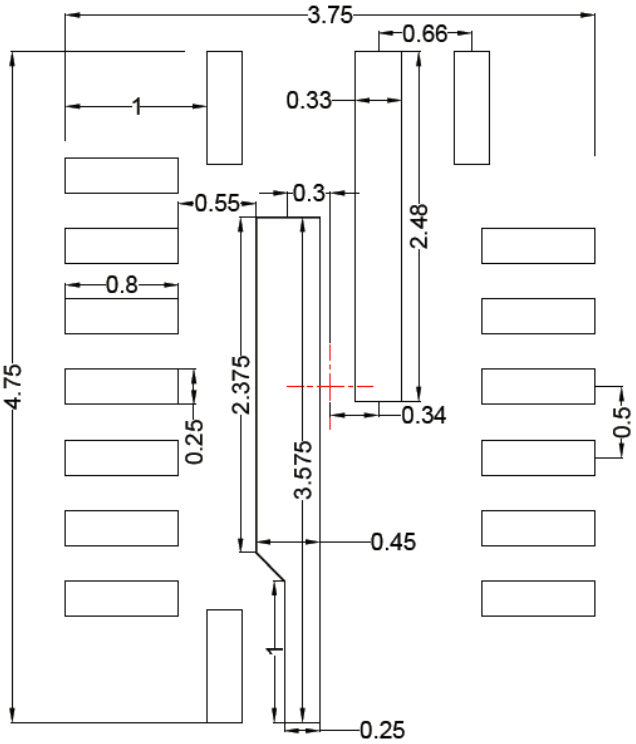
Top view



Bottom view



Front view

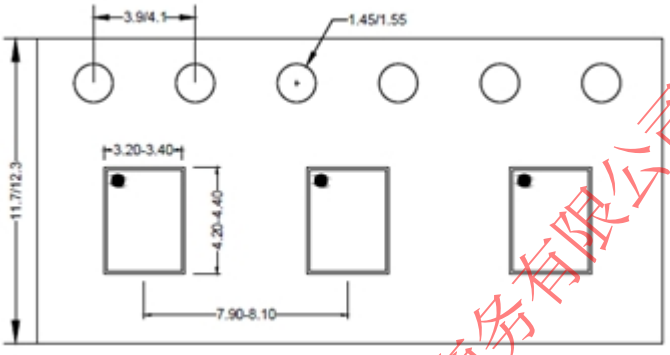


Recommended PCB layout
(Reference only)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr.
2, center line refers chip body center.

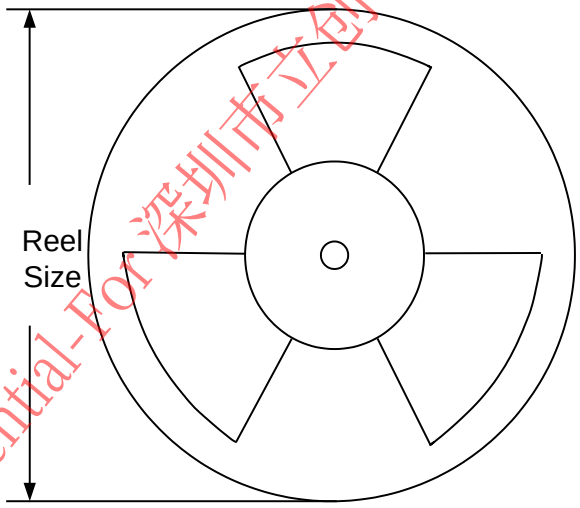
Taping & Reel Specification

1. Taping orientation for packages



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×4	12	8	13"	400	400	5000

3. Others: NA