

SIS903DN-T1-GE3-VB Datasheet

Dual P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
- 30	0.038 at $V_{GS} = - 10$ V	- 6.4
	0.060 at $V_{GS} = - 4.5$ V	- 5

FEATURES

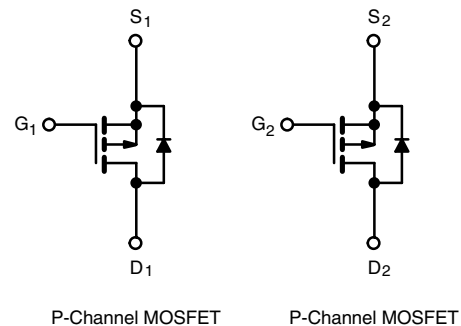
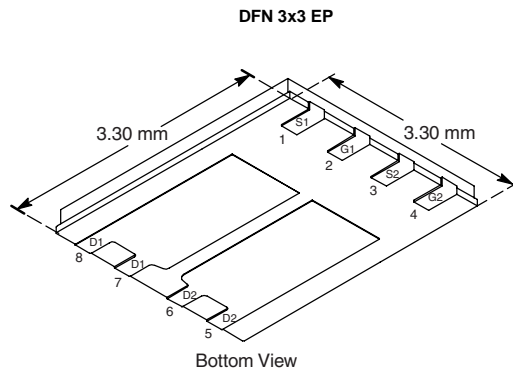
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Portable
- Battery Switch
- Load Switch



ABSOLUTE MAXIMUM RATINGS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Parameter	Symbol	10 s	Steady State	Unit
Drain-Source Voltage	V_{DS}	- 30		V
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 150\text{ }^{\circ}\text{C}$) ^a	I_D	- 6.4	- 4.3	A
		- 4.6	- 3.1	
Pulsed Drain Current	I_{DM}	- 20		
Continuous Source Current (Diode Conduction) ^a	I_S	- 2.3	- 1.1	
Maximum Power Dissipation ^a	P_D	2.8	1.3	W
		1.5	0.85	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		$^{\circ}\text{C}$
Soldering Recommendations (Peak Temperature) ^{b, c}		260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	35	44	$^{\circ}\text{C/W}$
		75	94	
Maximum Junction-to-Case (Drain)	R_{thJC}	4	5	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. The DFN3x3 package is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	-1.0		-3.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\text{ V}$, $V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -30\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^{\circ}\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}$, $V_{GS} = -10\text{ V}$	-20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$, $I_D = -6.4\text{ A}$		0.038		Ω
		$V_{GS} = -4.5\text{ V}$, $I_D = -5\text{ A}$		0.060		
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}$, $I_D = -6.4\text{ A}$		13		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -2.3\text{ A}$, $V_{GS} = 0\text{ V}$		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -15\text{ V}$, $V_{GS} = -10\text{ V}$, $I_D = -6.4\text{ A}$		14	21	nC
Gate-Source Charge	Q_{gs}			2.4		
Gate-Drain Charge	Q_{gd}			3.8		
Gate Resistance	R_g			8.5		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\text{ V}$, $R_L = 15\text{ }\Omega$ $I_D \cong -1\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 6\text{ }\Omega$		10	15	ns
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			38	60	
Fall Time	t_f			28	45	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.3\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		20	40	

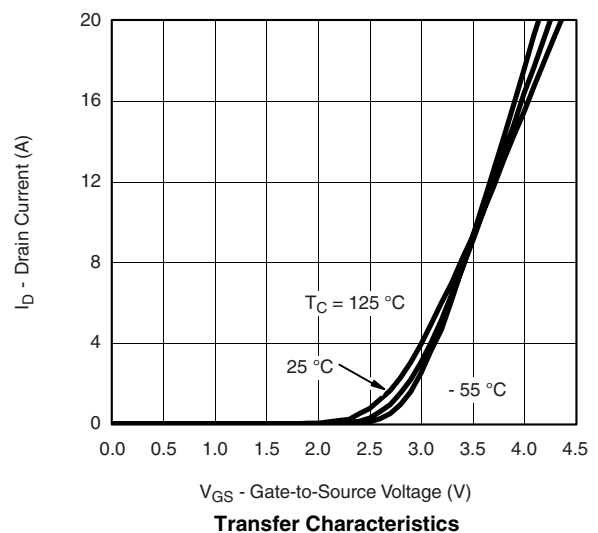
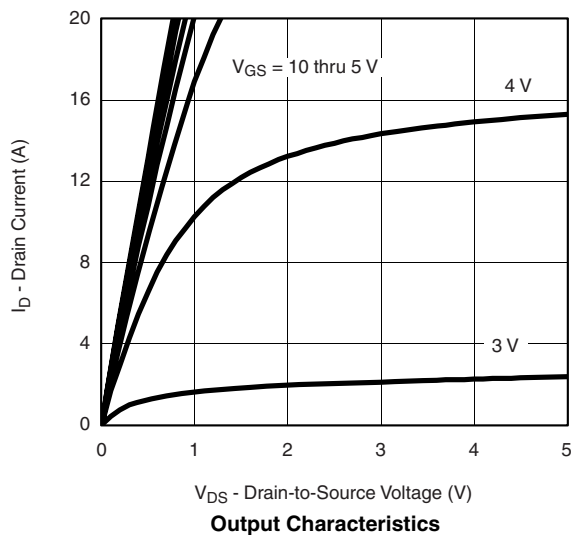
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

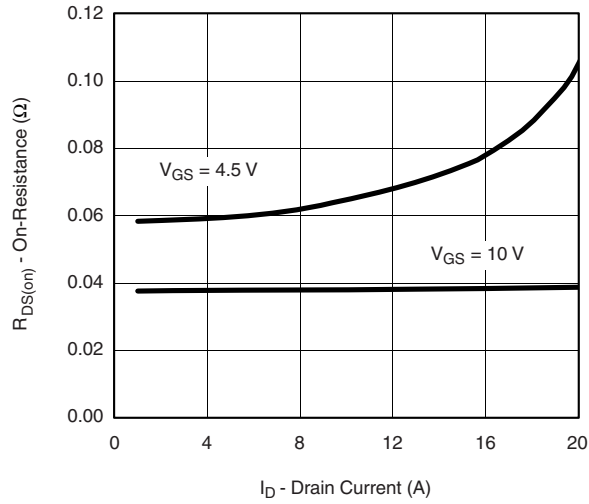
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

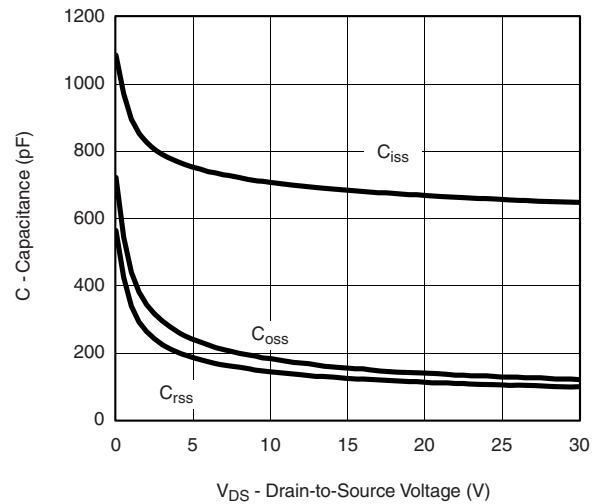
TYPICAL CHARACTERISTICS $25\text{ }^{\circ}\text{C}$, unless otherwise noted



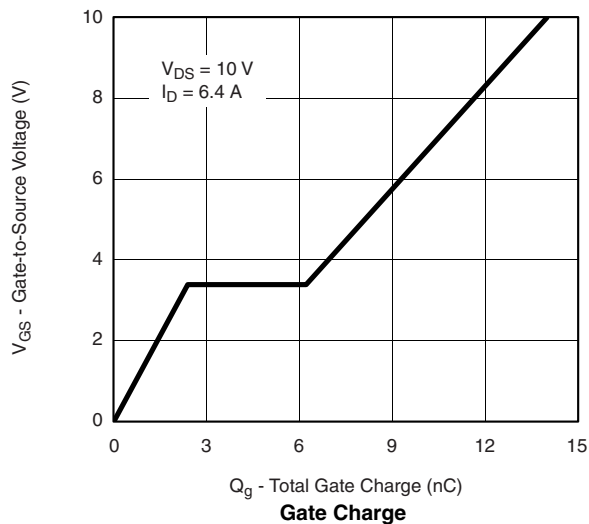
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



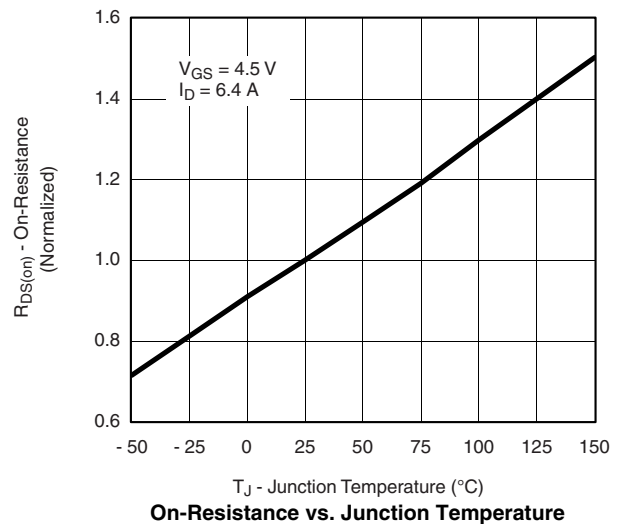
On-Resistance vs. Drain Current



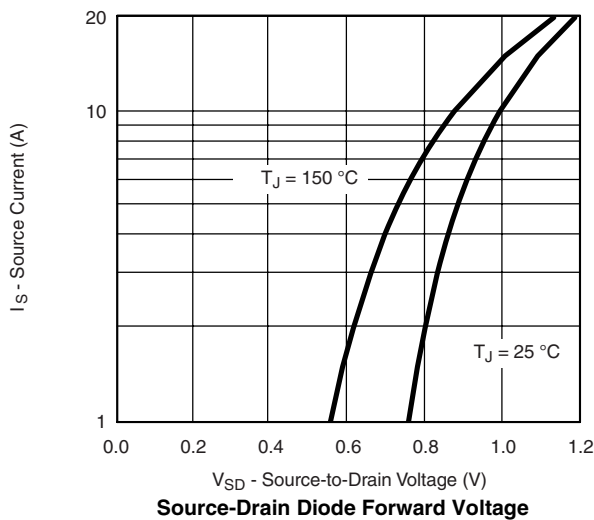
Capacitance



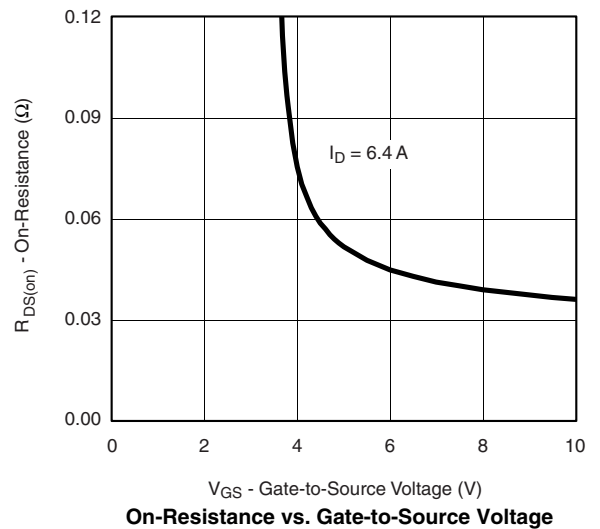
Gate Charge



On-Resistance vs. Junction Temperature

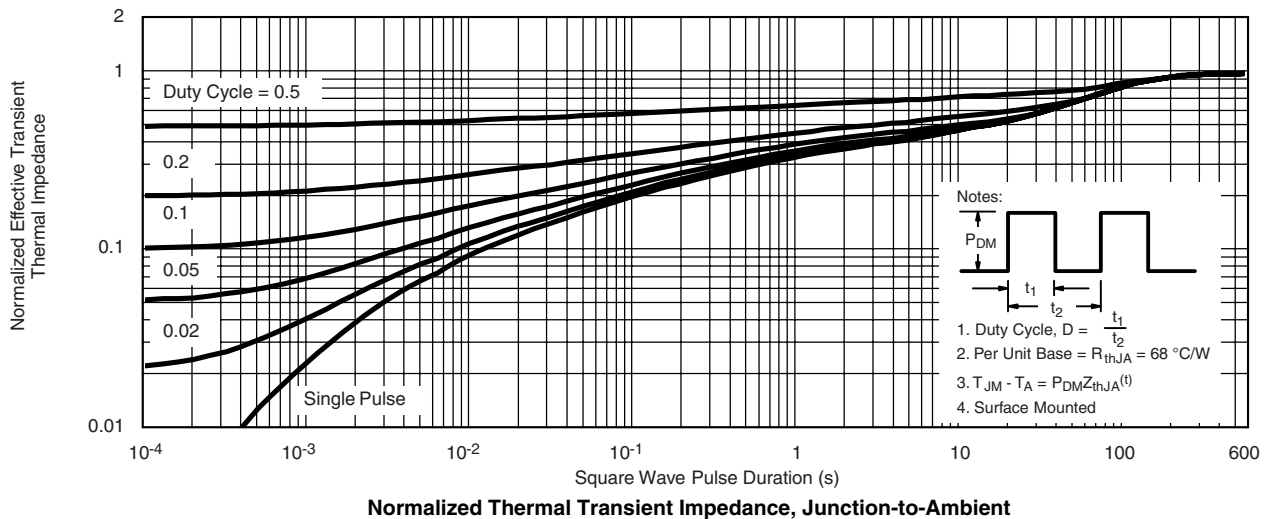
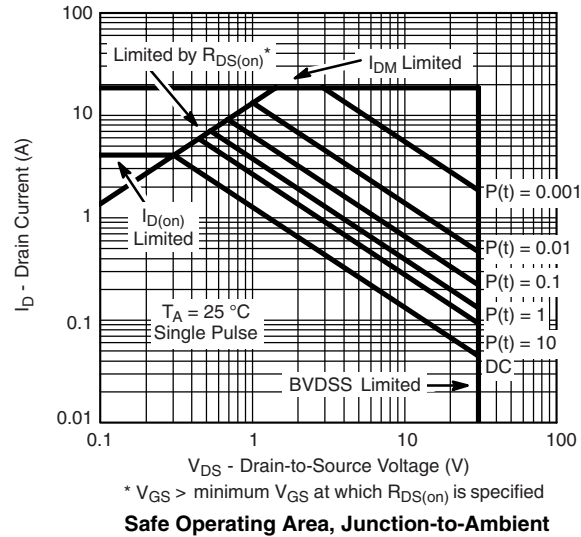
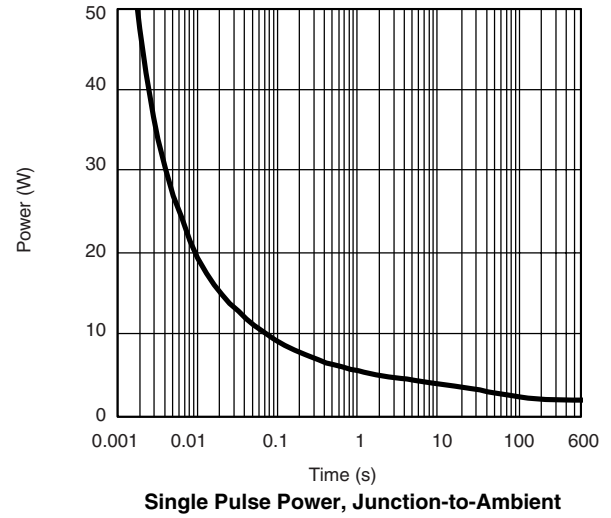
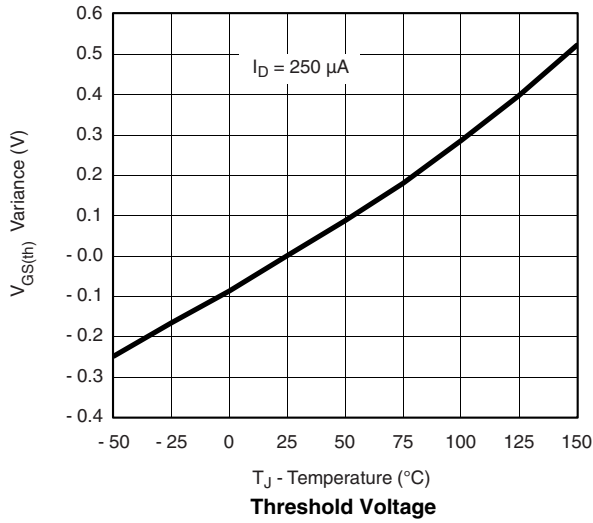


Source-Drain Diode Forward Voltage

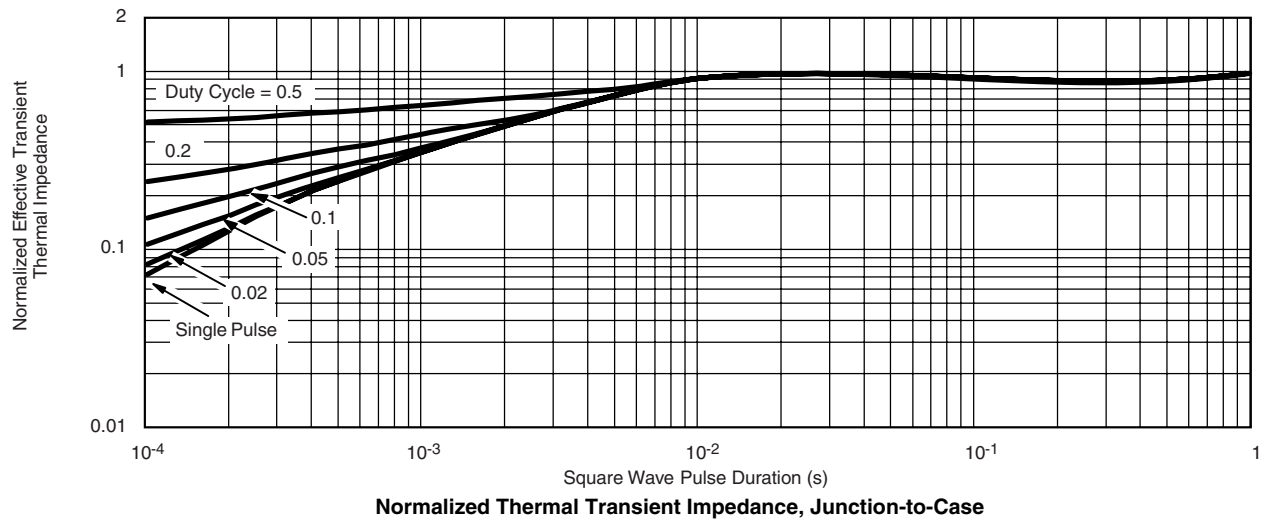


On-Resistance vs. Gate-to-Source Voltage

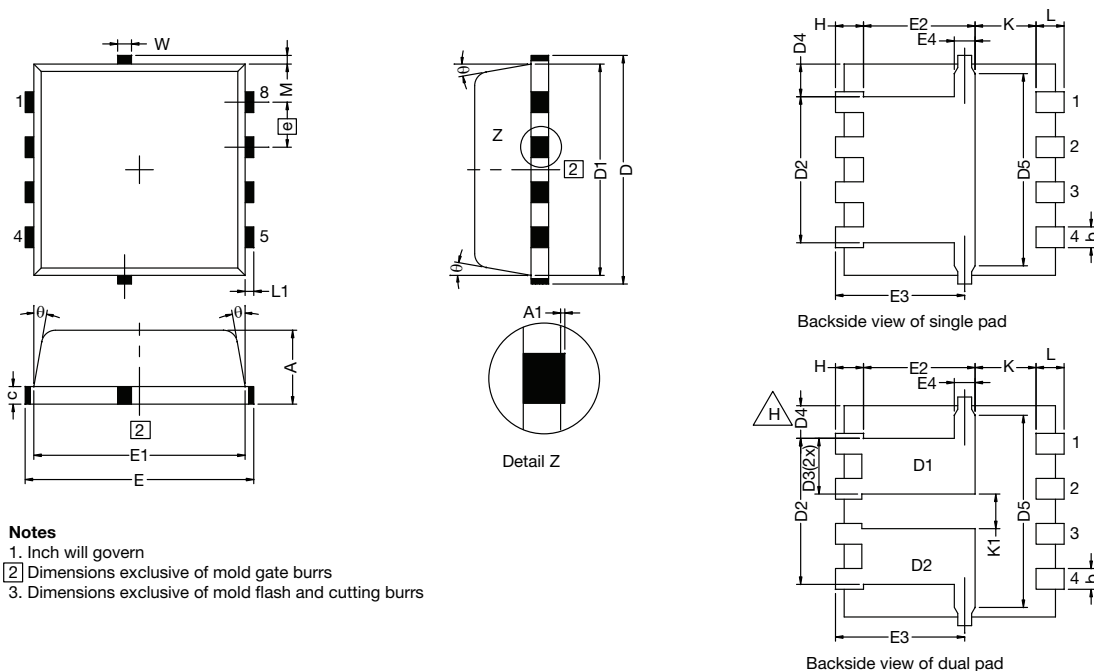
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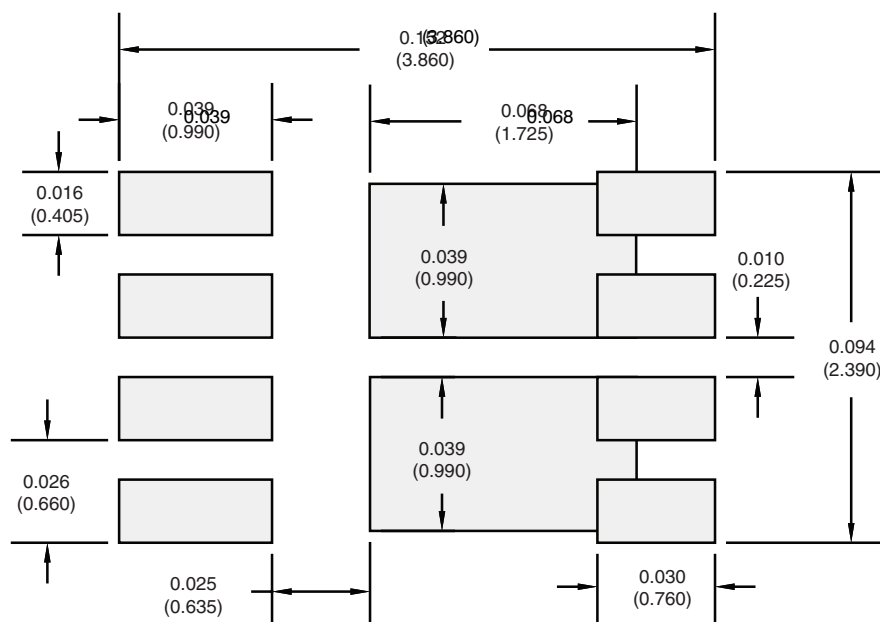


DFN3x3, (Single / Dual)



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0.00	-	0.05	0.000	-	0.002
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D3	0.48	-	0.89	0.019	-	0.035
D4	0.47 typ.			0.0185 typ		
D5	2.3 typ.			0.090 typ		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.034 typ.			0.013 typ.		
e	0.65 BSC			0.026 BSC		
K	0.86 typ.			0.034 typ.		
K1	0.35	-	-	0.014	-	-
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: S16-2667-Rev. M, 09-Jan-17						
DWG: 5882						

RECOMMENDED MINIMUM PADS FOR DFN 3x3 Dual



Recommended Minimum PADS for PowerPAK 1212-8 Dual
Dimensions in Inches/(mm)

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