

Features

- ❑ CMOS Technology
- ❑ Low Power Consumption
- ❑ 8-Step Dimming Circuitry
- ❑ Key Scanning (8 x 2 bit)
- ❑ Display Modes (14 segment, 8 Grid)
- ❑ Serial Interface for Clock, Data Input/Output, Strobe Pins
- ❑ Available in 32-pin, SOP Package

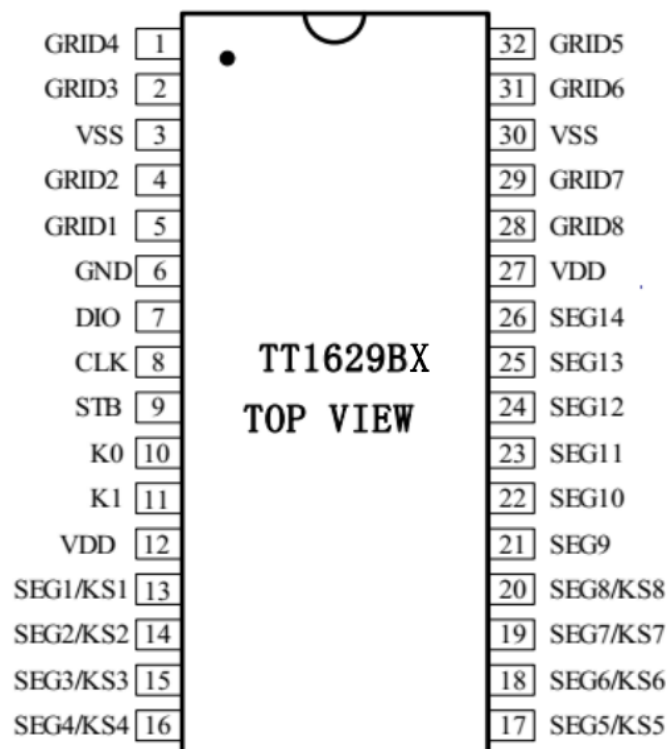
Applications

- ❑ Micro-computer Peripheral Device
- ❑ VCR set
- ❑ Combi set

Description

TT1629BX is an LED Controller driven on a 1/7 to 1/8 duty factor. Fourteen segment output lines, eight grid output lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip microcomputer.

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	Pin Function	Description
DIO	Data Input Output Pin	This pin inputs serial data at the rising edge of the shift clock(starting from the lower bit); This pin outputs serial data at the falling edge of the shift clock (starting from the lower bit).
STB	Serial Interface Strobe Pin	The data input after the STB has fallen is processed as a command. When this pin is "HIGH", CLK is ignored.
CLK	Clock Input Pin	This pin reads serial data at the rising edge and outputs data at the falling edge.
K0~K1	Key Data Input Pins	The data sent to these pins are latched at the end of the display cycle.(Internal Pull-Low Resistor)
SEG1/KS1 ~ SEG8/KS8	Segment Output Pins	Segment Output Pins(P- channel, open drain) Also acts as the Key Source.
SEG9~SEG14	Segment Output pins	Segment Output pins (P-Channel, open drain)
GRID1~GRID8	Grid Output Pins	Grid Output Pins (N-Channel, open drain)
VDD	Power Supply	5V±10%
VSS	Ground Pin	Ground Pin

▲ Note The output data of DIO port is N channel open drain, and the pull up resistance of 1K 10K is needed when reading key data We recommend 10K pull-up resistance DIO controls the action of N MOS at the falling edge of the clock. At this time, the reading is unstable. You can refer to Fig. 1, which is stable at the rising edge of the clock

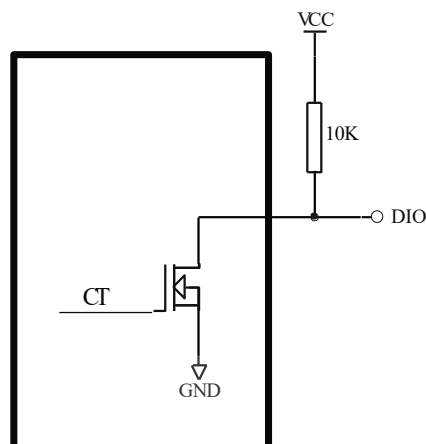


Fig.1

Display Register Address And Display Mode

Data transmitted from an external device to TT1629BX via the serial interface are stored in the Display register. The register addresses of TT1629BX are 16 bytes from 00H-0FH, It corresponds to the LED lamp connected by the SGE and GRID pins respectively. The allocation is as follows:

When writing data for LED display, it operates from low to high position of display address and from low to high position of data byte.

X	X	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1		
		xxHU (high four bits)				xxHL (low four bits)				xxHU (high four bits)				xxHL (low four bits)			
B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0		
GRID1		01HU				01HL				00HU				00HL			
GRID2		03HU				03HL				02HU				02HL			
GRID3		05HU				05HL				04HU				04HL			
GRID4		07HU				07HL				06HU				06HL			
GRID5		09HU				09HL				08HU				08HL			
GRID6		0BHU				0BHL				0AHU				0AHL			
GRID7		0DHU				0DHL				0CHU				0CHL			
GRID8		0FHU				0FHL				0EHU				0EHL			



B0	B1	B2	B3	B4	B5	B6	B7	
X	X	K1	K0	X	X	K1	K0	
KS1				KS2				BYTE1
KS3				KS4				BYTE2
KS5				KS6				BYTE3
KS7				KS8				BYTE4



Address Command Settings

MSB				LSB				Display Address
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	Irrelevant terms, Set 0		0	0	0	0	00H
1	1			0	0	0	1	01H
1	1			0	0	1	0	02H
1	1			0	0	1	1	03H
1	1			0	1	0	0	04H
1	1			0	1	0	1	05H
1	1			0	1	1	0	06H
1	1			0	1	1	1	07H
1	1			1	0	0	0	08H
1	1			1	0	0	1	09H
1	1			1	0	1	0	0AH
1	1			1	0	1	1	0BH
1	1			1	1	0	0	0CH
1	1			1	1	0	1	0DH
1	1			1	1	1	0	0EH
1	1			1	1	1	1	0FH

This instruction is used to set the address of the display register. If the address is set to 10H or higher, the data is ignored until the effective address is set. When power on, the address is set to 00H by default.

Display Control

MSB				LSB				Function	Explain
B7	B6	B5	B4	B3	B2	B1	B0		
1	0	Irrelevant terms, Set 0			0	0	0	Extinction Number Settings	Set the pulse width to 1/16
1	0				0	0	1		Set the pulse width to 2/16
1	0				0	1	0		Set the pulse width to 4/16
1	0				0	1	1		Set the pulse width to 10/16
1	0				1	0	0		Set the pulse width to 11/16
1	0				1	0	1		Set the pulse width to 12/16
1	0				1	1	0		Set the pulse width to 13/16
1	0				1	1	1		Set the pulse width to 14/16
1	0			0				Display Switch Settings	Display closed
1	0			1					Display open

Serial Data Transfer Format

Reading and receiving a BIT are performed at the rising edge of the clock.

Data Receiving (Writing)

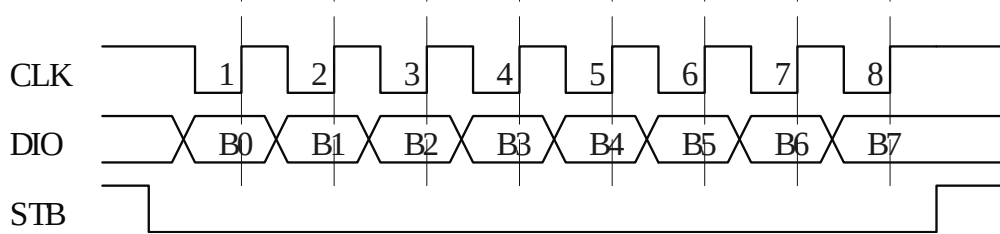


Fig.5

Data Reading (Reading)

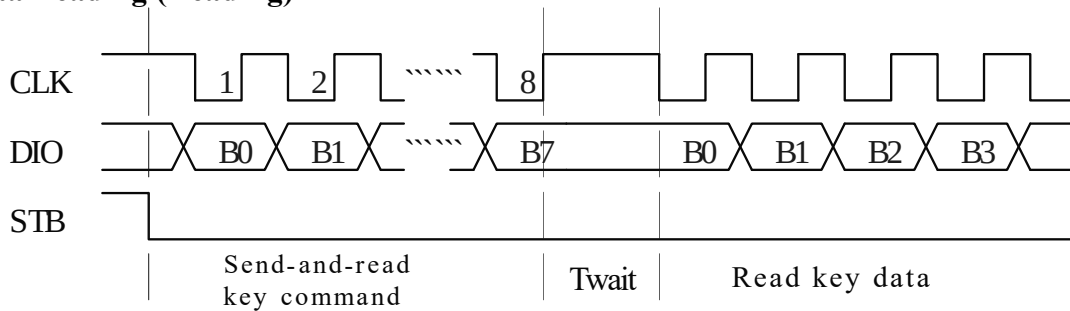


Fig.6

▲**Note:** When reading data, there is a waiting time T_{wait} (minimum 1 μ S) between setting instructions from the 8th rising edge of serial clock CLK to the falling edge of CLK.

Display and Key Scanning

Display

Drive Common Cathode Digital Tube :

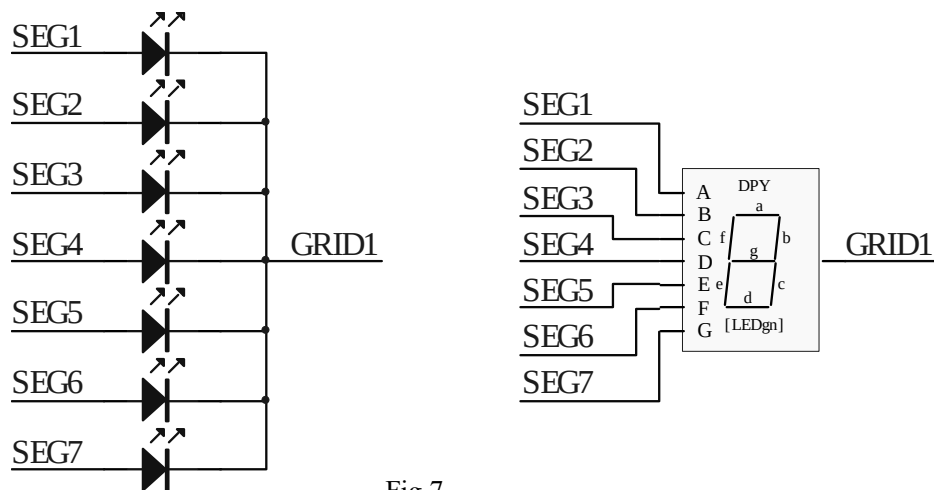


Fig.7

Fig. 7 shows the connection diagram of the common cathode digital tube. If the digital tube displays "0", then you need to make SEG1, SEG2, SEG3, SEG4, SEG5, SEG6 high and SEG7 low when GRID1 is low. Look at the address table in Fig.2. Just write the data 3FH in the 00H address to make the digital tube display "0".

SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	
0	0	1	1	1	1	1	1	00H
B7	B6	B5	B4	B3	B2	B1	B0	

Drive Common Anode Digital Tube :

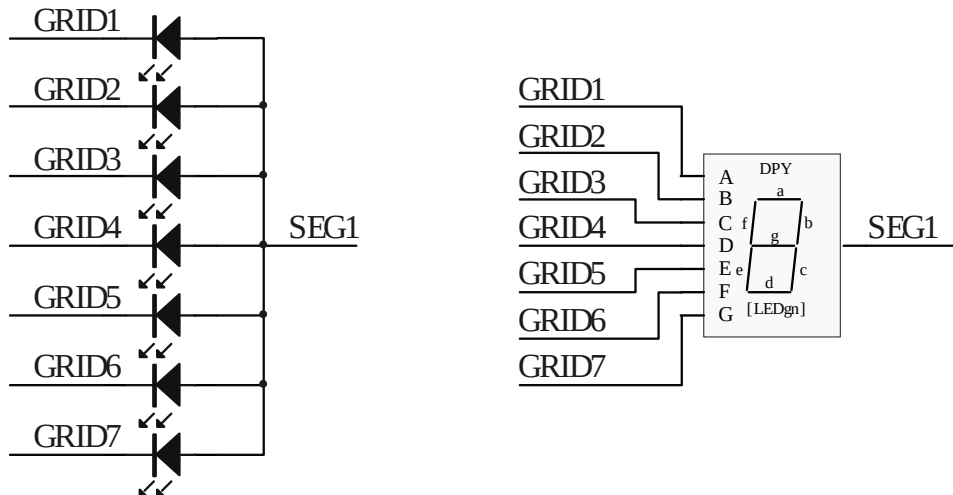


Fig.8

Fig. 8 shows the connection diagram of the common anode digital tube. If the digital tube shows "0", then you need to make SEG1 high when GRID1, GRID2, GRID3, GRID4, GRID5 and GRID6 are low, and SEG1 low when GRID7 is low. Write data 01H to address units 00H, 02H, 04H, 06H, 08H, 0AH, respectively, the rest of the address units all write data 00H.

SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	
0	0	0	0	0	0	0	1	00H
0	0	0	0	0	0	0	1	02H
0	0	0	0	0	0	0	1	04H
0	0	0	0	0	0	0	1	06H
0	0	0	0	0	0	0	1	08H
0	0	0	0	0	0	0	1	0AH
0	0	0	0	0	0	0	0	0CH
B7	B6	B5	B4	B3	B2	B1	B0	

▲ Note: SEG1-14 is the P channel open drain output, GRID 1-8 is the N channel open drain output. When using, SEG1-14 can only connect the anode of LED, GRID can only connect the cathode of LED, no reverse connection.

Keyboard Scanning:

You can observe the output waveforms of SEG1/KS1 and SEG2/KS2 with an oscilloscope according to Fig.9. The output waveforms of SEGn/KSn are shown in Fig.10.

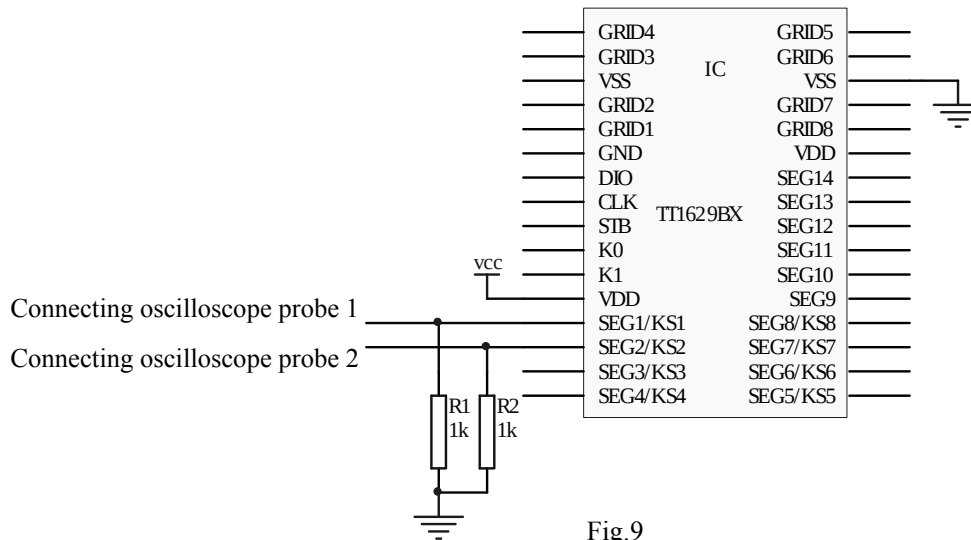


Fig.9

The waveform of SEGN/KSN during keyboard scanning :

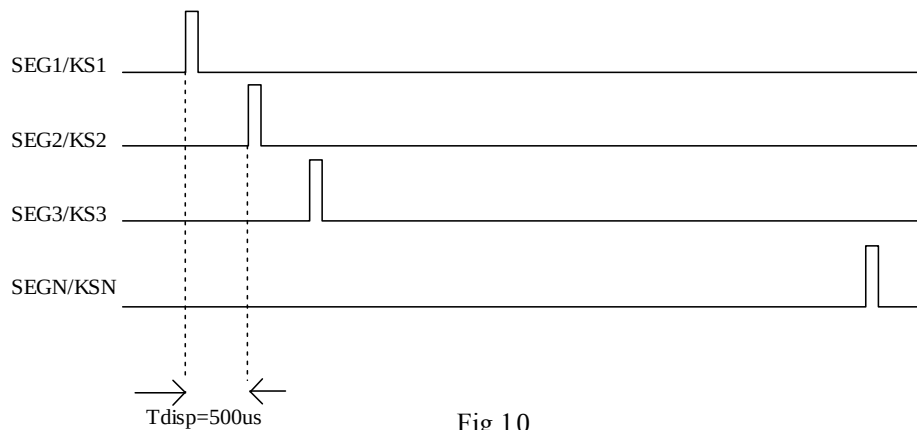


Fig.10

Tdisp is related to the IC's oscillation frequency. Our TT1629BX has been perfected many times and the oscillation frequency is not completely consistent. 500uS is only for reference.

In general, we use Fig.11 to meet the requirements of key design.

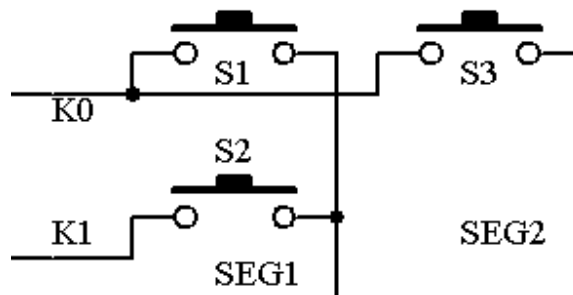


Fig.11

When S1 is pressed, B0 in the first byte reads "1".

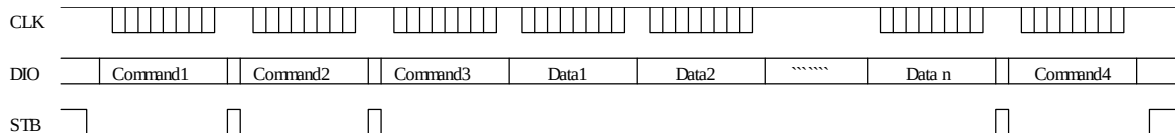
If multiple keys are pressed, multiple "1" will be read.

When S2 and S3 are pressed, the first byte of B1 and B3 reads "1".

Transmission of Serial Data in Application

Address addition mode

Address auto plus 1 mode. Setting the address is actually setting the starting address of the data stream to be stored. After the start address command word is sent, STB does not need to be set high to transmit data, up to 16BYTE. The STB will not be raised until the data transmission is completed.



Command1: Setting Display Mode

Command2: Setting Data Command

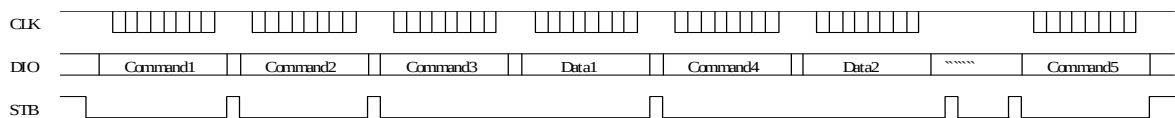
Command3: Setting Display Address

Data1 ~ n: Transfer display data to Command3 address and subsequent address (up to 16 bytes)

Command4: Display Control Command

Fixed Address Mode

Using fixed address mode, setting address is actually setting the address of 1BYTE data storage that needs to be transmitted. After the address is sent, the STB does not need to be set high, and then the 1BYTE data is transmitted. Only after the data is transmitted, the STB is set high. Then reset the address where the second data needs to be stored. Up to 16BYTE data has been transmitted, and STB is set high.



Command1: Setting Display Mode

Command2: Setting Data Command

Command3: Setting Display Address 1

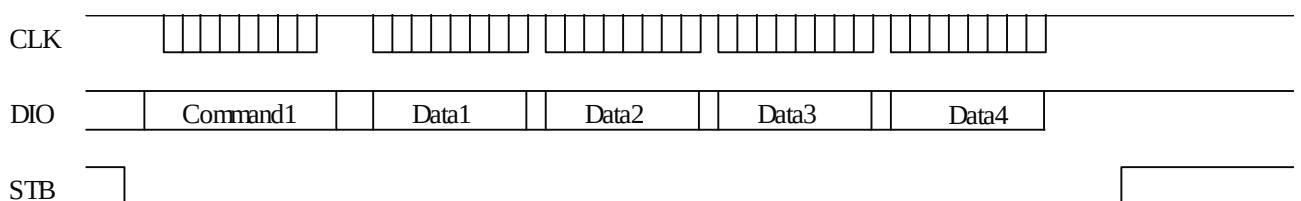
Data1: Transfer Display Data 1 to Command3 Address

Command4: Setting Display Address 2

Data2: Transfer display data 2 to Command4 address

Command5: Display Control Command

Reading Key Timing

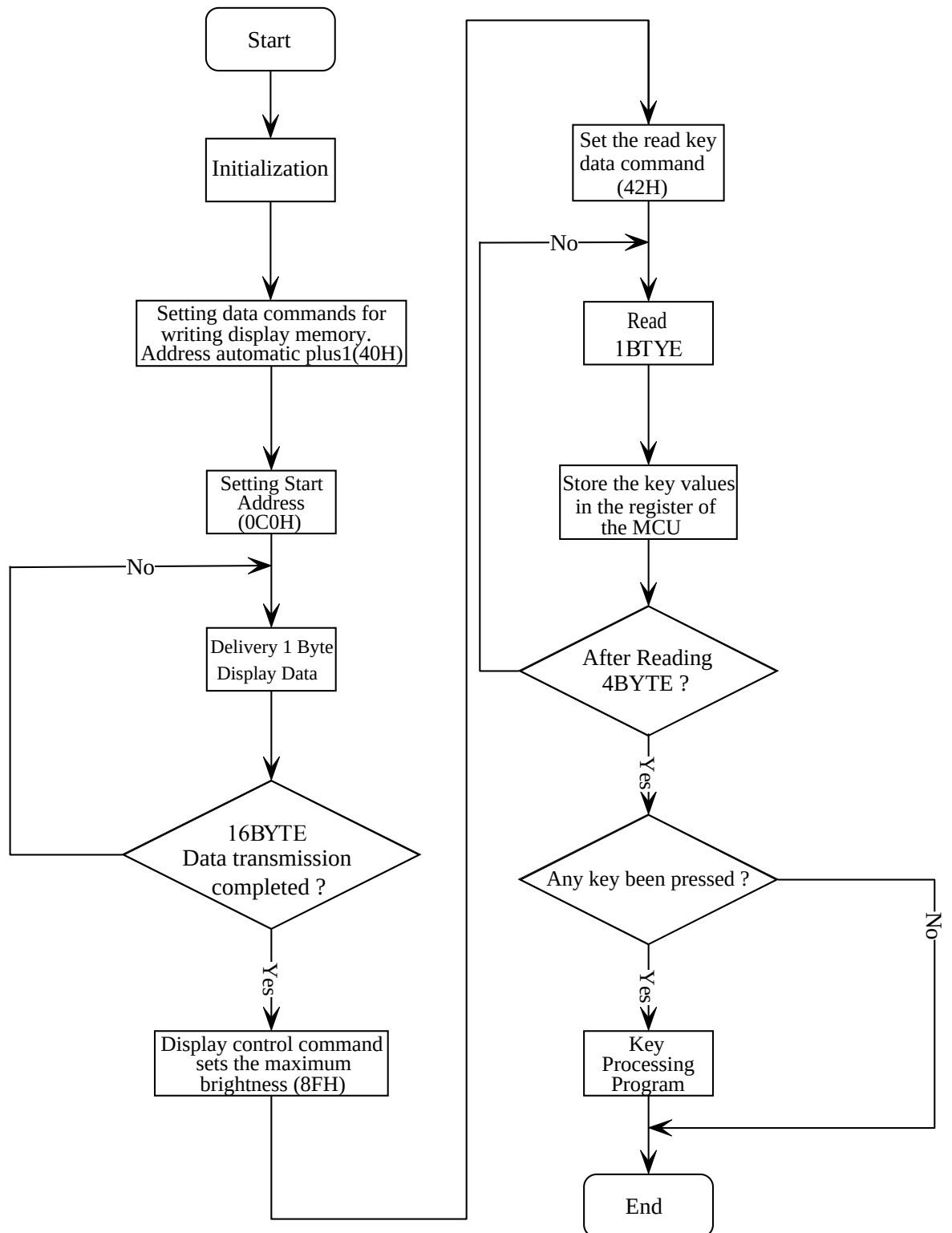


Command1: Setting Display Mode

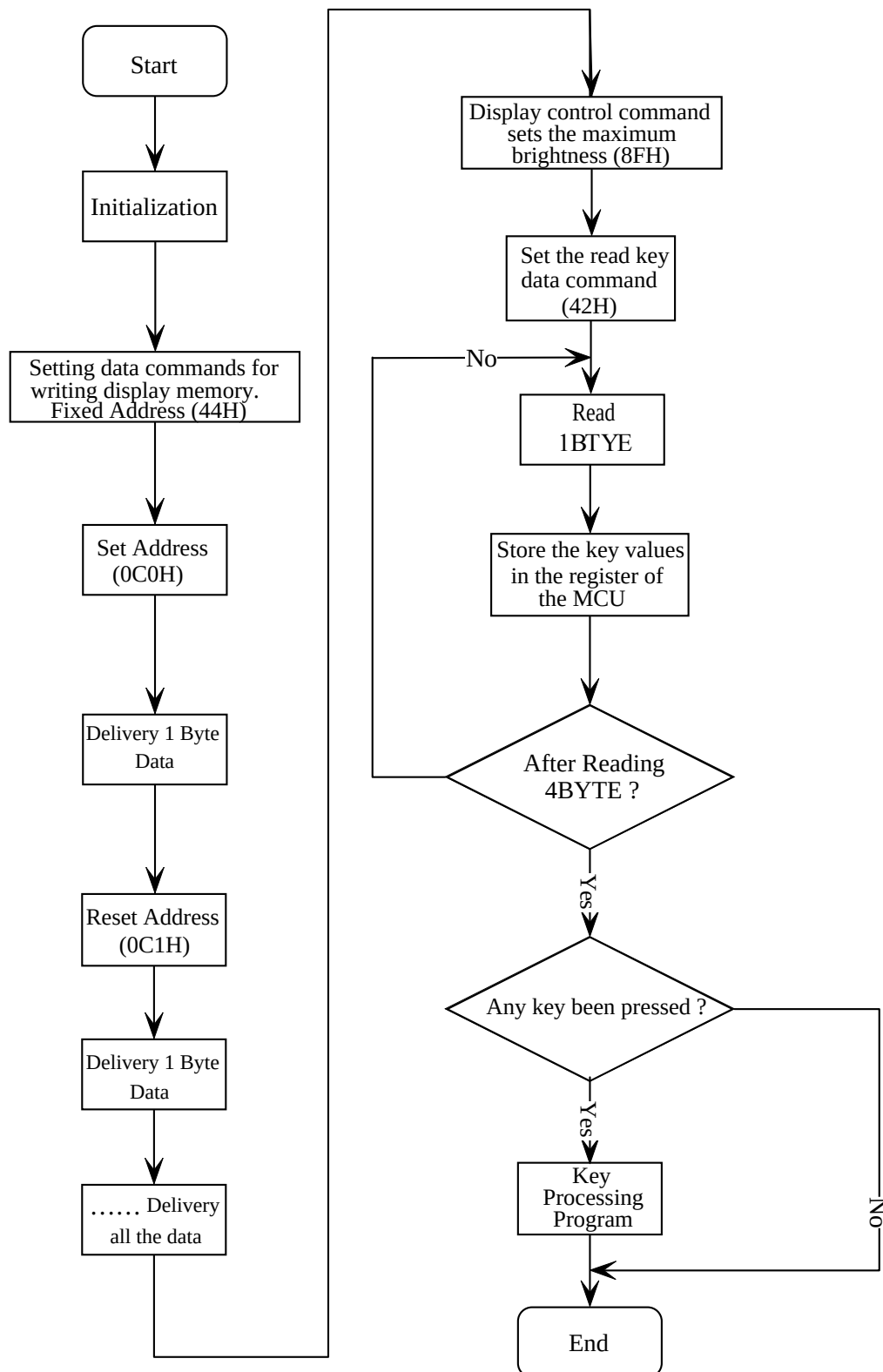
Data1 ~4: Read Key Data

Programming Flow Chart

Flow chart of automatic plus 1 address program:



Fixed address programming flow chart:



Application Circuit

TT1629BX drives hardware circuit of common anode digital screen, as shown in Fig.16

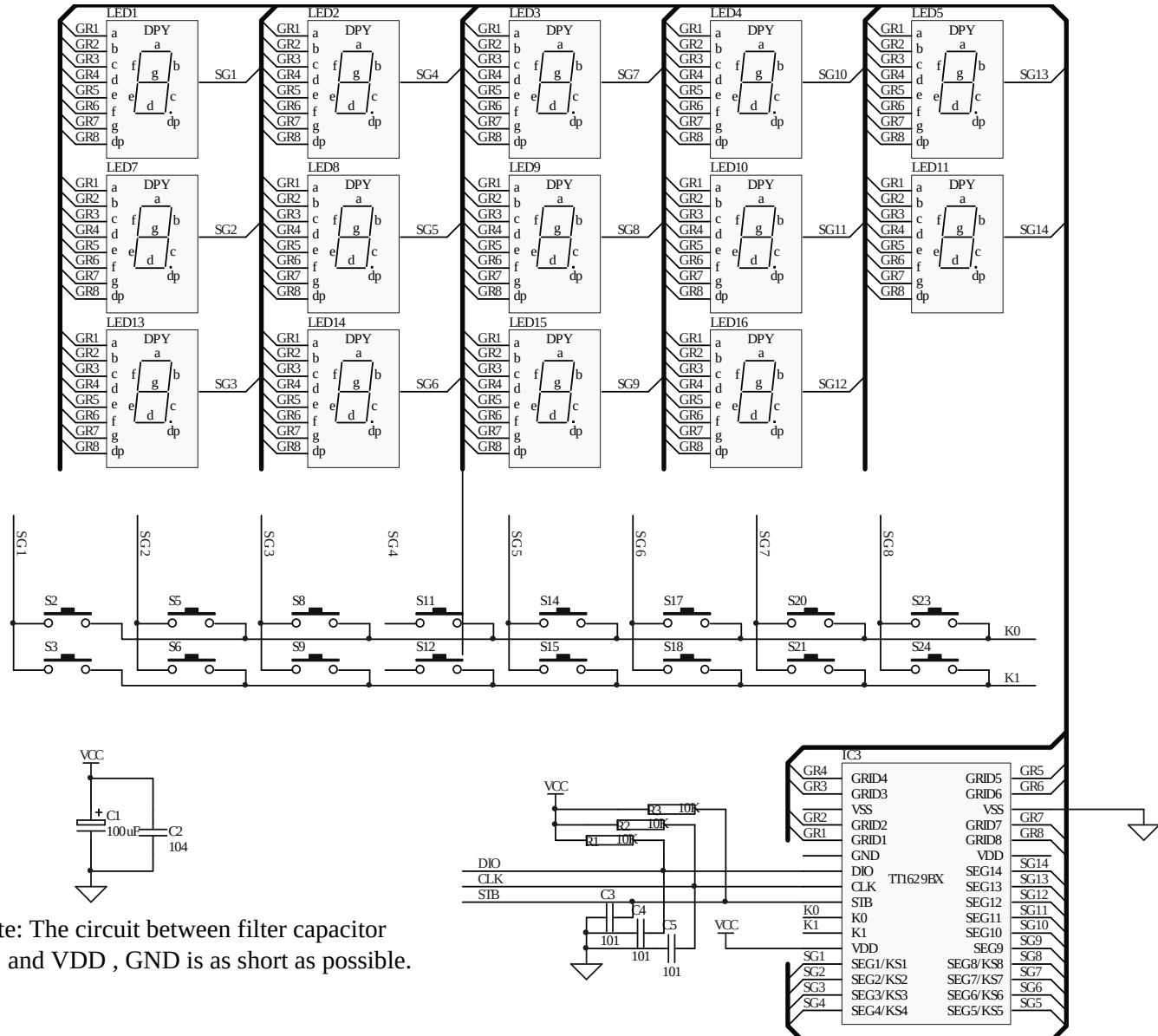


Fig.16

TT1629BX drives hardware circuit of common cathode digital screen, as shown in Fig.17

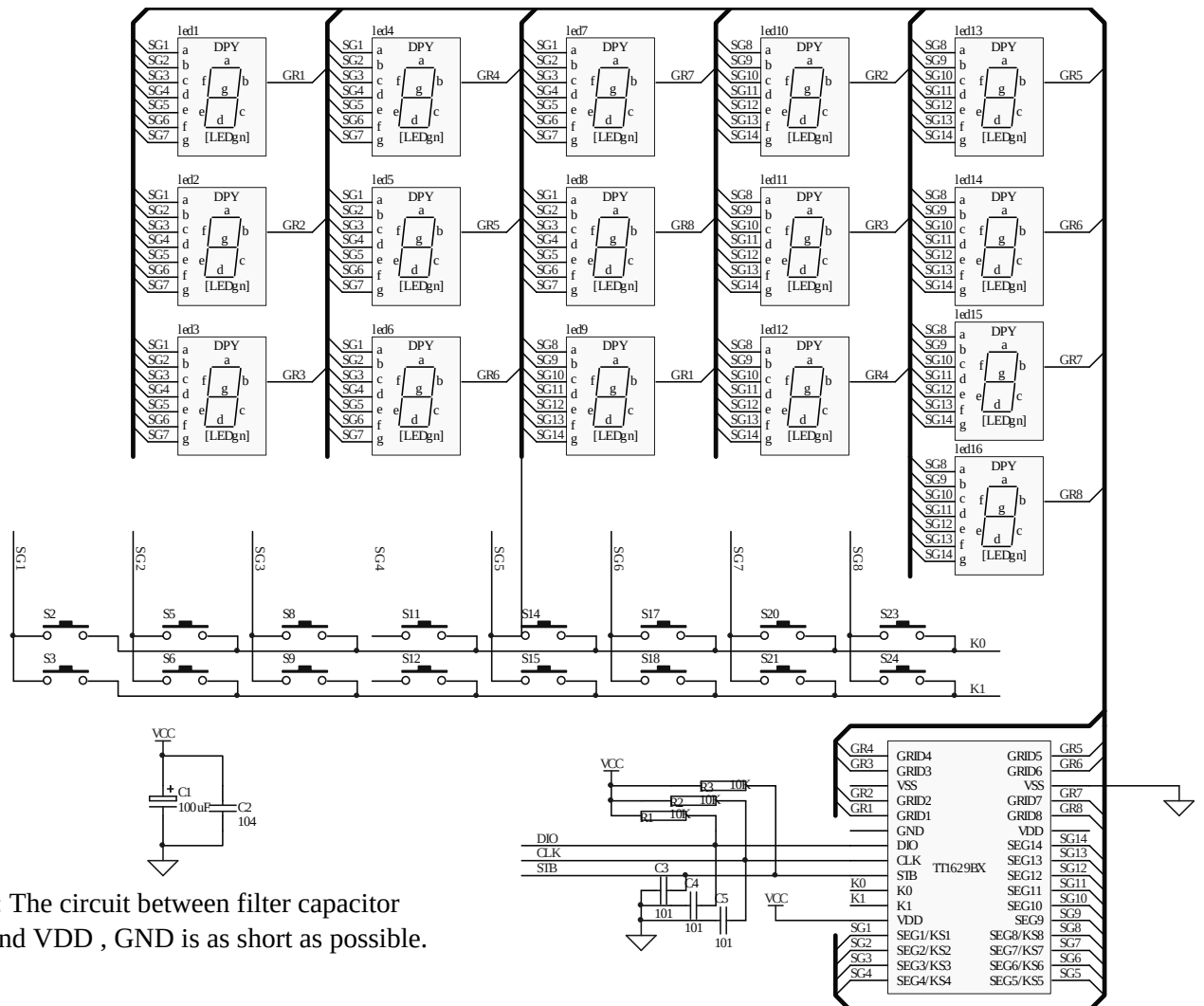


Fig.16

- ▲NOTE :**
- 1.The filter capacitor between VDD and GND should be placed as close as possible to TT1629BX chip to enhance the filtering effect.
 - 2.Three 100P capacitors connected to DIO, CLK and STB communication ports can reduce interference to communication ports.
 - 3.Because the forward voltage drop of blu-ray digital tube are about 3V, the power supply of TT1629BX should be 5V.

Electrical parameters

Absolute maximum ratings ($T_a = 25^{\circ}\text{C}$, $V_{ss} = 0\text{ V}$)

Parameter	Symbol	Range	Unit
Logic power supply voltage	VDD	-0.5 ~ +7.0	V
Logic Input Voltage	V _{I1}	-0.5 ~ VDD + 0.5	V
LED Seg Drive Output Current	IO1	-50	mA
LED Grid Drive Output Current	IO2	+200	mA
Power Loss	PD	400	mW
Working Temperature	T _{opt}	-40 ~ +80	°C
Storage Temperature	T _{stg}	-65 ~ +150	°C

Rated operating range ($T_a = -20 \sim +70^{\circ}\text{C}$, $V_{ss} = 0\text{ V}$)

Parameter	Symbol	Min.	Typical	Max.	Unit	Testing Conditions
Logic power supply voltage	VDD		5		V	-
High level input voltage	V _{IH}	0.7 VDD	-	VDD	V	-
Low level input voltage	V _{IL}	0	-	0.3 VDD	V	-

Electrical Characteristics ($T_a = -20 \sim +70^{\circ}\text{C}$, $V_{DD} = 4.5 \sim 5.5\text{ V}$, $V_{ss} = 0\text{ V}$)

Parameter	Symbol	Min.	Typical	Max.	Unit	Testing Conditions
High level output current	I _{oh1}	-20	-25	-40	mA	Seg1~Seg11, V _o = vdd-2V
	I _{oh2}	-20	-30	-50	mA	Seg1~Seg11, V _o = vdd-3V
Low level output current	I _{OL1}	80	140	-	mA	Grid1~Grid6 V _o =0.3V
Low level output current	I _{dout}	4	-	-	mA	V _O = 0.4V, d _{out}



High level output current allowance	I _{OLsg}	-	-	5	%	V _O = V _{DD} - 3V, Seg1~Seg11
Output pulldown resistance	R _L		10		K Ω	K1~K3
Input current	I _I	-	-	± 1	μ A	V _I = V _{DD} / V _{SS}
High level input voltage	V _{IH}	0.7 V _{DD}	-		V	CLK, DIN, STB
Low level input voltage	V _{IL}	-	-	0.3 V _{DD}	V	CLK, DIN, STB
Hysteresis voltage	V _H	-	0.35	-	V	CLK, DIN, STB
Dynamic Current Loss	I _{DDdyn}	-	-	5	mA	No load, Display off

Switching Characteristics (T_a = -20 ~ +70°C, V_{DD} = 4.5 ~ 5.5 V)

Parameter	Symbol	Min.	Typical	Max.	Unit	Testing Conditions	
Oscillation Frequency	f _{osc}	-	500	-	KHz	R = 16.5 K Ω	
Transmission delay time	t _{PLZ}	-	-	300	ns	CLK → DOUT	
	t _{PZL}	-	-	100	ns	CL = 15pF, R _L = 10K Ω	
Rise Time	TTZH 1	-	-	2	μ s	CL = 300p F	Seg1~Seg11
	TTZH 2	-	-	0.5	μ s		Grid1~Grid4 Seg12/Grid7~ Seg14/Grid5
Fall Time	TTHZ	-	-	120	μ s	CL = 300pF, Segn, Gridn	
Clock Frequency (Max.)	F _{max}	1	-	-	MHz	Duty Cycle 50%	
Input Capacitance	C _I	-	-	15	pF	-	

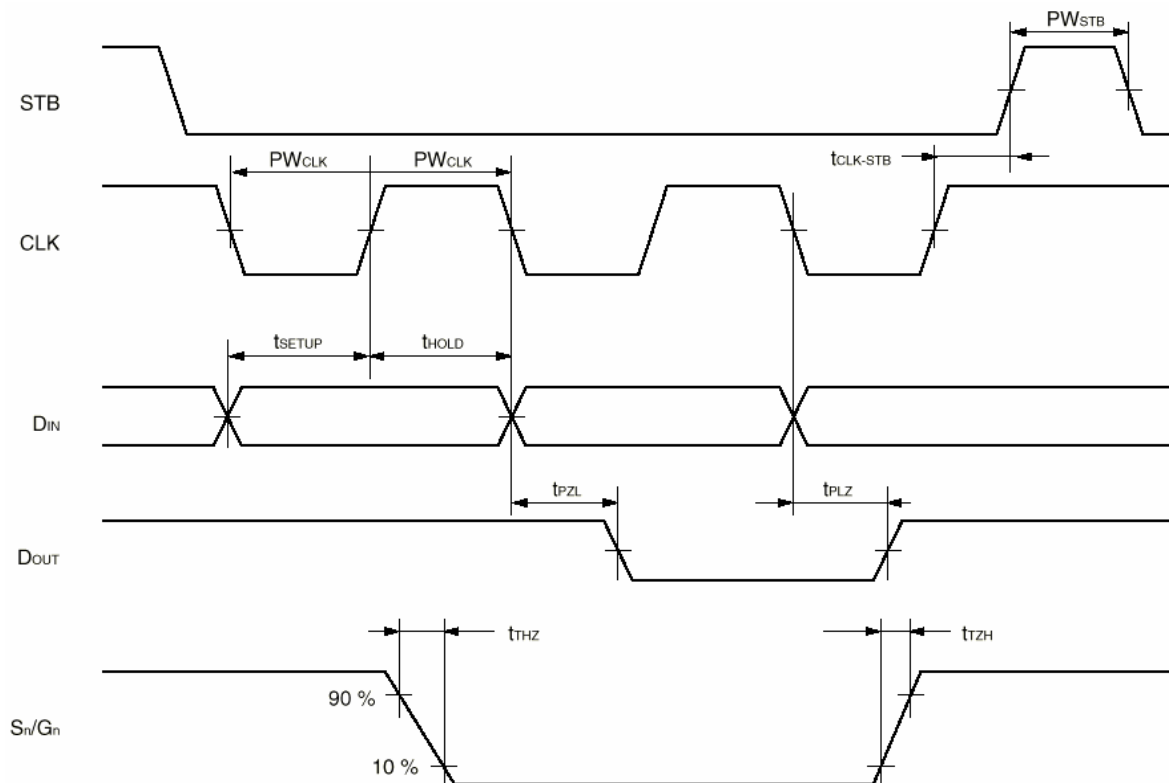


Timing Sequence Characteristic

($T_a = -20 \sim +70^{\circ}\text{C}$, $V_{DD} = 4.5 \sim 5.5\text{V}$)

Parameter	Symbol	Min.	Typical	Max.	Unit	Testing Conditions
Clock Pulse Width	PWCLK	400	-	-	ns	-
Strobe Pulse Width	PWSTB	1	-	-	μs	-
Data SetupTime	t _{SETUP}	100			ns	
Data Holding Time	t _{HOLD}	100	-	-	ns	-
CLK→STB Time	t _{CLK STB}	1			μs	CLK↑→STB↑
Waiting Time	t _{WAIT}	1	-	-	μs	CLK↑→CLK↓

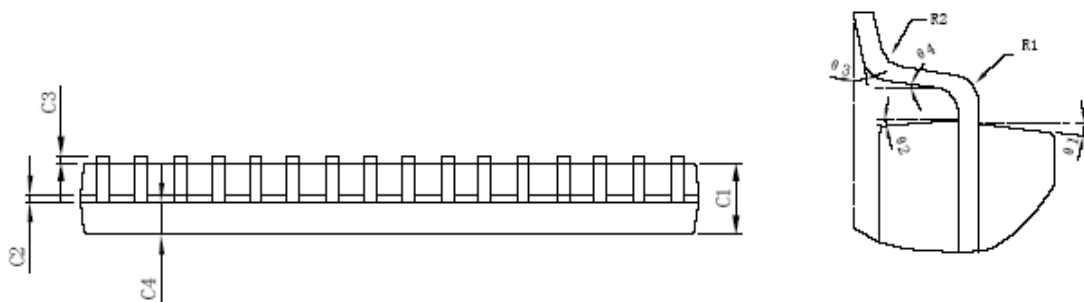
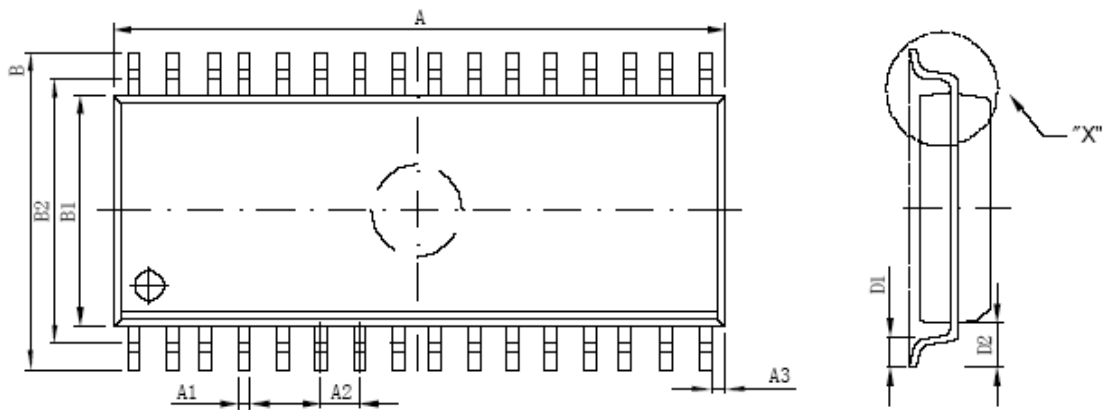
Timing Sequence Waveform





Package Size

SYMBOL \ SIZE	Min. (mm)	Max. (mm)	SYMBOL \ SIZE	Min. (mm)	Max. (mm)
A	20.88	21.08	C4	0.99TYP	
A1	0.3	0.5	D1	0.55	0.95
A2	1.27TYP		D2	1.45	
A3	0.77TYP		R1		
B	10.2	10.6	R2		
B1	7.42	7.62	θ 1	8°TYP	
B2	8.9TYP		θ 2	15°TYP	
C1	2.14	2.34	θ 3	4°TYP	
C2	0.2	0.32	θ 4	14°TYP	
C3	0.10	0.25			



DETAIL "X"

- All specs and applications shown above subject to change without prior notice.