Features

- Transient protection for high-speed data lines
  - IEC 61000-4-2 (ESD) ±25kV (Air)
    ±17kV (Contact)
  - IEC 61000-4-4 (EFT) 40A (5/50 ns)
  - IEC 61000-4-5 (Lightning) 3.0A (8/20μs)
  - Cable Discharge Event (CDE)
- Small package (1.6mm × 1.6mm × 0.75mm)
- Protects two data lines
- Low capacitance: 0.25pF Typical (I/O-I/O)
- Low leakage current: 0.1μA @ V_{RWM} (Typical)
- Low clamping voltage
- Each I/O pin can withstand over 1000 ESD strikes for ±8kV contact discharge

Description

TT0512TFX is an ultra-low capacitance Transient Voltage Suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With typical capacitance of 0.25pF only, TT0512TFX is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD), Level 4 (±15kV air, ±8kV contact discharge), IEC 61000-4-4 (electrical fast transient - EFT) (40A, 5/50 ns), very fast charged device model (CDM) ESD and cable discharge event (CDE), etc.

TT0512TFX uses small SOT523 package. Each TT0512TFX device can protect two high-speed data lines. The combined features of low capacitance, small size and high ESD robustness make TT0512TFX ideal for high-speed data ports and high-frequency lines (e.g., USB2.0 & DVI) applications. The low clamping voltage of the TT0512TF guarantees a minimum stress on the protected IC.

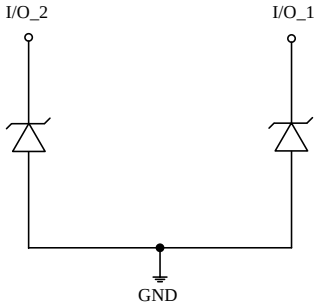
Applications

- Serial ATA
- PCI Express
- Desktops, Servers and Notebooks
- MDDI Ports
- USB2.0 Power and Data Line Protection
- Display Ports
- Digital Visual Interfaces (DVI)

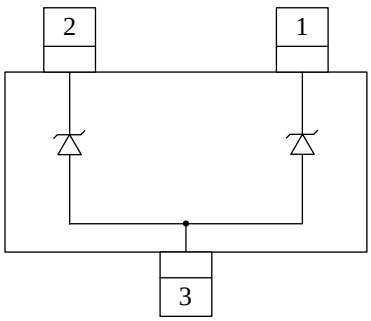
Mechanical Characteristics

- SOT523 package
- Flammability Rating: UL 94V-0
- Marking: Part number, Date
- Packaging: Tape and Reel

Circuit Diagram



Pin Configuration



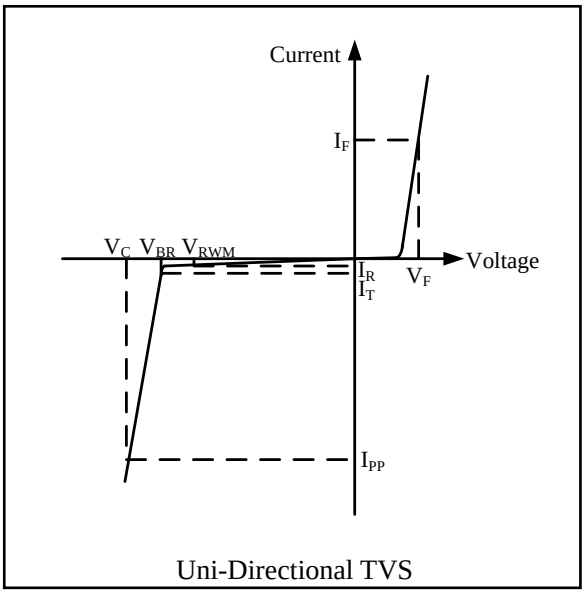
SOT523
(Top View, not to scale)

Absolute Maximum Rating

Symbol	Parameter	Value	Units
V_{ESD}	ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	±25 ±17	kV
T_{OPT}	Operating Temperature	-55/+125	°C
T_{STG}	Storage Temperature	-55/+150	°C
I_{PP}	Peak Pulse Current (8/20μs)	3	A

Electrical Characteristics (T = 25°C)

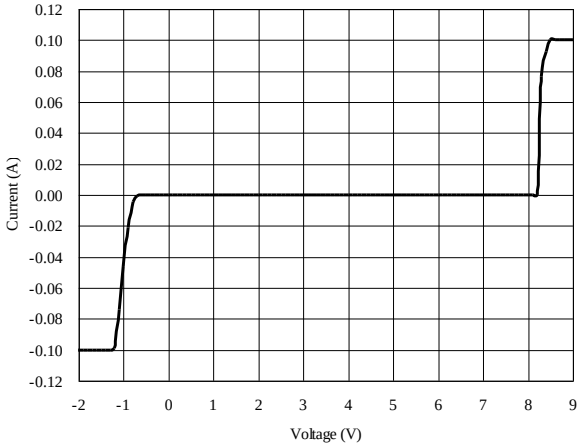
Symbol	Parameter
V_{RWM}	Nominal Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Reverse Breakdown Voltage @ I_T
I_T	Test Current for Reverse Breakdown
V_C	Clamping Voltage @ I_{PP}
I_{PP}	Maximum Peak Pulse Current
C_{ESD}	Parasitic Capacitance
V_R	Reverse Voltage
f	Small Signal Frequency
I_F	Forward Current
V_F	Forward Voltage @ I_F



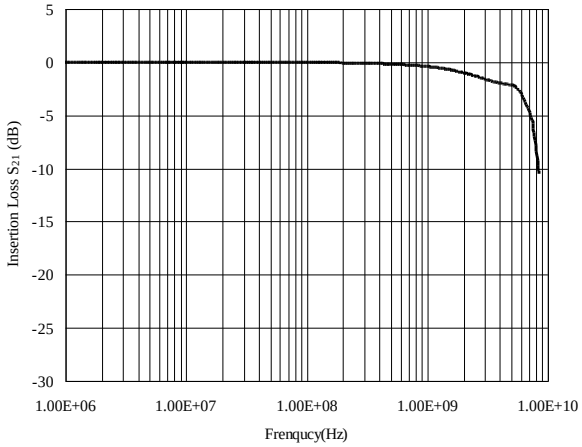
Uni-Directional TVS

Symbol	Test Condition	Minimum	Typical	Maximum	Units
V_{RWM}				5.0	V
I_R	V_{RWM} = 5V, T = 25°C Between I/O and GND		0.1	1.0	μA
V_{BR}	I_T = 1mA Between I/O and GND	6.0	8.0	10.0	V
V_C	I_{PP} = 3A, t_p = 8/20μs Between I/O and GND			13	V
C_{ESD}	V_R = 0V, f = 1MHz Between I/O and GND		0.8	1.2	pF
C_{ESD}	V_R = 0V, f = 1MHz Between I/O and I/O		0.25	0.5	pF

Voltage Sweeping of I/O to I/O

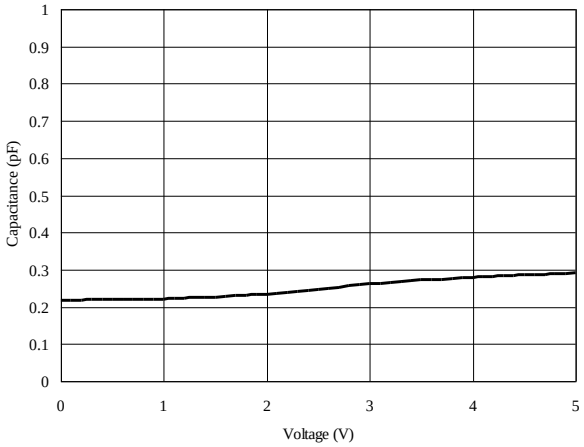


Insertion Loss S21 of I/O to I/O

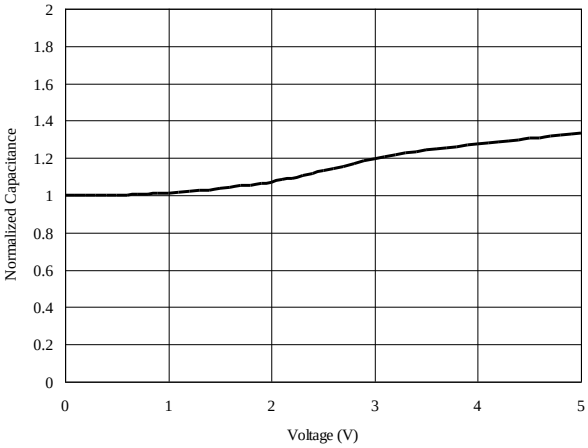


Capacitance vs. Voltage of I/O to I/O (f = 1MHz)

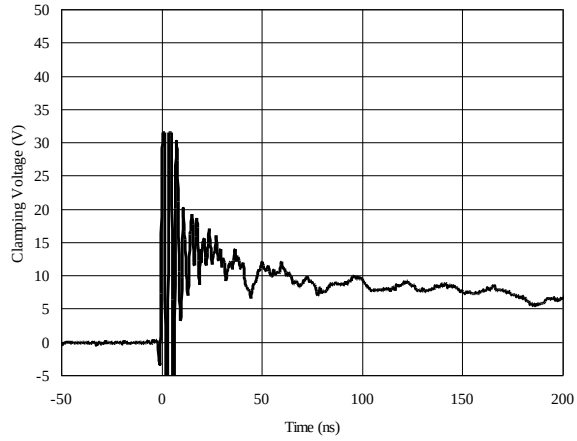
Capacitance *vs.* Reverse Voltage



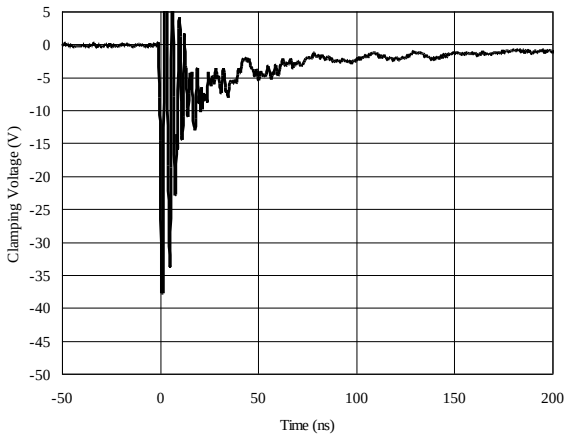
Normalized Capacitance *vs.* Reverse Voltage



ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)



ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)



Application Information

Pin Connection in PCB

TT0512TFX is capable to provide ESD protection for two data lines simultaneously. The pin connection is shown in Figure 1.

Two parallel data lines, from inner IC to I/O port connector, could connect to TT0512TFX two I/O pins directly. Pin 3 of TT0512TFX is the negative reference pin, which should connect to the GND of PCB. The connection wires should be as short as possible in order to minimize the parasitic inductance.

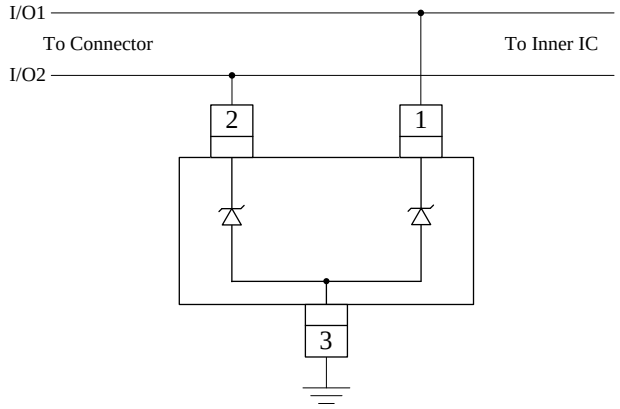


Figure 1 TT0512TF pin connection in PCB

PCB Layout Guidelines

For optimum ESD protection and the whole circuit performance, the following PCB layout guidelines are recommended:

- ❑ TT0512TFX GND pin to the PCB GND rail path should be as short as possible. It could reduce the ESD transient return path to GND.
- ❑ The vias connecting TT0512TFX VCC & GND pins to the PCB VCC & GND should be wide.
- ❑ Place TT0512TFX as close to the connector port as possible. It could reduce the parasitic inductance and restrict ESD coupling into adjacent traces.
- ❑ Avoid running critical signals near board edges.

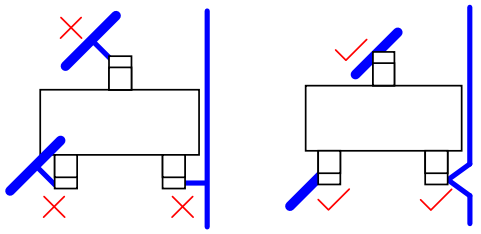


Figure 2 TT0512TFX Layout Guidelines

Universal Serial Bus ESD Protection

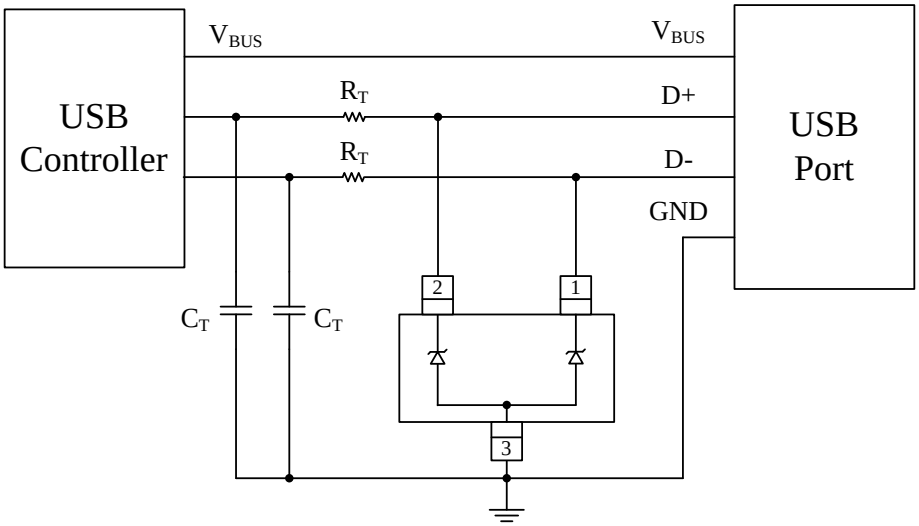
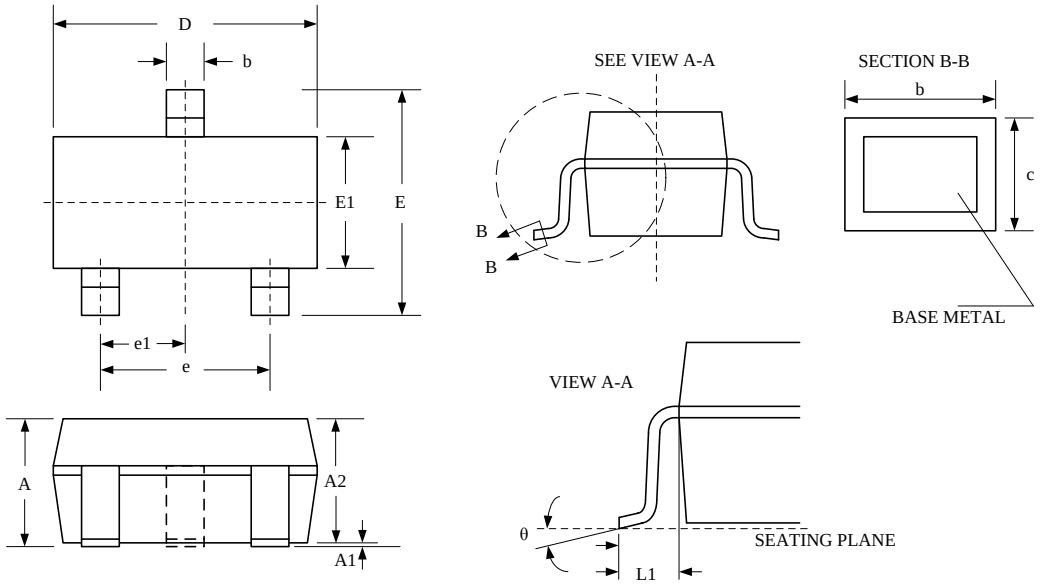


Figure 3 Schematic and Diagram for USB 2.0 Protection using TT0512TFX

Package Outline

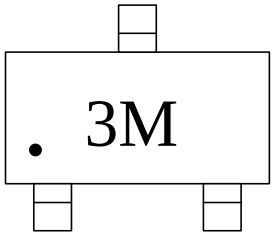
❑ SOT523 package



Package Dimensions (Controlling dimensions are in millimeters)

Symbol	Dimensions (mm)			Dimensions (Inches)		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
A	0.600	—	0.900	0.023	—	0.035
A1	0.000	—	0.100	0.000	—	0.004
A2	0.600	0.750	0.800	0.023	0.030	0.031
b	0.150	—	0.300	0.005	—	0.012
c	0.100	—	0.200	0.003	—	0.008
D	1.500	1.600	1.700	0.059	0.063	0.067
e	1.00 BSC			0.039 BSC		
e1	0.50 BSC			0.020 BSC		
E	1.450	1.600	1.750	0.057	0.063	0.069
E1	0.750	0.800	0.850	0.029	0.031	0.033
L1	0.220 REF			0.009 REF		
θ	0°	—	8°	0°	—	8°

Marking Codes



Note:

(1) "3M" is part number, fixed.

Ordering Information

Part Number	Working Voltage	Quantity Per Reel	Reel Size
TT0512TFX	5V	3,000	7 Inch