BATTERY PROTECTION IC FOR SINGLE-CELL PACK

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The JYBP8261X series are lithium-ion / lithium polyme rechargeable battery protection ICs incorporating high-accuracy voltage detection circuit and delay circuit.
The JYBP8261X series are suitable for protection of single-cell lithium ion/lithium polymer battery packs from overcharge , overdischarge and overcurrent.

■ Features

(1) Internal high accuracy voltage detection circuit
- Overcharge detection voltage 4.288V
  Accuracy: ±25 mV (+25°C)
- Overdischarge detection voltage 3.0V
  Accuracy: ±35 mV (+25°C)
- Overdischarge Overcurrent 0.08V
  Accuracy: ±15 mV (+25°C)
- Short Current Detection 0.09V
  Accuracy: ±30 mV (+25°C)

(2) High voltage device is used for charger connection pins
(VM and CO pins: absolute maximum rating = 28 V)

(3) Low current consumption
- Operation mode 3.0 μA typ., 6.0 μA max.
- Power-down mode 0.1 μA max.

(4) Wide operating temperature range –40 °C to +85 °C
Wide Storage temperature range –55 °C to +125 °C

(5) Small package SOT-23-6, 6-Pin SNB(B)

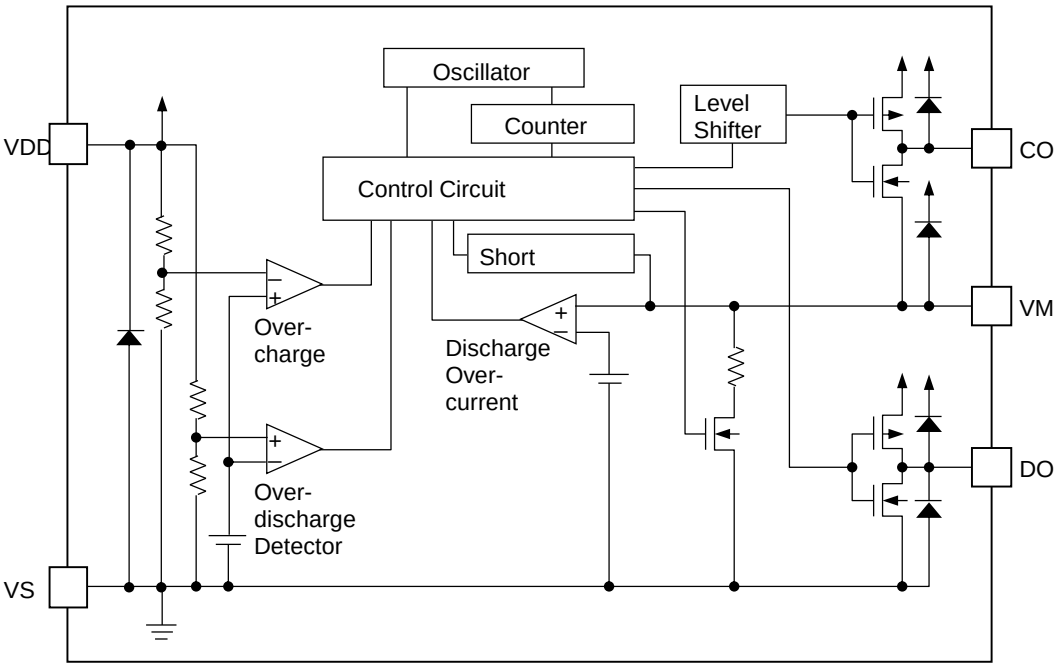
(6) Lead free products

***1.** Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage
(where overcharge release voltage < 3.8 V is prohibited.)
***2.** Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(where overdischarge release voltage > 3.4 V is prohibited.)

■ Applications

- Lithium-ion rechargeable battery packs
- Lithium polymer rechargeable battery packs

Functional Block Diagram



Terminal explanations

Terminal No.	Symbol	Descriptions
1	VSS	Negative power input
2	CO	FET gate connection for charge control (CMOS output)
3	VDD	Positive power input (Chip back side)
4	VM	Voltage monitoring for charger negative
5	DO	FET gate connection for discharge control (CMOS output)

Absolute maximum ratings

Topr = 25 degrees

Item	Symbol	Rating	Unit
Supply Voltage	VDD	VSS-0.3 to VSS+7	V
VM Terminal Input Voltage	VM	VDD-28 to VDD+0.3	V
CO Terminal Output Voltage	VCO	VDD-28 to VDD+0.3	V
DO Terminal Output Voltage	VDO	VSS-0.3 to VDD+0.3	V
Operating Temperature	Topr	-40 to +85	℃
Storage Temperature	Tstg	-55 to +125	℃

Electrical characteristics

Topr = 25℃

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test circuit
Operating Input Voltage	VDD	VDD - VSS	1.5	-	5.5	V	1
Minimum Operating Voltage for 0V Charging	Vcha	VDD - VM, VDD-VSS=0V	-	-	1.4	V	3
Discharge Over-current Release Resistance	Rdwn	VDD=3.5V, VM=1.0V	30	50	100	kΩ	5
CO Pch ON Resistance	Rcop	CO=3.0V, VDD=3.5V, VM=0V	1.0	2.5	4.0	kΩ	5
CO Nch ON Resistance	Rcon	CO=0.5V, VDD=4.6V, VM=0V	0.5	1.4	2.2	kΩ	5
DO Pch ON Resistance	Rdop	DO=3.0V, VDD=3.5V, VM=0V	0.5	1.4	2.2	kΩ	5
DO Nch ON Resistance	Rdon	DO=0.5V, VDD=VM=1.8V	0.5	1.4	2.2	kΩ	5
Current Consumption	Iopr	VDD=3.5V, VM=0V	-	3.0	6.0	uA	4
Current Consumption at Shutdown	Isdn	VDD=VM=1.8V	-	-	0.1	uA	4
Overcharge Detection	VDET1	R1=330Ω	4.255	4.280	4.305	V	1
	tVDET1	VDD=VDET1-0.2V → VDET1+0.2V, VM=0V	1.02	1.28	1.54	s	6
	VREL1	R1=330Ω	4.050	4.080	4.110	V	1
	tVREL1	VDD=VDET1+0.2V → VDET1-0.2V, VM=1.0V	1.6	2.0	2.4	ms	6
Overdischarge Detection	VDET2	R1=330Ω	2.965	3.000	3.035	V	1
	tVDET2	VDD=VDET2+0.2V → VDET2-0.2V, VM=0V	102.0	128.0	154.0	ms	6
	VREL2	R1=330Ω	2.930	3.000	3.070	V	1
	tVREL2	VDD=VDET2-0.2V → VDET2+0.2V, VM=-2.0V	1.6	2.0	2.4	ms	6
Overdischarge Overcurrent	VDET3	VDD=3.5V	0.065	0.080	0.095	V	2
	tVDET3	VDD=3.5V, VM=0 → 1.0V	6.4	8.0	9.6	ms	6
	tVREL3	VDD=3.5V, VM=1.0 → 0V	1.6	2.0	2.4	ms	6
Short Current Detection	VDET5	VDD=3.5V	0.60	0.90	1.20	V	2
	tVDET5	VDD=3.5V, VM=0 → 3.5V	250	375	550	us	6
	tVREL5	VDD=3.5V, VM=3.5 → 0V	1.6	2.0	2.4	ms	6
Abnormal Charger Detection Voltage	Vchg	VDD=3.5V, R2=2.2kΩ	-1.60	-1.30	-1.00	V	7

Electrical characteristics

Topr = -5~60℃

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test circuit
Overcharge Detection	VDET1	R1=330Ω	4.250	4.280	4.310	V	1
	tVDET1	VDD=VDET1-0.2V → VDET1+0.2V, VM=0V	0.89	1.28	1.67	s	6
	VREL1	R1=330Ω	4.040	4.080	4.120	V	1
	tVREL1	VDD=VDET1+0.2V → VDET1-0.2V, VM=1.0V	1.4	2.0	2.6	ms	6
Overdischarge Detection	VDET2	R1=330Ω	2.950	3.000	3.050	V	1
	tVDET2	VDD=VDET2+0.2V → VDET2-0.2V, VM=0V	89.0	128.0	167.0	ms	6
	VREL2	R1=330Ω	2.920	3.000	3.080	V	1
	tVREL2	VDD=VDET2-0.2V → VDET2+0.2V, VM=-2.0V	1.4	2.0	2.6	ms	6
Overdischarge Overcurrent	VDET3	VDD=3.5V	0.060	0.080	0.100	V	2
	tVDET3	VDD=3.5V, VM=0 → 1.0V	5.6	8.0	10.4	ms	6
	tVREL3	VDD=3.5V, VM=1.0 → 0V	1.4	2.0	2.6	ms	6
Short Current Detection	VDET5	VDD=3.5V	0.55	0.90	1.25	V	2
	tVDET5	VDD=3.5V, VM=0 → 3.5V	230	375	600	us	6
	tVREL5	VDD=3.5V, VM=3.5 → 0V	1.4	2.0	2.6	ms	6
Abnormal Charger Detection Voltage	Vchg	VDD=3.5V, R2=2.2kΩ	-1.65	-1.30	-0.95	V	7

The specification for this temperature range is guaranteed by design, not tested in production.

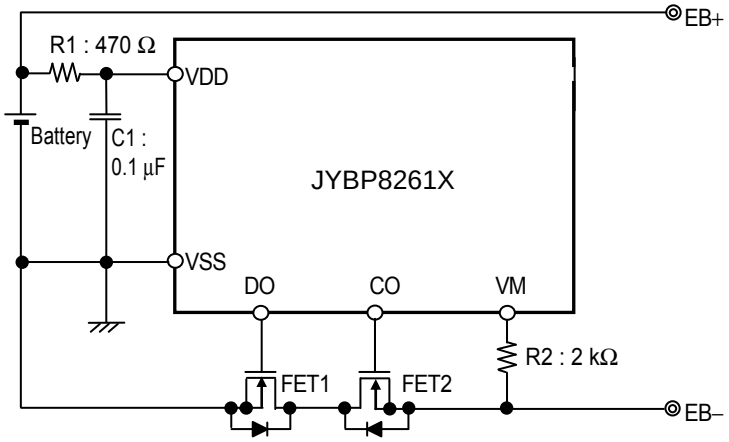
Electrical characteristics

Topr = -30~70℃

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test circuit
Overcharge Detection	VDET1	R1=330Ω	4.235	4.280	4.325	V	1
	tVDET1	VDD=VDET1-0.2V → VDET1+0.2V, VM=0V	0.77	1.28	1.79	s	6
	VREL1	R1=330Ω	4.020	4.080	4.140	V	1
	tVREL1	VDD=VDET1+0.2V → VDET1-0.2V, VM=1.0V	1.2	2.0	2.8	ms	6
Overdischarge Detection	VDET2	R1=330Ω	2.930	3.000	3.070	V	1
	tVDET2	VDD=VDET2+0.2V → VDET2-0.2V, VM=0V	77.0	128.0	179.0	ms	6
	VREL2	R1=330Ω	2.900	3.000	3.100	V	1
	tVREL2	VDD=VDET2-0.2V → VDET2+0.2V, VM=-2.0V	1.2	2.0	2.8	ms	6
Overdischarge Overcurrent	VDET3	VDD=3.5V	0.055	0.080	0.105	V	2
	tVDET3	VDD=3.5V, VM=0 → 1.0V	4.8	8.0	11.2	ms	6
	tVREL3	VDD=3.5V, VM=1.0 → 0V	1.2	2.0	2.8	ms	6
Short Current Detection	VDET5	VDD=3.5V	0.50	0.90	1.30	V	2
	tVDET5	VDD=3.5V, VM=0 → 3.5V	190	375	750	us	6
	tVREL5	VDD=3.5V, VM=3.5 → 0V	1.2	2.0	2.8	ms	6
Abnormal Charger Detection Voltage	Vchg	VDD=3.5V, R2=2.2kΩ	-1.70	-1.30	-0.90	V	7

The specification for this temperature range is guaranteed by design, not tested in production.

■ Battery Protection IC Connection Example



Symbol	Part	Purpose	Min.	Typ.	Max.	Remarks
FET1	N-channel MOS FET	Discharge control	—	—	—	Threshold voltage ≤ Overdischarge detection voltage*1 Gate to source withstanding voltage ≥ Charger voltage*2
FET2	N-channel MOS FET	Charge control	—	—	—	Threshold voltage ≤ Overdischarge detection voltage*1 Gate to source withstanding voltage ≥ Charger voltage*2
R1	Resistor	ESD protection, For power fluctuation	300 Ω	470 Ω	1 kΩ	Resistance should be as small as possible to avoid lowering of the overcharge detection accuracy caused by VDD pin current.*3
C1	Capacitor	For power fluctuation	0.022 µF	0.1 µF	1.0 µF	Install a capacitor of 0.022 µF or higher between VDD and VSS.*4
R2	Resistor	Protection for reverse connection of a charger	300 Ω	2 kΩ	4 kΩ	Select a resistance as large as possible to prevent large current when a charger is connected in reverse.*5

***1.** If the threshold voltage of an FET is low, the FET may not cut the charging current.
If an FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stopped before overdischarge is detected.

***2.** If the withstanding voltage between the gate and source is lower than the charger voltage, the FET may be destroyed.

***3.** If R1 has a high resistance, the voltage between VDD and VSS may exceed the absolute maximum rating when a charger is connected in reverse since the current flows from the charger to the IC. Insert a resistor of 300 Ω or higher to R1 for ESD protection.

***4.** If a capacitor of less than 0.022 µF is connected to C1, DO may oscillate when load short-circuiting is detected. Be sure to connect a capacitor of 0.022 µF or higher to C1.

***5.** If R2 has a resistance higher than 4 kΩ, the charging current may not be cut when a high-voltage charger is connected.

Operation

- **Normal condition**

  This IC monitors the battery voltage (VDD) and the voltage of VM terminal, and controls charge and discharge.
  If VDD is in the range from the over-discharge detection voltage (VDET2) to the over-charge detection voltage (VDET1) and the VM terminal voltage is lower than the over-current detection voltage (VDET3), this IC turns on both the charge and discharge control FETs. This state is called the normal condition, and charge and discharge are possible together.

- **Discharge over-current detection, Load short-circuiting detection**

  When the discharge current becomes equal to or higher than the specified value under the normal condition, and if the VM terminal voltage is in the range from the discharge over-current detection voltage (VDET3) to the short-circuiting detection voltage (VDET5) and that state is maintained during more than the discharge over-current detection delay time (tVDET3), this IC turns off the discharge control FET to stop discharge. This state is called the discharge over-current detection condition.
  At that time, if the VM terminal voltage is equal to or higher than VDET5 and that state is maintained during more than the load short-circuiting detection delay time (tVDET5), this IC turns off the discharge control FET to stop discharge. This state is called the load short-circuiting detection condition.
  While load is connected, in both conditions, the VM terminal voltage equals to VDD potential due to the load, but it falls by the discharge over-current release resistance (Rdwn) when the load is removed and the resistance between (+) and (-) terminals of battery pack becomes larger than the value which enables the automatic return.
  Then the VM terminal voltage becomes less than VDET3, and if that state is maintained during more than the discharge over-current release delay time (tVREL3), this IC returns to normal condition.

Operation

- **Overcharge detection**

When the battery voltage (VDD) under the normal condition becomes equal to or higher than the over-charge detection voltage (VDET1) and that state is maintained during more than the over-charge detection delay time (tVDET1), this IC turns off the charge control FET and stops charge. This state is called the over-charge detection condition.
Release of the over-charge detection condition includes following two cases.

(1) When the VDD voltage falls to the over-charge release voltage (VREL1) without load and that state is maintained during more than the Over-charge release delay time (tVREL1), this IC turns on the charge control FET and returns to the normal condition.

(2) When the load is installed and discharge starts, the discharge current flows through the internal parasitic diode of the charge control FET. Then the VM terminal voltage rises to only the Vf voltage of the internal parasitic diode over VSS potential and becomes higher than the discharge over-current detection voltage (VDET3). In this case, this IC returns to the normal condition when the VDD becomes equal to or lower thanVDET1 and that state continues more than the release delay time (tVREL1).

- **Overdischarge detection**

When the battery voltage (VDD) under the normal condition becomes equal to or less than the over-discharge detection voltage (VDET2) and that state is maintained during more than the over-discharge detection delay time (tVDET2), this IC turns off the discharge control FET and stops discharge. This state is called the over-discharge detection condition.
The over-discharge detection condition is released when the charger is connected as following two cases.

(1) When the charger is connected and charge starts, the charge current flows through the internal parasitic diode of the discharge control FET. Then VM terminal voltage falls to only the Vf voltage of the internal parasitic diode under VSS potential.
If VM terminal voltage is less than the abnormal charger detection voltage (Vchg), the over-discharge detection is released when VDD is higher than the over-discharge detection voltage (VDET2).

(2) In case (1), If VM terminal voltage is higher than the abnormal charger detection voltage (Vchg), the over-discharge detection is released when VDD is higher than the over-discharge release voltage (VREL2).

This over-discharge release function has delay time (tVREL2).

This IC stops all internal circuits (Shut down condition) after detecting the over-discharge and reduces current consumption. (MAX0.1μA at VDD=1.8V)

- **Charge to 0V battery**

If the voltage of charger (the voltage between VDD and VM) is larger than the Minimum Operationg Voltage for 0V Charging (Vcha), 0V battery charge becomes possible when CO terminal outputs VDD potential and turns on the charge control FET.

- **Abnormal Charger detection**

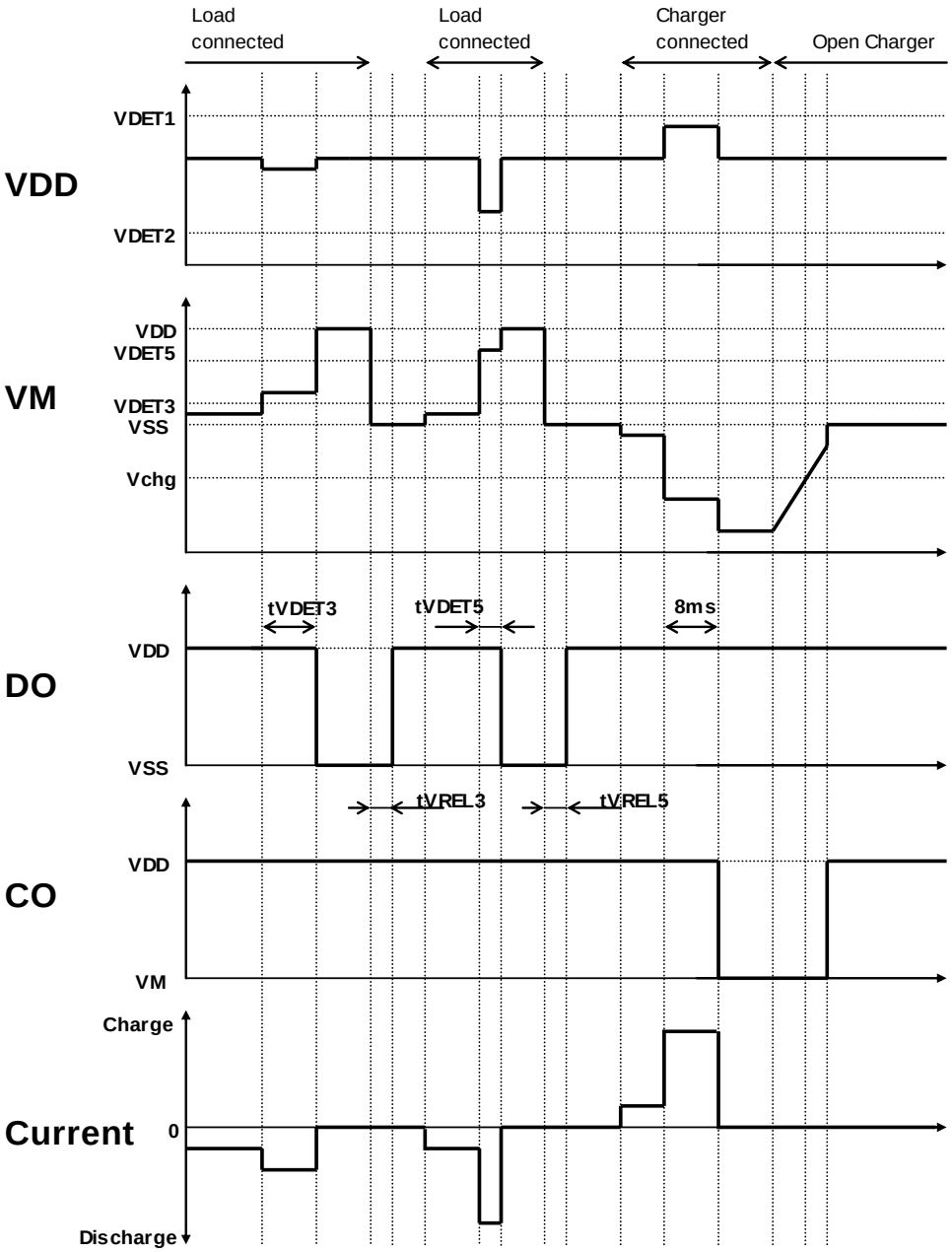
Under normal condition, when VM voltage becomes less than the Abnormal Charger detection voltage (Vchg), this IC turns off the charge control FET and stops charge. And then VM becomes higher than Vchg, this IC turns on the charge control FET and returns to the normal condition.
This function has the detection delay time 8ms (typ.).

- **DS delay shortening function**

In the test, tVDET1 delay time are shortened by making VDD=6.5[V]
tVDET1 is shortened to 1/100 (typical).

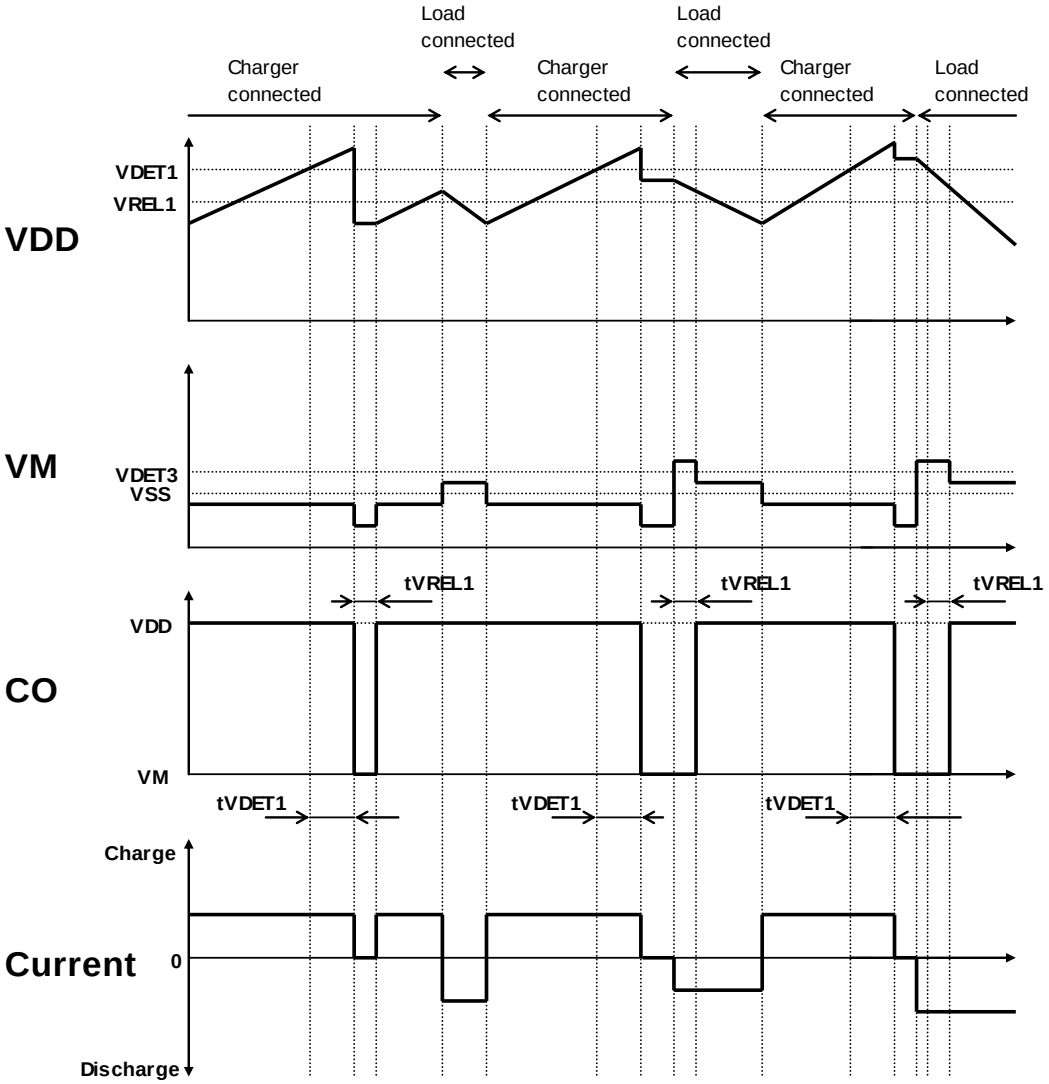
Timing Chart

1. Discharge over-current, Load short-circuiting, Abnormal charger detection



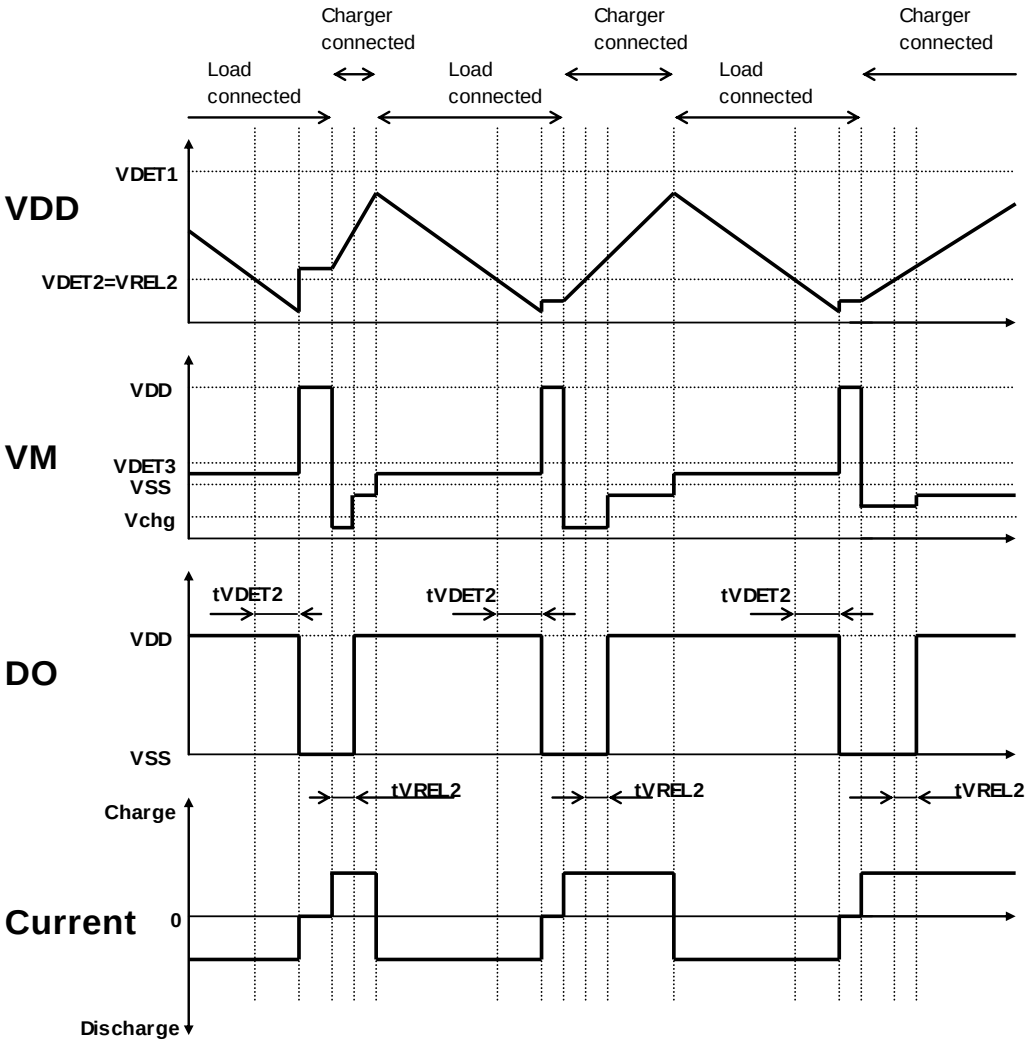
Timing Chart

2. Over charge



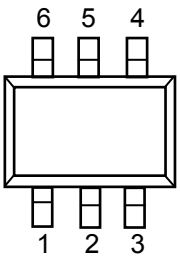
Timing Chart

3. Over discharge



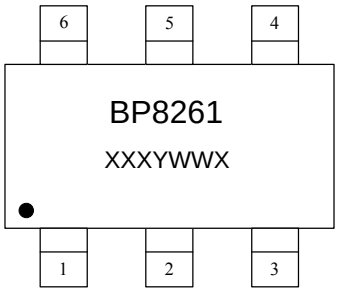
Pin Configuration

SOT-23-6
Top view



Pin No.	PIN NAME	Descriptions
1	DO	FET gate connection for discharge control
2	VM	Voltage monitoring for charger negative
3	CO	FET gate connection for charge control
4	NC	N / C
5	VDD	Positive power input
6	VSS	Negative power input

Marking Information



(1) BP8261: Part number,fixed

(2) XXX: Wafer's Lot No

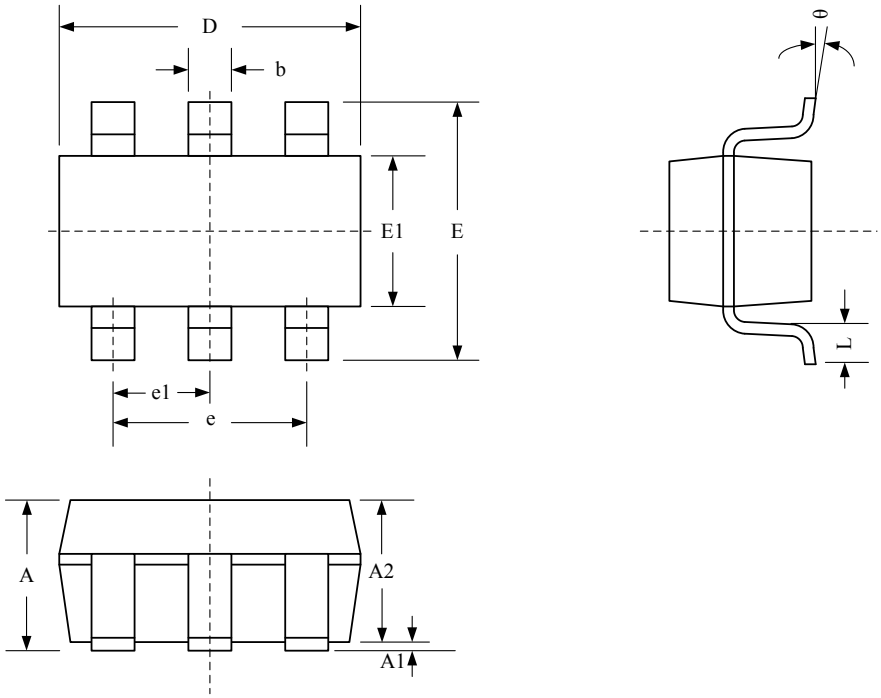
Y: Assembly year

WW: Assembly week

X: Internal code

Package Outline

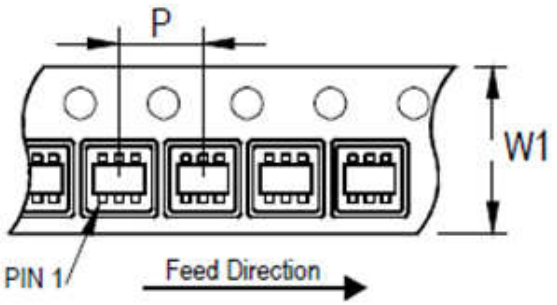
SOT23-6L package

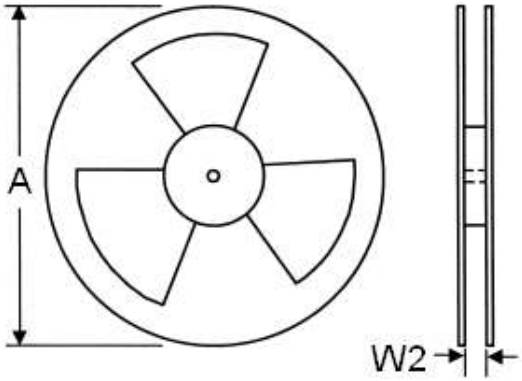


Package Dimensions (Controlling dimensions are in millimeters)

Symbol	Dimensions (mm)			Dimensions (Inches)		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
A	—	—	1.450	—	—	0.057
A1	0.000	—	0.150	0.000	—	0.006
A2	—	—	1.300	—	—	0.012
b	0.300	—	0.500	0.012	—	0.020
D	2.90 BSC			0.114 BSC		
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
E	2.80 BSC			0.110 BSC		
E1	1.60 BSC			0.063 BSC		
L	0.300	0.450	0.600	0.012	0.018	0.024
θ	0	4	8	0	4	8

Carrier Dimensions





Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	300~1000	3,000