Dual-Channel Low-Side Gate Driver

Hynetek Semiconductor Co., Ltd.

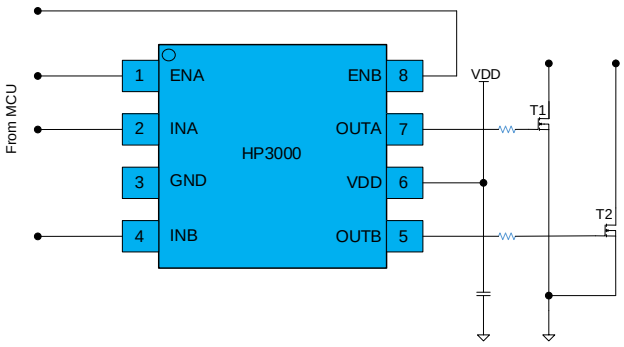
HP3000

FEATURES

- Typical 5-A peak source and sink drive current for each channel
- Input and enable pins capable of handling -12 V
- Output capable of handling -2 V transients
- Absolute maximum VDD voltage: 35 V
- Wide VDD operating range from 4.5 V to 30 V with UVLO
- Two independent gate drive channels
- Independent enable function for each output
- Hysteretic-logic thresholds for high noise immunity
- VDD independent input thresholds (TTL compatible)
- Fast propagation delays (22-ns typical)
- Fast rise and fall times (7-ns and 9-ns typical)
- 1-ns typical delay matching between the two channels
- Two channels can be paralleled for higher drive current
- SOP-8L and DFN2X2-8L package options
- Operating junction temperature range of -40 °C to 150 °C

APPLICATIONS

Switch-mode power-supplies (SMPS)
Power factor correction (PFC) circuits
DC-DC converter
Motor drives
Solar power supplies
Pulse transformer driver



Typical Application Circuit

GENERAL DESCRIPTION

The HP3000 is a dual-channel, high-speed, low-side gate driver that effectively drives MOSFET, IGBT, SiC, and GaN power switches. It has a typical peak drive strength of 5 A which reduces rise and fall times of the power switches, lowers switching losses, and increases efficiency. The fast propagation delay (22-ns typical) yields better power stage efficiency by improving the dead time optimization, pulse width utilization, control loop response, and transient performance of the system.

HP3000 can handle -12 V at its inputs, which improves robustness in systems with moderate ground bouncing. The inputs are independent of supply voltage and can be connected to most controller outputs for maximum control flexibility. An independent enable signal allows the power stage to be controlled independently of main control logic. In the event of a system fault, the gate driver can quickly shut-off by pulling enable low. Many high-frequency switching power supplies exhibit noise at the gate of the power device, which can get injected into the output pin on the gate driver and can cause the driver to malfunction. The HP3000's transient reverse current and reverse voltage capability allow it to tolerate noise on the gate of the power device or pulse-transformer and avoid driver malfunction.

The HP3000 also features under voltage lockout (UVLO) for improved system robustness. When there is not enough bias voltage to fully enhance the power device, the gate driver output is held low by the strong internal pull down MOSFET.

Device Information

PART NUMBER	PACKAGE	BODY SIZE
HP3000	SOP-8L	4.90 × 3.90 mm^2
HP3000	DFN2X2-8L	2.00 × 2.00 mm^2

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REVISION HISTORY

Version	Date	Descriptions
Rev. 1.0	11/2023	Initial version

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

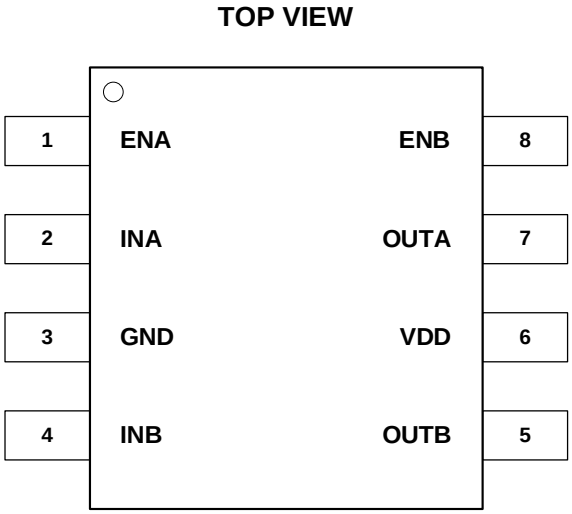


Figure 1 HP3000-AA000-SP08R Pin Assignment

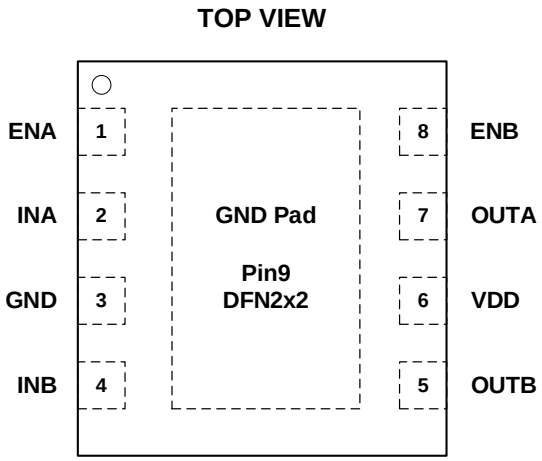


Figure 2 HP3000-AD000-HD08R Pin Assignment

Table 1. Pin Function Descriptions for HP3000-AA000-SP08R、HP3000-AD000-HD08R

Pin No.	Name	Type[1]	Primary Function
1	ENA	I	Enable input for Channel A. Biasing ENA, LOW will disable Channel A output regardless of the state of INA. Pulling ENA, HIGH enables the Channel A output. If ENA is left floating, Channel A is enabled by default due to an internal pull-up resistor. It is recommended to connect this pin to VDD if unused.
2	INA	I	Input to Channel A. INA is the non-inverting input of the HP3000 device. OUTA is held LOW if INA is unbiased or floating by default due to an internal pulldown resistor. Connect this pin to GND if unused.
3	GND	-	Ground: All signals are referenced to this pin.
4	INB	I	Input to Channel B. INB is the non-inverting input of the HP3000 device. OUTB is held LOW if INB is unbiased or floating by default due to an internal pulldown resistor. Connect this pin to GND if unused.
5	OUTB	O	Channel B Output
6	VDD	I	Bias supply input. Bypass this pin with two ceramic capacitors, generally ≥ 1 μF and 0.1 μF, which are referenced to GND pin of this device.

Pin No.	Name	Type[1]	Primary Function
7	OUTA	O	Channel A Output
8	ENB	I	Enable input for Channel B. Biasing ENB, LOW will disable Channel B output regardless of the state of INB. Pulling ENB, HIGH enables the Channel B output. If ENB is left floating, Channel B is enabled by default due to an internal pull-up resistor. It is recommended to connect this pin to VDD if unused.
9	Thermal Pad	-	Connect to GND through large copper plane. This pad is not a low-impedance path to GND

1. I = Input; O = Output

SPECIFICATIONS

V_{DD} = 12.0 V, T_J = −40°C to +150°C, 1-µF capacitor from V_{DD} to GND, no load on the output, for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2. Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
Operating Supply Voltage	V_{DD}		4.5	12	30	V
VDD quiescent supply current	I_{DD_Q}	V_{INx} = 3.3 V, VDD = 3.4 V, ENx = V_{DD}		260	500	µA
VDD static supply current	I_{DD}	V_{INx} = 3.3 V, ENx = V_{DD}		0.4	0.8	mA
		V_{INx} = 0.0 V, ENx = V_{DD}		0.35	0.7	mA
VDD operating current	I_{DDO}	fsw = 1000 kHz, VINx = 0.0 V to 3.3 V PWM, ENx = V_{DD}		3.6	4.2	mA
Shutdown current	I_{DD_SD}	V_{INx} = 3.3 V, ENx = 0 V		0.5	0.9	mA
UNDER VOLTAGE LOCKOUT (UVLO)						
VDD UVLO rising threshold	V_{DD_ON}		3.8	4.1	4.4	V
VDD UVLO falling threshold	V_{DD_OFF}		3.5	3.8	4.1	V
VDD UVLO hysteresis	V_{DD_HYST}			0.3		V
INPUT (INA, INB)						
Input signal high threshold	V_{INx_H}	Output High, ENx = HIGH	1.8	2	2.2	V
Input signal low threshold	V_{INx_L}	Output Low, ENx = HIGH	0.8	1	1.2	V
Input signal hysteresis	V_{INx_HYST}			1		V
Input pin pulldown resistor	R_{INx}	INx = 3.3 V		120		kΩ
ENABLE (ENA, ENB)						
Enable signal high threshold	V_{ENx_H}	Output High, INx = HIGH	1.8	2	2.2	V
Enable signal low threshold	V_{ENx_L}	Output Low INx = HIGH	0.8	1	1.2	V
Enable signal hysteresis	V_{ENx_HYST}			1		V
Enable pin pull-up resistor	R_{ENx}	ENx = 0 V		200		kΩ
OUTPUTS (OUTA, OUTB)						
Peak output source current	I_{SRC}	V_{DD} = 12 V, C_{VDD} = 10 µF, C_L = 0.1 µF, f = 1 kHz		5		A
Peak output sink current	I_{SNK}	V_{DD} = 12 V, C_{VDD} = 10 µF, C_L = 0.1 µF, f = 1 kHz		5		A
Pullup resistance	R_{CH}	I_{OUT} = –50 mA		0.8	1.32	Ω
Pulldown resistance	R_{CL}	I_{OUT} = 50 mA		0.6	1.15	Ω
Switching Characteristics						
Rise time	t_{Rx}	C_{LOAD} = 1.8 nF, 20% to 80%, Vin = 0 V to 3.3 V		7	13	ns
Fall time	t_{Fx}	C_{LOAD} = 1.8 nF, 80% to 20%, Vin = 0 V to 3.3 V		9	15	ns
Turn-on propagation delay	t_{D1x}	C_{LOAD} = 1.8 nF, V_{INx_H} of the input rise to 10% of output rise, Vin = 0 V to 3.3 V, f_{SW} = 500 kHz, 50% duty cycle, T_J = 125 °C		22	32	ns
Turn-off propagation delay	t_{D2x}	C_{LOAD} = 1.8 nF, V_{INx_L} of the input fall to 90% of output fall, Vin = 0 V to 3.3 V, f_{SW} = 500 kHz, 50% duty cycle, T_J = 125 °C		22	32	ns
Enable propagation delay	t_{D3x}	C_{LOAD} = 1.8 nF, V_{ENx_H} of the enable rise to 10% of output rise, V_{IN} = 0 V to 3.3 V, f_{sw} = 500 kHz, 50% duty cycle, T_J = 125 °C		22	32	ns

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Disable propagation delay	t_{D4x}	C_{LOAD} = 1.8 nF, V_{ENx_L} of the enable fall to 10% of output fall, Vin = 0 V to 3.3 V, f_{SW} = 500 kHz, 50% duty cycle, T_J = 125 °C		22	32	ns
Delay matching between two channels	t_M	C_{LOAD} = 1.8 nF, V_{IN} = 0 V to 3.3 V, f_{SW} = 500 kHz, 50% duty cycle, INA = INB, $\|t_{RA} - t_{RB}\|$, $\|t_{FA} - t_{FB}\|$		1	2	ns
Minimum input pulse width	t_{PWmin}	C_{LOAD} = 1.8 nF, V_{IN} = 0 V to 3.3 V, f_{SW} = 500 kHz, V_O > 1.5 V		10	15	ns

1 Legend:
A = Analog Pin
P = Power Pin
D = Digital Pin
I = Input Pin
O = Output Pin

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute maximum ratings

Parameter	Rating
Supply voltage, VDD (Continuous)	35 V
Output voltage, OUTA, OUTB (DC)	-0.3 V to VDD + 0.3 V
Output voltage, OUTA, OUTB (200ns Pulse)	-2 V to VDD + 3 V
Input voltage INA, INB, ENA, ENB	-12 V to 35 V
Operating temperature range (junction)	−40°C to +150°C
Soldering conditions	JEDEC J-STD-020
Electrostatic Discharge (ESD)	
Human body model	±2000 V
Changed device model	±1000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

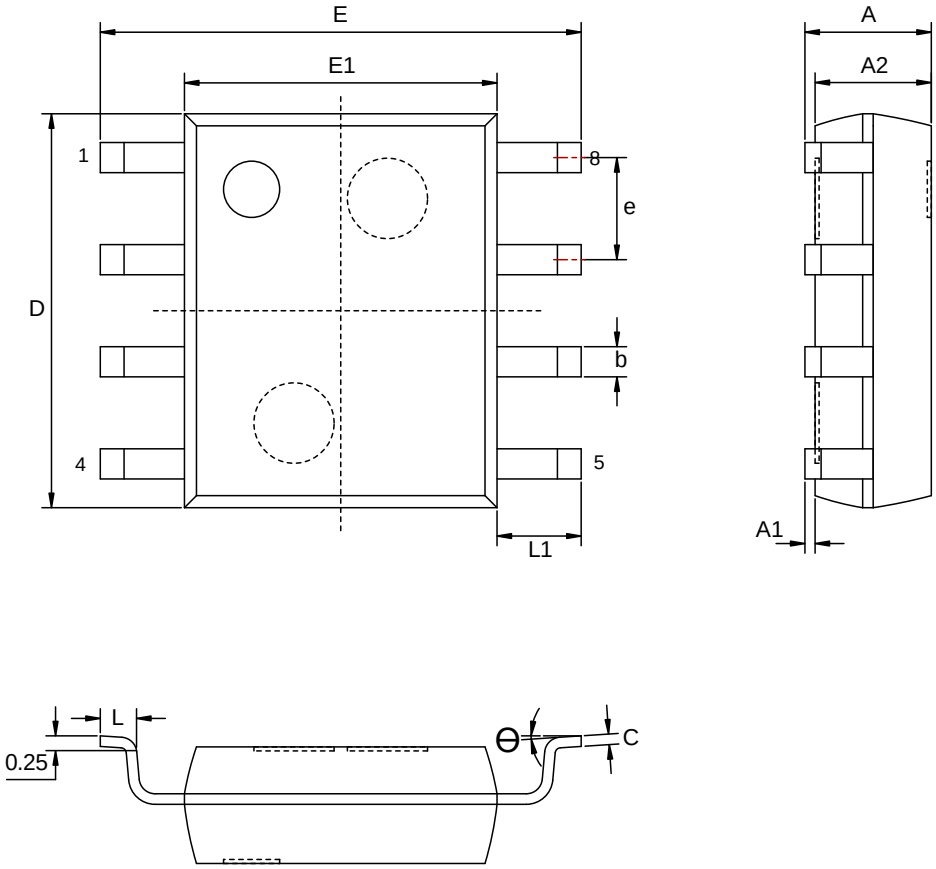
Package Type	θ_{JA}	θ_{JC}	Unit
8-lead SOP	133.9	59.7	°C/W
8-lead DFN2x2-8L	92	74.5	°C/W

ESD CAUTION

Electrostatic Discharge Sensitive Device.

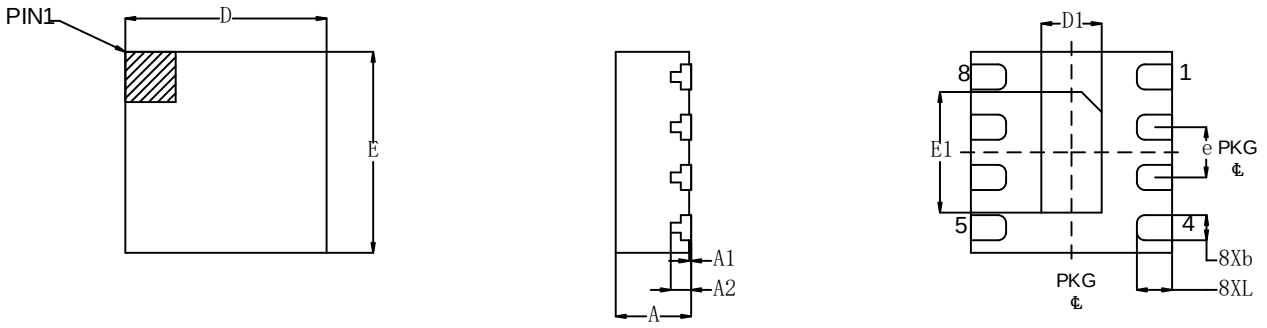
Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE OUTLINE DIMENSIONS



SYMBOLS	DIMENSION IN MILLIMETERS		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.25
A2	1.35	1.45	1.55
b	0.30	-	0.51
C	0.17	-	0.25
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	-	1.27
θ	0°	-	8°

Figure 2 HP3000-AA000-SP08R Dimension

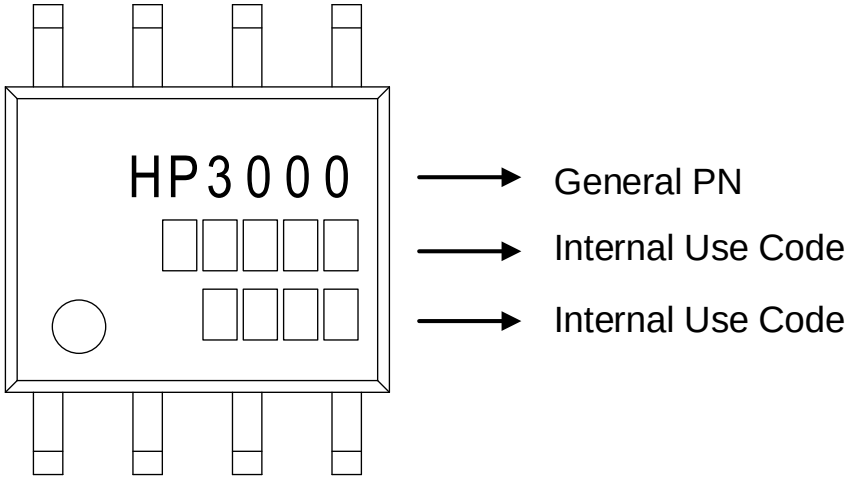


TOP VIEW SIDE VIEW BOTTOM VIEW

	DIMENSION IN MILLIMETERS		
SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.203 REF		
b	0.20	0.25	0.30
D	2 BSC		
E	2 BSC		
e	0.5 BSC		
L	0.30	0.35	0.40
D1	0.55	0.60	0.65
E1	1.15	1.20	1.25

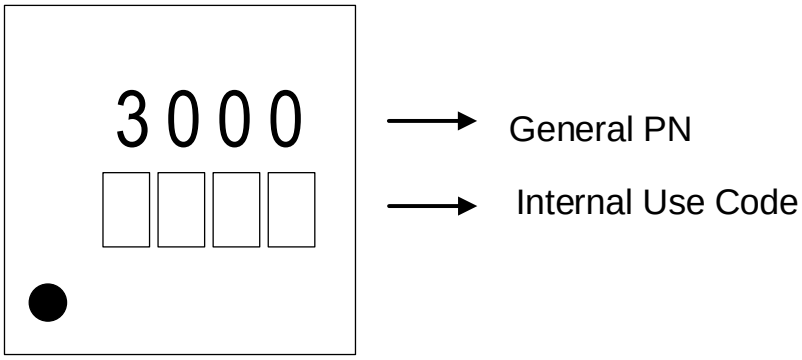
Figure 3 HP3000-AD000-HD08R Dimension

PACKAGE TOP MARKING



SOP 8L

Figure 4 HP3000-AA000-SP08R Package Top Marking



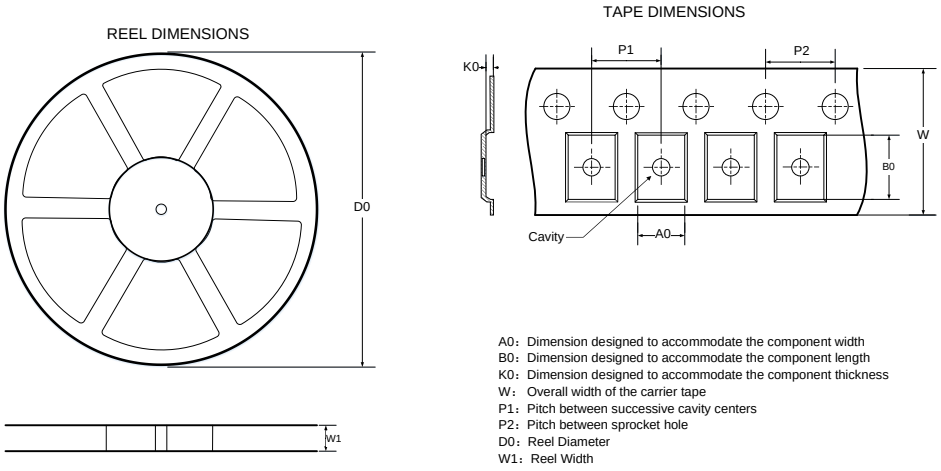
DFN2X2-8L

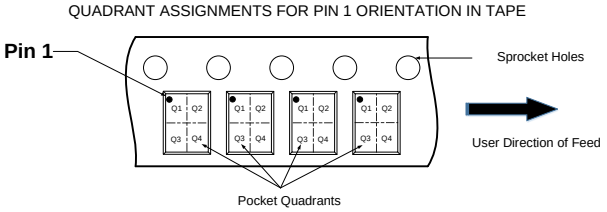
Figure 5 HP3000-AD000-HD08R Package Top Marking

ORDERING GUIDE

Model	Package Type	Tj Temp (℃)	MSL	Package	Package Qty
HP3000-AA000-SP08R	SOP8L	-40~150	Level 2	T&R	4000ea
HP3000-AD000-HD08R	DFN2×2-8L	-40~150	Level 1	T&R	4000ea

TAPE AND REEL INFORMATION





DIMENSIONS AND PIN1 ORIENTATION

Device	Package Type	D0 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant	Quantity
HP3000-AAXXX-SP08R	SOP8L	330.00	12.40	6.40	5.40	2.10	8.00	4.00	12.00	Q1	4000
HP3000-ADXXX-HD08R	DFN2X2-8L	180.00	9.50	2.30	2.30	1.10	4.00	4.00	8.00	Q2	4000

All dimensions are nominal

Figure 6 Tape and Reel Information

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