



24C16 (LX) I²C-Compatible Serial E²PROM

Product Specification

Specification Revision History :

Version	Date	Description
2022-01-A4	2022-01	New-made



1、General Description

The 24C16 is 16-Kbit I²C-compatible Serial EEPROM (Electrically Erasable Programmable Memory) device. It contains a memory array of 2048 × 8bits, which is organized in 16 -byte per page. The device is used in low-voltage and low-power systems.

Features:

- Single Supply Voltage and High Speed
 - Minimum operating voltage down to 1.7V
 - 1 MHz clock from 2.5V to 5.5V
 - 400kHz clock from 1.7V to 2.5V
- Low power CMOS technology
 - Read current 1.0mA, maximum
 - Write current 2.0mA, maximum
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Sequential & Random Read Features
- Page Write Modes, Partial Page Writes Allowed
- Write protect of the whole memory array
- Self-timed Write Cycle (5ms maximum)
- High Reliability
 - Endurance: > 1 Million Write Cycles
 - Data Retention: > 100 Years
- LATCH UP Capability: +/- 200mA
- Package: DIP8, SOP8, TSSOP8



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Shenzhen Lingxing Microelectronics Technology Co., Ltd.

版次: B1

编号: 24C16-LX-A016

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
24C16(LX)	DIP8	24C16	50 PCS/tube	40 tube/box	2000 PCS/box	Dimensions of plastic enclosure: 9.2mm×6.4mm Pin spacing: 2.54mm
24C16(LX)	SOP8	24C16	100 PCS/tube	100 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 4.9mm×3.9mm Pin spacing: 1.27mm

Reel packing specifications:

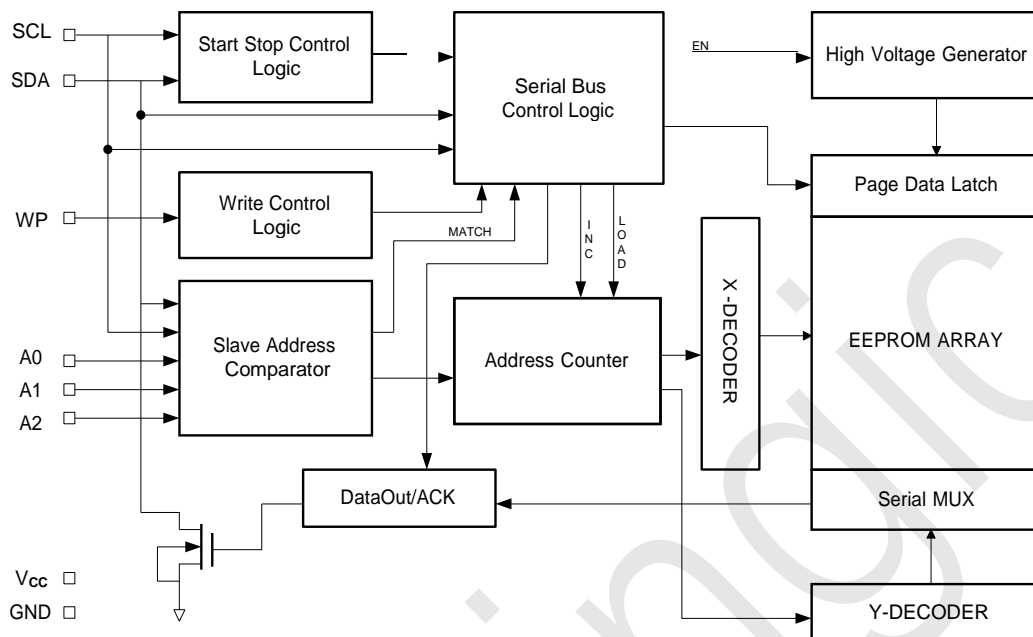
Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
24C16(LX)	SOP8	24C16	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 4.9mm×3.9mm Pin spacing: 1.27mm
24C16(LX)	TSSOP8	24C16	3000PCS/reel	3000PCS/box	Dimensions of plastic enclosure: 3.0mm×3.0mm Pin spacing: 0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

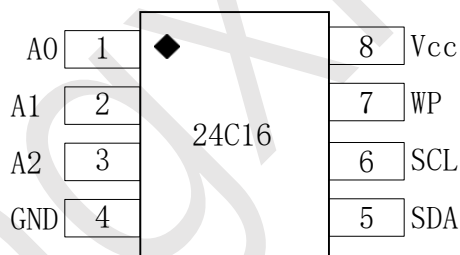


2、Block Diagram And Pin Description

2.1 、Block Diagram



2.2 、Pin Configurations



2.3 、Pin Description

Pin No.	Pin Name	Description
1	A0	Not connected
2	A1	Not connected
3	A2	Not connected
4	GND	Ground
5	SDA	Serial Data Input and Serial Data Output
6	SCL	Serial Clock Input
7	WP	Write Control, Low Enable Write
8	Vcc	Power



2.4 、 Pin Descriptions

Serial Clock (SCL): The SCL input is used to positive-edge clock data in and negative-edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wire-Ored with any number of other open-drain or open-collector devices.

Device Addresses (A2, A1, A0): The A2, A1 and A0 pins are device address inputs. Typically, the A2, A1 and A0 pins are for hardware addressing and a total of 8 devices can be connected on a single bus system. If these pins are left floating, the A2, A1 and A0 pins will be internally pulled down to GND.

Write Control (WP): The Write Control input, when WP is connected directly to V_{CC} , all write operations to the memory are inhibited. When connected to GND, allows normal write operations. If the pin is left floating, the WP pin will be internally pulled down to GND.

3、 Electrical Parameter

3.1 、 Absolute Maximum Ratings

($T_{amb}=25^{\circ}C$, All voltage referenced to GND, unless otherwise specified)

Characteristic	Symbol	Conditions		Value	Unit
Power Supply Voltage	V_{CC}	-		6.25	V
Voltage on Any Pin with Respect to Ground	V	-		-1.0 to +7.0	V
DC Output Current	I	-		5.0	mA
Input/Output Capacitance (SDA)	$C_{I/O}$	$f=1.0MHz$, $V_{CC}=5V$, $V_{I/O}=GND$		8	pF
Input Capacitance (E0,E1,E2,WP,SCL)	C_{IN}	$f=1.0MHz$, $V_{CC}=5V$, $V_{IN}=GND$		6	pF
Operating Temperature	T_{amb}	-		-40 to +85	$^{\circ}C$
Storage Temperature	T_{stg}	-		-65 to +150	$^{\circ}C$
Soldering Temperature	T_L	10s	DIP	245	$^{\circ}C$
			SOP	250	

Notes:

[1] This parameter is ensured by characterization not 100% tested

[2]Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



3.2、Electrical Characteristics

3.2.1、DC Characteristics

($T_{amb}=-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC}=+1.8\text{V}$ to $+5.5\text{V}$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	-	1.7	-	5.5	V
Standby Current	I_{sb}	$V_{CC}=3.3\text{V}$, $T_{amb}=85^{\circ}\text{C}$	-	-	1.0	μA
		$V_{CC}=5.5\text{V}$, $T_{amb}=85^{\circ}\text{C}$	-	-	3.0	μA
Supply Current	I_{CC1}	$V_{CC}=5.5\text{V}$, Read at 400Khz	-	-	1.0	mA
Supply Current	I_{CC2}	$V_{CC}=5.5\text{V}$, Write at 400Khz	-	-	2.0	mA
Input Leakage Current	I_{LI}	$V_{IN}=V_{CC}$ or GND	-	0.10	1.0	μA
Output Leakage Current	I_{LO}	$V_{OUT}=V_{CC}$ or GND	-	0.05	1.0	μA
Input Low Level	V_{IL}	-	-0.6	-	$0.3V_{CC}$	V
Input High Level	V_{IH}	-	$0.7V_{CC}$	-	$V_{CC}+0.5$	V
Output Low Level	V_{OL1}	$V_{CC}=1.7\text{V}$ (SDA) $I_{OL}=1.5\text{ mA}$	-	-	0.2	V
Output Low Level	V_{OL2}	$V_{CC}=3.0\text{V}$ (SDA) $I_{OL}=2.1\text{ mA}$	-	-	0.4	V

Notes: [1] This parameter is ensured by characterization not 100% tested

3.2.2、AC Characteristics

($T_{amb}=-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC}=+1.8\text{V}$ to $+5.5\text{V}$, $C_L=1\text{ TTL Gate}$ and 100pF , unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock Frequency, SCL	f_{SCL}	$V_{CC}=1.7\text{V}$	-	-	400	kHz
		$V_{CC}=2.7\text{V}$	-	-	1000	
		$V_{CC}=5.0\text{V}$	-	-	1000	
Clock Pulse Width Low	t_{LOW}	$V_{CC}=1.7\text{V}$	1.3	-	-	μs
		$V_{CC}=2.7\text{V}$	0.4	-	-	
		$V_{CC}=5.0\text{V}$	0.4	-	-	
Clock Pulse Width High	t_{HIGH}	$V_{CC}=1.7\text{V}$	0.6	-	-	μs
		$V_{CC}=2.7\text{V}$	0.4	-	-	
		$V_{CC}=5.0\text{V}$	0.4	-	-	
Noise Suppression Time	t_I	$V_{CC}=1.7\text{V}$	-	-	100	ns
		$V_{CC}=2.7\text{V}$	-	-	50	
		$V_{CC}=5.0\text{V}$	-	-	50	
Clock Low to Data Out Valid	t_{AA}	$V_{CC}=1.7\text{V}$	0.05	-	0.9	μs
		$V_{CC}=2.7\text{V}$	0.05	-	0.55	
		$V_{CC}=5.0\text{V}$	0.05	-	0.55	
Time the bus must be free before a new transmission can start	t_{BUF}	$V_{CC}=1.7\text{V}$	1.3	-	-	μs
		$V_{CC}=2.7\text{V}$	0.5	-	-	
		$V_{CC}=5.0\text{V}$	0.5	-	-	
Start Hold Time	$t_{HD,STA}$	$V_{CC}=1.7\text{V}$	0.6	-	-	μs
		$V_{CC}=2.7\text{V}$	0.25	-	-	
		$V_{CC}=5.0\text{V}$	0.25	-	-	
Start Setup Time	$t_{SU,STA}$	$V_{CC}=1.7\text{V}$	0.6	-	-	μs
		$V_{CC}=2.7\text{V}$	0.25	-	-	
		$V_{CC}=5.0\text{V}$	0.25	-	-	



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Data In Hold Time	$t_{HD.D}$	$V_{CC}=1.7V$	0	-	-	us
		$V_{CC}=2.7V$	0	-	-	
		$V_{CC}=5.0V$	0	-	-	
Data In Setup Time	$t_{SU.D}$	$V_{CC}=1.7V$	100	-	-	ns
		$V_{CC}=2.7V$	100	-	-	
		$V_{CC}=5.0V$	100	-	-	
Inputs Rise Time ^[1]	t_R	$V_{CC}=1.7V$	-	-	300	ns
		$V_{CC}=2.7V$	-	-	300	
		$V_{CC}=5.0V$	-	-	300	
Inputs Fall Time ^[1]	t_F	$V_{CC}=1.7V$	-	-	300	ns
		$V_{CC}=2.7V$	-	-	300	
		$V_{CC}=5.0V$	-	-	100	
Stop Setup Time	$t_{SU.STO}$	$V_{CC}=1.7V$	0.6	-	-	us
		$V_{CC}=2.7V$	0.25	-	-	
		$V_{CC}=5.0V$	0.25	-	-	
Data Out Hold Time	t_{DH}	$V_{CC}=1.7V$	50	-	-	ns
		$V_{CC}=2.7V$	50	-	-	
		$V_{CC}=5.0V$	50	-	-	
WP pin Setup Time	$t_{SU.WP}$	$V_{CC}=1.7V$	1.2	-	-	us
		$V_{CC}=2.7V$	0.6	-	-	
		$V_{CC}=5.0V$	0.6	-	-	
WP pin Hold Time	$t_{HD.WP}$	$V_{CC}=1.7V$	1.2	-	-	us
		$V_{CC}=2.7V$	0.6	-	-	
		$V_{CC}=5.0V$	0.6	-	-	
Write Cycle Time	t_{WR}	$V_{CC}=1.7V$	-	-	5	ms
		$V_{CC}=2.7V$	-	-	5	
		$V_{CC}=5.0V$	-	-	5	
Endurance	EDR	3.3V, Page mode	1,000,000	-	-	Write cycles
Data retention	DRET	-	100	-	-	Years

Note: [1] This parameter is ensured by characterization and is not 100% tested



4、Function Description

4.1、Device Operation

4.1.1、Data Input

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 4-1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

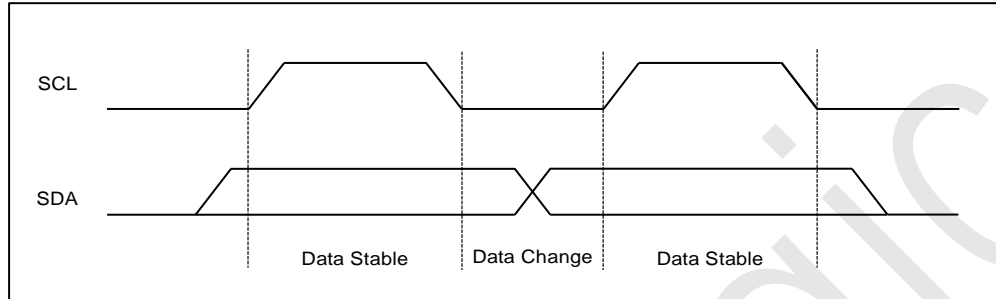


Figure 4-1

4.1.2、Start Condition

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 4-2).

4.1.3、Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the 24C16 in a standby power mode (see Figure 4-2)

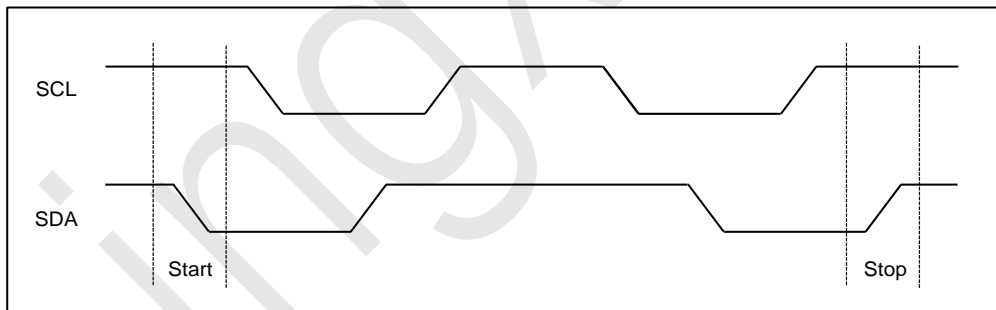


Figure 4-2



4.1.4 、 Acknowledge (ACK)

All addresses and data words are serially transmitted to and from the 24C16 in 8-bit words. The 24C16 sends a “0” to acknowledge that it has received each word. This happens during the ninth clock cycle(see to Figure 4-3).

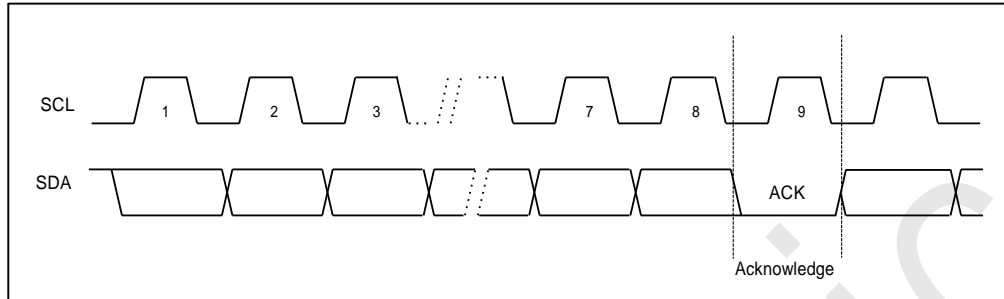


Figure 4-3

4.1.5 、 Standby Mode

The 24C16 features a low-power standby mode which is enabled: (a) after a fresh power up, (b) after receiving a STOP bit in read mode, and (c) after completing a self-time internal programming operation.

4.1.6 、 Soft Reset

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps: (a) Create a start condition, (b) Clock nine cycles, and (c) create another start bit followed by stop bit condition, as shown below. The device is ready for the next communication after the above steps have been completed(see to Figure 4-4).

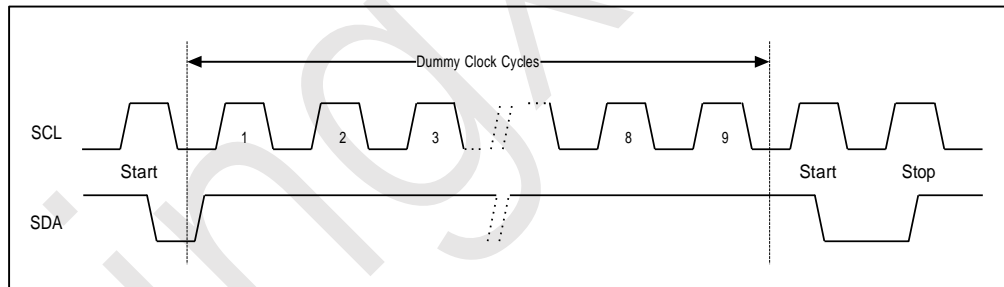


Figure 4-4



4.1.7 、 Bus Timing(see to Figure 4-5).

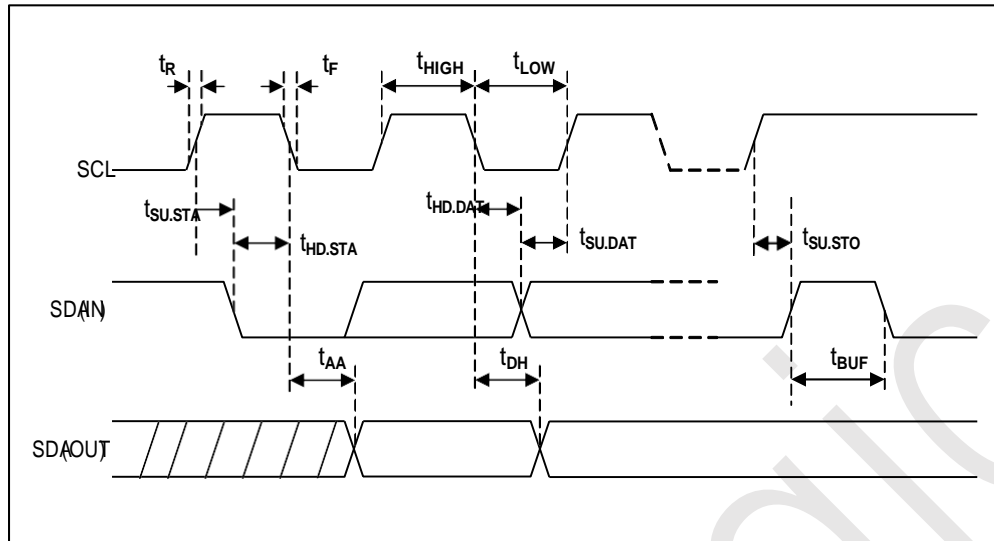


Figure 4-5

4.1.8 、 Write Cycle Timing(see to Figure 4-6)

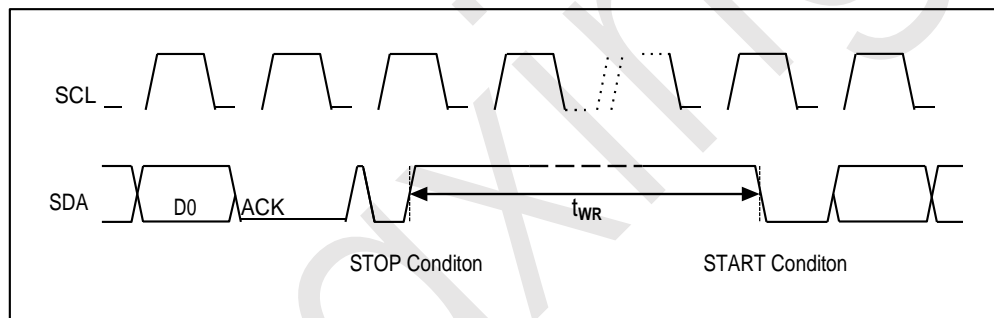


Figure 4-6

4.2 、 Device Addressing

The 24C16 requires an 8-bit device address word following a start condition to enable the chip for a read or write operation. The device address word consists of a mandatory one-zero sequence for the first four most-significant bits.

MSB				LSB			
1	0	1	0	A2 (B10)	A1 (B9)	A0 (B8)	R/W

The A2, A1 and A0 device address bits can be used as the upper three bits of the data word address.. The A2, A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are floating.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. Upon a compare of the device address, the Chip will output a zero. If a compare is not made, the device will return to a standby state.

MSB				LSB			
B7	B6	B5	B4	B3	B2	B1	B0



4.3 、Data Security

24C16 has a hardware data protection scheme that allows the user to write protect the whole memory when the WP pin is at Vcc.

4.4 、Write Operations

4.4.1、Byte Write

A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the 24C16 will again respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the 24C16 will output a “0” and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. And then the 24C16 enters an internally timed write cycle, all inputs are disabled during this write cycle and the 24C16 will not respond until the write is complete (see Figure 4-7).

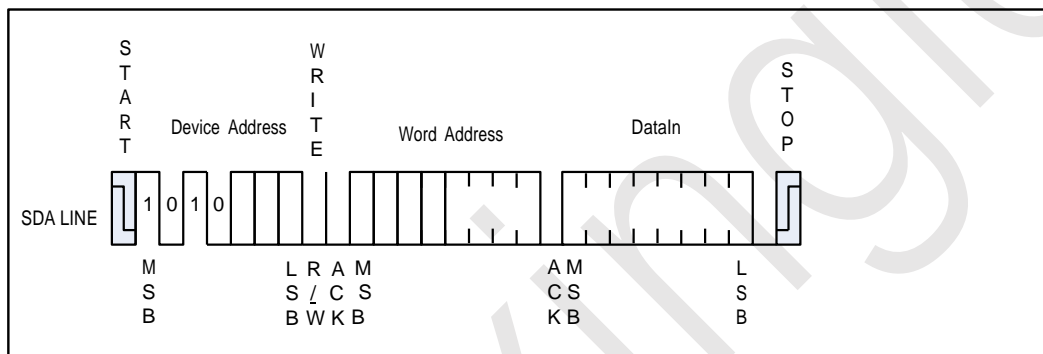


Figure 4-7

4.4.2 、Page Write

A page write is initiated the same as a byte write, but the master does not send a stop condition after the first data word is clocked in. Instead, after the 24C16 acknowledges receipt of the first data word, the master can transmit more data words. The 24C16 will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 4-8).

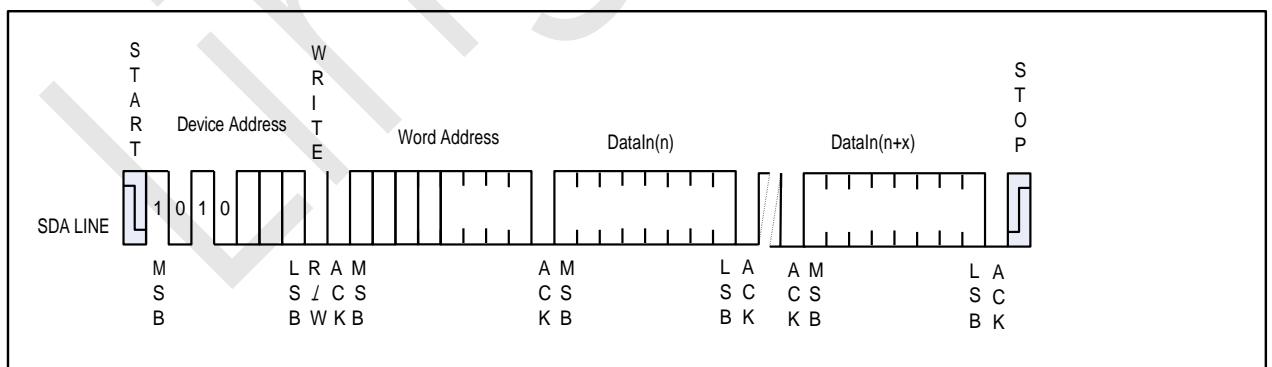


Figure 4-8

The lower four bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 16 data words are transmitted to the 24C16, the data word



address will roll-over, and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

4.4.3 、 Acknowledge Polling

Once the internally timed write cycle has started and the 24C16 inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the 24C16 respond with a “0”, allowing the read or write sequence to continue.

4.5 、 Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to “1”. There are three read operations: Current Address Read; Random Address Read and Sequential Read.

4.5.1 、 Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to “1” is clocked in and acknowledged by the 24C16, the current address data word is serially clocked out. The microcontroller does not respond with an input “0” but does generate a following stop condition (see Figure 4-9).

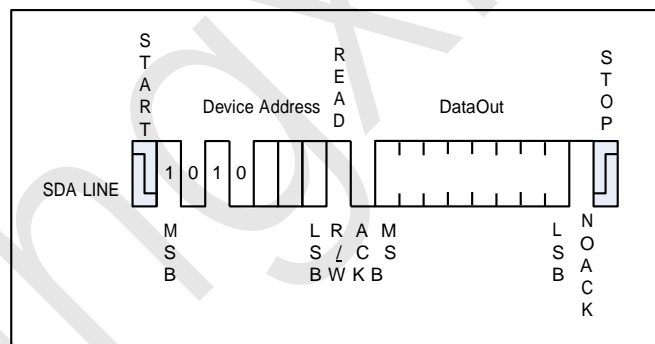


Figure 4-9

4.5.2 、 Random Read

A Random Read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the 24C16, the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The 24C16 acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 4-10).

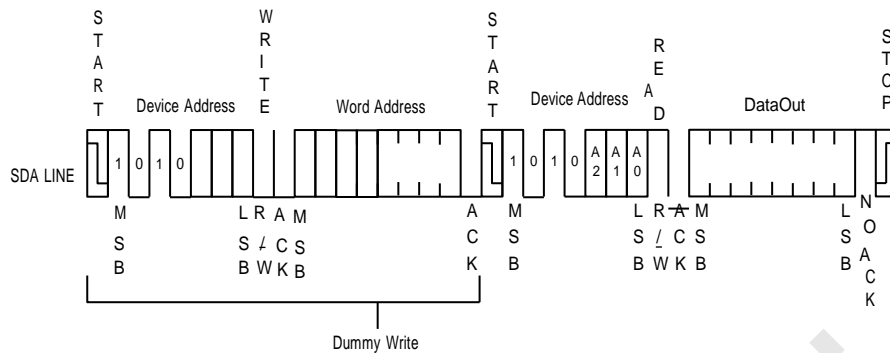


Figure 4-10

4.4.3、Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with acknowledge. As long as the 24C16 receives acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 4-11)

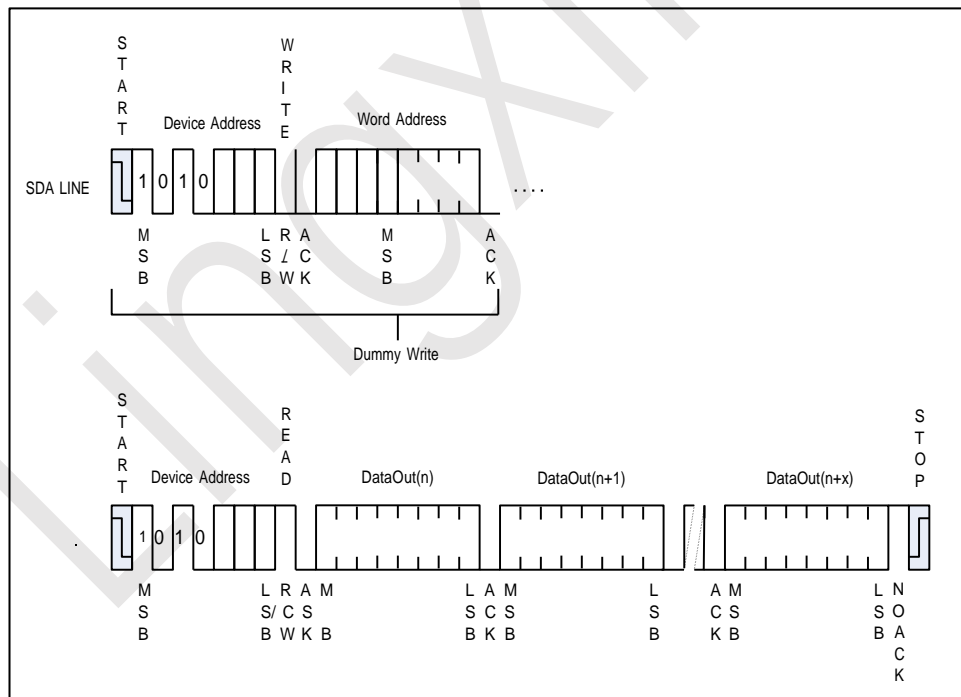
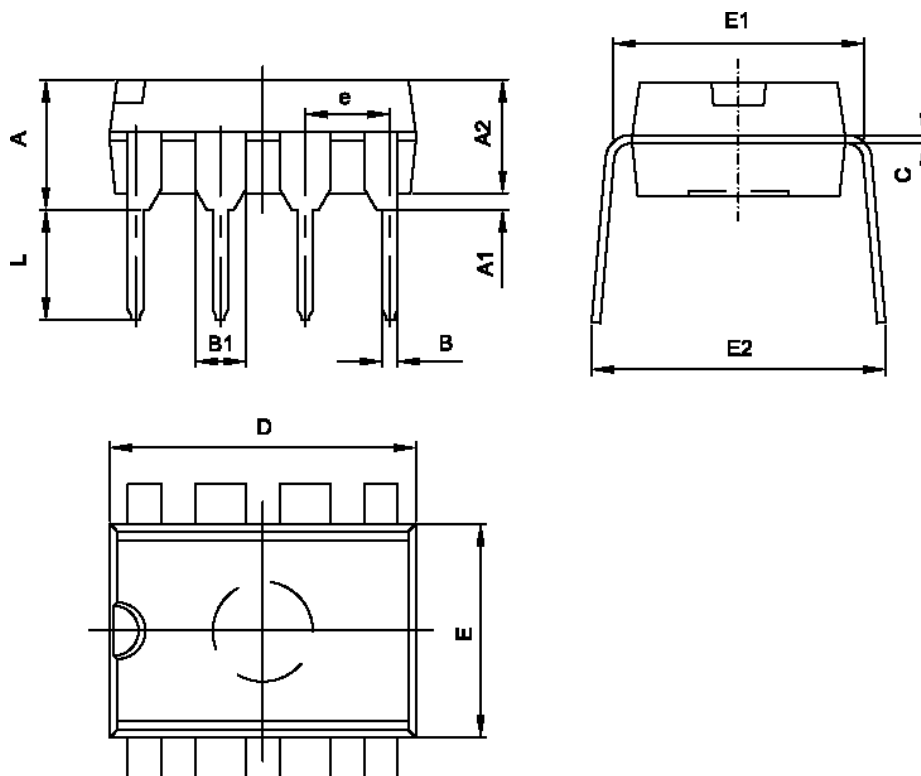


Figure 4-11



5、Package Information

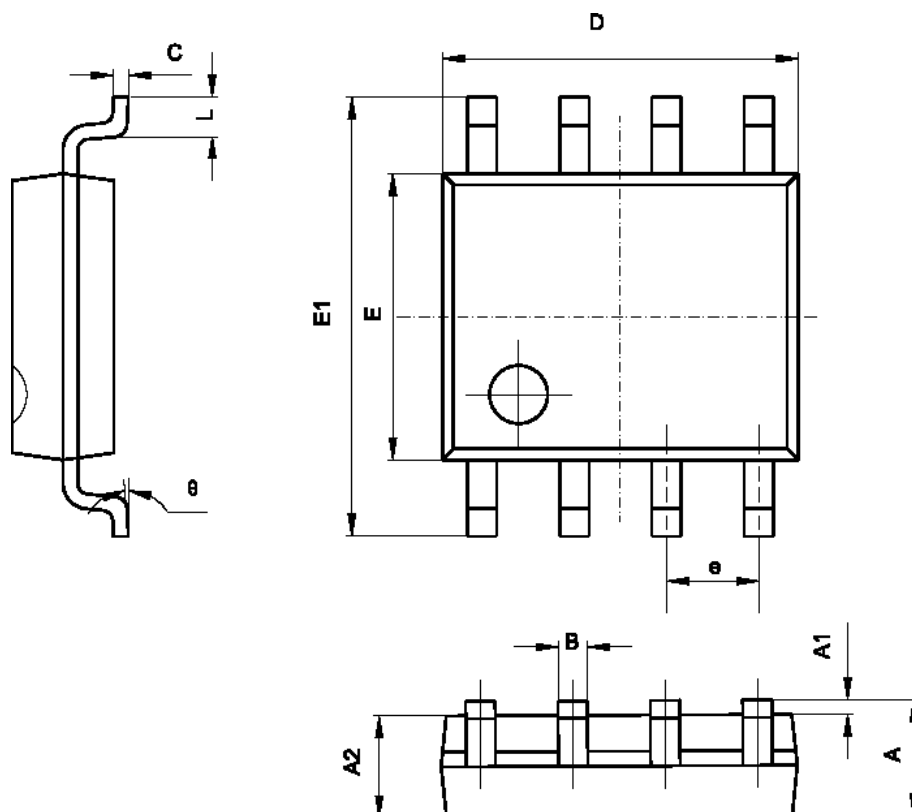
5.1、DIP8



Symbol	Dimension In Millimeters		Dimension In Inches	
	Min	Max	Min	Max
A	3.610	4.310	0.142	0.170
A1	0.510		0.020	
A2	3.100	3.600	0.122	0.142
B	0.360	0.560	0.014	0.022
B1	1.524(TYP)		0.060(TYP)	
C	0.200	0.360	0.008	0.014
D	9.000	9.500	0.354	0.374
E	6.100	6.600	0.240	0.260
E1	7.620(TYP)		0.300(TYP)	
e	2.540(TYP)		0.100(TYP)	
L	3.000	3.600	0.118	0.142
E2	8.200	9.400	0.323	0.370



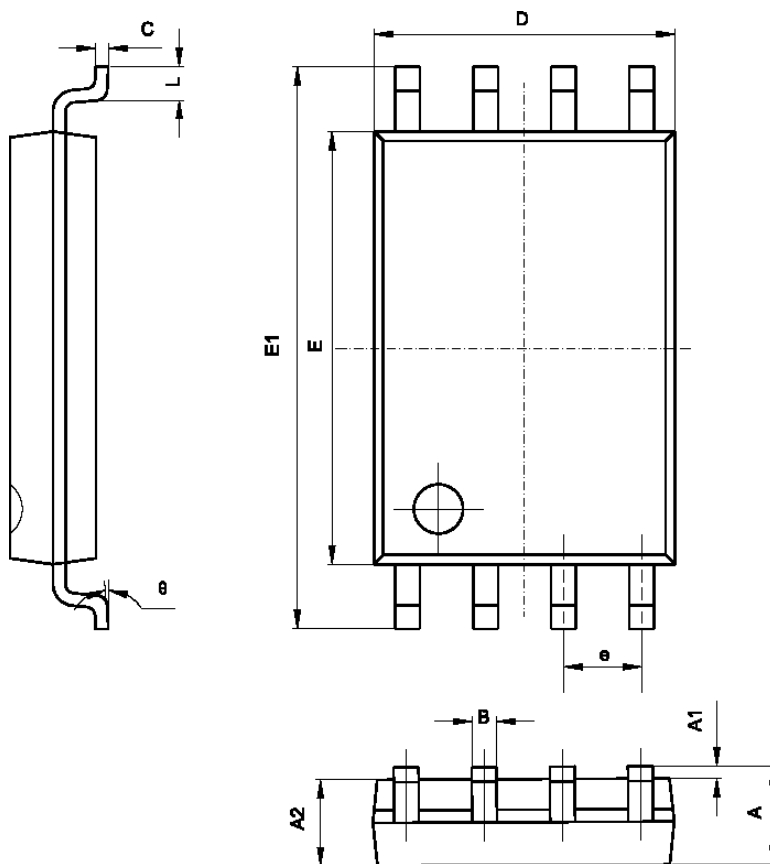
5.2、SOP8



Symbol	Dimension In Millimeters		Dimension In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.170	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270(TYP)		0.050(TYP)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



5.3、TSSOP8



Symbol	Dimension In Millimeters		Dimension In Inches	
	Min	Max	Min	Max
A	1.1 MAX TYP		0.043 MAX TYP	
A1	0.050	0.150	0.002	0.006
A2	0.850	0.950	0.033	0.037
B	0.190	0.300	0.007	0.012
C	0.090	0.200	0.004	0.008
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.224	0.260
e	0.650 (TYP)		0.026 (TYP)	
L	0.500	0.700	0.020	0.028
θ	1°	7°	1°	7°



6、Statements And Notes

6.1 、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2 、Notion

Recommended carefully reading this information before the use of this product;

The information in this document are subject to change without notice;

This information is using to the reference only, the company is not responsible for any loss;

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.