

## 1. DESCRIPTION

The XL75176AD/XL75176AP differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus-transmission lines.

The XL75176AD/XL75176AP combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or  $V_{CC} = 0$ . These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 k $\Omega$ , an input sensitivity of  $\pm 200$  mV, and a typical input hysteresis of 50 mV.

The XL75176AD/XL75176AP is characterized for operation from -40°C to 85°C.

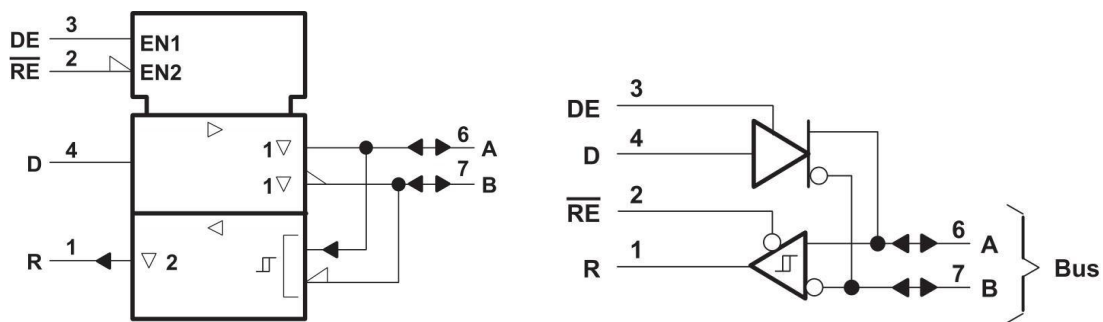
## 2. FEATURES

- Bidirectional Transceiver
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability  $\pm 60$  mA Max
- Thermal-Shutdown Protection
- CAN bus communication speed up to 1 Mbps
- Driver Positive-Current Limiting and Negative-Current Limiting
- Receiver Input Impedance 12 k $\Omega$  Min
- Receiver Input Sensitivity  $\pm 200$  mV
- Receiver Input Hysteresis 50 mV Typ
- Operates From Single 5-V Supply
- Package option: XL75176AD (SOP8), XL75176AP (DIP8)

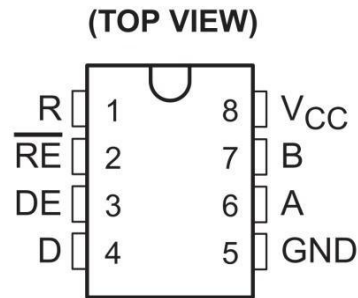
### 3. APPLICATIONS

- Low Speed RS485 communication (5 Mbps or less)
- For 10 Mbps, use XL75176AD/XL75176AP

### 4. SIMPLIFIED SCHEMATICS



## 5. PIN CONFIGURATIONS AND FUNCTIONS



PIN		TYPE	DESCRIPTION
NAME	NO.		
R	1	O	Logic Data Output from RS-485 Receiver
$\overline{\text{RE}}$	2	I	Receive Enable (active low)
DE	3	I	Driver Enable (active high)
D	4	I	Logic Data Input to RS-485 Driver
GND	5	—	Device Ground Pin
A	6	I/O	RS-422 or RS-485 Data Line
B	7	I/O	RS-422 or RS-485 Data Line
V <sub>CC</sub>	8	—	Power Input. Connect to 5-V Power Source.

## 6. SPECIFICATIONS

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply Voltage <sup>(2)</sup>		7	V
	Voltage range at any bus terminal	-10	15	V
V <sub>I</sub>	Enable input voltage		5.5	V
	Continuous Total power Dissipation	See Table 1		
T <sub>A</sub>	Operating free-air temperature range	-40	85	°C
T <sub>stg</sub>	Storage temperature range	65	150	°C

- [1] Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- [2] All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±XXX
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±YYY
			V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommend Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V <sub>CC</sub>	Supply Voltage	4.75	5	5.25	V
V <sub>I</sub> or V <sub>IC</sub>	Voltage at any buss terminal (separately or common mode)	-7		12	V
V <sub>IH</sub>	High-level input voltage	D, DE, and $\overline{RE}$		2	V
V <sub>IL</sub>	Low-level input voltage	D, DE, and $\overline{RE}$		0.8	V
V <sub>ID</sub>	Differential input voltage <sup>(1)</sup>			±12	V
I <sub>OH</sub>	High-level output current	Driver		-60	mA
		Receiver		-400	μA
I <sub>OL</sub>	Low-level output current	Driver		60	mA
		Receiver		8	mA
T <sub>A</sub>	Operating free-air temperature	0		70	°C

- (1) Differential-input/output bus voltage is measured at the non-inverting terminal A with respect to the inverting terminal B.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN75176A		UNIT	
	D	P		
	8 PINS	8 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	172	113	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

**Table 1. Dissipation Rating Table**

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1100 mW	8.8 mW/°C	704 mW

## 6.5 Electrical Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IK}$	Input clamp voltage	$I_I = -18 \text{ mA}$			-1.5	V
$V_{OH}$	High-level output voltage	$V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -33 \text{ mA}$		3.7		V
$V_{OL}$	Low-level output voltage	$V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = 33 \text{ mA}$		1.1		V
$ V_{OD1} $	Differential output voltage	$I_O = 0$			$2V_{OD2}$	V
$ V_{OD2} $	Differential output voltage	$RL = 100 \Omega$ , see Figure 8	2	2.7		V
		$RL = 54 \Omega$ , see Figure 8	1.5	2.4		
$\Delta V_{OD} $	Change in magnitude of differential output voltage <sup>(2)</sup>				$\pm 0.2$	V
$V_{OC}$	Common-mode output voltage <sup>(3)</sup>	$RL = 54 \Omega$ or $100 \Omega$ , see Figure 8			3	V
$\Delta V_{OC} $	Change in magnitude of common-mode output voltage <sup>(2)</sup>				$\pm 0.2$	V
$I_O$	Output current	Output disabled <sup>(4)</sup>	$V_O = 12 \text{ V}$		1	mA
			$V_O = -7 \text{ V}$		-0.8	
$I_{IH}$	High-level input current	$V_I = 2.4 \text{ V}$			20	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_I = 0.4 \text{ V}$			-400	$\mu\text{A}$
$I_{OS}$	Short-circuit output current	$V_O = -7 \text{ V}$			-250	mA
		$V_O = V_{CC}$			250	
		$V_O = 12 \text{ V}$			500	
$I_{CC}$	Supply current (total package)	No load	Outputs enabled	35	50	mA
			Outputs disabled	26	40	

(1) All typical values are at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .

(2)  $\Delta|V_{OD}|$  and  $\Delta|V_{OC}|$  are the changes in magnitude of  $V_{OD}$  and  $V_{OC}$  respectively, that occur when the input is changed from a high level to a low level.

(3) In ANSI Standard EIA/TIA-422-B,  $V_{OC}$ , which is the average of the two output voltages with respect to GND, is called output offset voltage,  $V_{OS}$ .

(4) This applies for both power on and off; refer to ANSI Standard EIA/TIA-422-B for exact conditions.

## 6.6 Electrical Characteristics - Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IT+}$	Positive-going input threshold voltage	$V_O = 2.7 \text{ V}, I_O = -0.4 \text{ mA}$			0.2	V
$V_{IT-}$	Negative-going input threshold voltage	$V_O = 0.5 \text{ V}, I_O = 8 \text{ mA}$		-0.2		V
$V_{hys}$	Input hysteresis voltage ( $V_{IT+} - V_{IT-}$ )			5 0		mV
$V_{IK}$	Enable clamp voltage	$I_I = -18 \text{ mA}$			-1.5	V
$V_{OH}$	High-level output voltage	$V_{ID} = 200 \text{ mV}, I_{OH} = -400 \mu\text{A}$ See Figure 9		2.7		V
$V_{OL}$	Low-level output voltage	$V_{ID} = 200 \text{ mV}, I_{OH} = 8 \text{ mA}$ See Figure 9			0.45	V
$I_{OZ}$	High-impedance-state output current	$V_O = 0.4 \text{ V to } 2.4 \text{ V}$			$\pm 20$	$\mu\text{A}$
$I_I$	Line input current	Other input = $0 \text{ V}^{(2)}$	$V_I = 12 \text{ V}$		1	mA
			$V_I = -7 \text{ V}$		-0.8	
$I_{IH}$	High-level enable input current	$V_{IH} = 2.7 \text{ V}$			20	$\mu\text{A}$
$I_{IL}$	Low-level enable input current	$V_{IL} = 0.4 \text{ V}$			-100	$\mu\text{A}$
$r_i$	Input resistance			12		$\text{k}\Omega$
$I_{OS}$	Short-circuit output current		-15		-85	mA
$I_{CC}$	Supply current (total package)	No load	Outputs enabled	35	50	mA
			Outputs disabled	26	40	

(1) All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(2) This applies for both power on and power off. Refer to ANSI Standard EIA/TIA-422-B for exact conditions.

### 6.7 Switching Characteristics - Driver

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$ Differential-output delay time	$R_L = 60\ \Omega$ , See Figure 10		40	60	ns
$t_{t(OD)}$ Differential-output transition time			65	95	ns
$t_{pZH}$ Output enable time to high level	$R_L = 110\ \Omega$ , See Figure 11		55	90	ns
$t_{pZL}$ Output enable time to low level	$R_L = 110\ \Omega$ , See Figure 12		30	50	ns
$t_{pHZ}$ Output disable time form high level	$R_L = 110\ \Omega$ , See Figure 11		85	130	ns
$t_{pLZ}$ Output disable time from low level	$R_L = 110\ \Omega$ , See Figure 12		20	40	ns

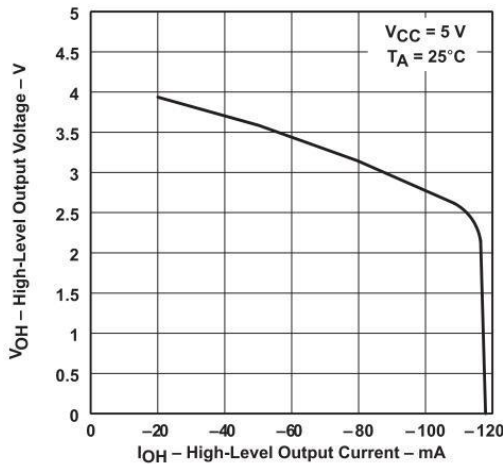
### 6.8 Switching Characteristics - Receiver

$V_{CC} = 5\text{ V}$ ,  $C_L = 15\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

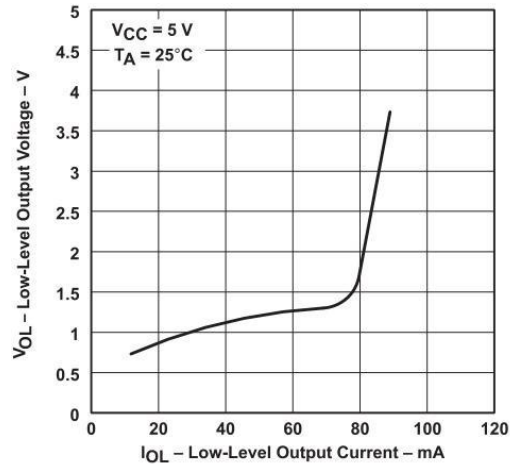
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low-to-high-level output	$V_{ID} = -1.5\text{ V to }1.5\text{ V}$ , See Figure 13		21	35	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output			23	35	ns
$t_{pZH}$ Output enable time to high level	See Figure 14		10	30	ns
$t_{pZL}$ Output enable time to low level			12	30	ns
$t_{pHZ}$ Output disable time from high level	See Figure 14		20	35	ns
$t_{pLZ}$ Output disable time from low level			17	25	ns

### 6.9 Typical Characteristics

Conditions listed in each chart

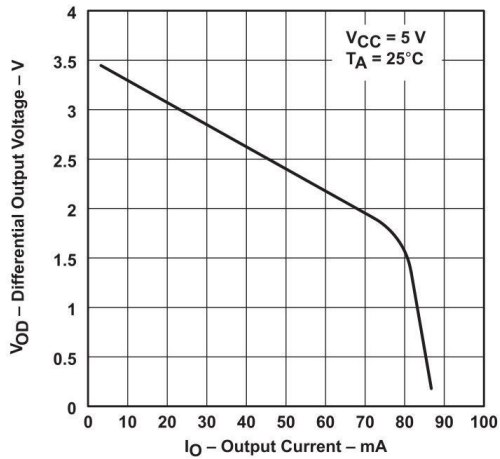


**Figure 1. Driver, High-level Output Voltage vs High-Level Output Current**

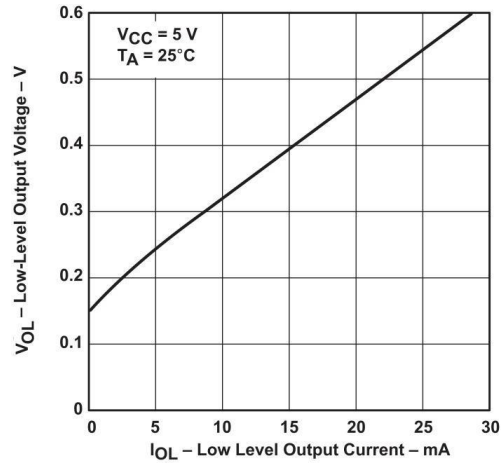


**Figure 2. Driver, Low-Level Output Voltage vs Low-Level Output Current**

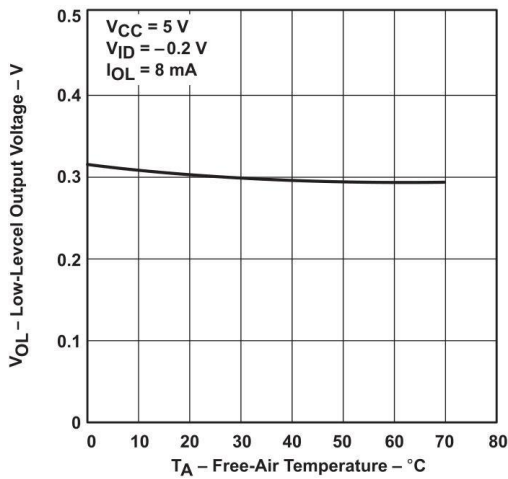
**Typical Characteristics(continued)**



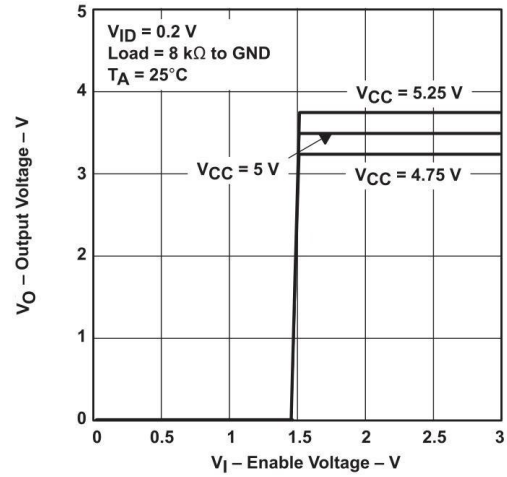
**Figure 3. Driver, Differential Output Voltage vs Output Current**



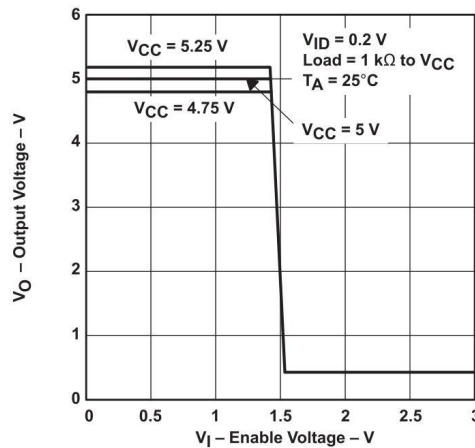
**Figure 4. Receiver, Low-Level Output Voltage vs Low-Level Output Current**



**Figure 5. Receiver, Low-Level Output Voltage vs Low-Level Output Current**



**Figure 6. Low-Level Output Voltage vs Free-Air Temperature**



**Figure 7. Output Voltage vs Enable Voltage**

## 7. PARAMETER MEASUREMENT INFORMATION

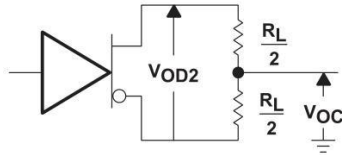


Figure 8. Driver  $V_{OD}$  and  $V_{OC}$

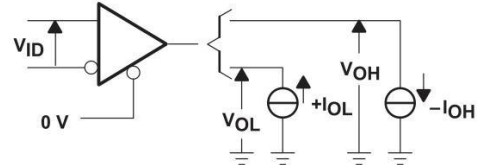
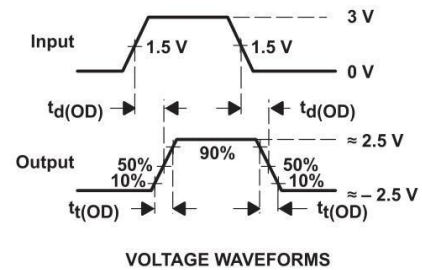
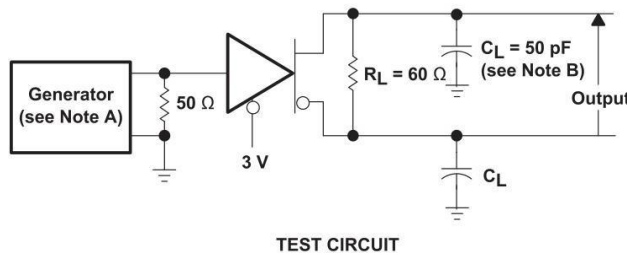
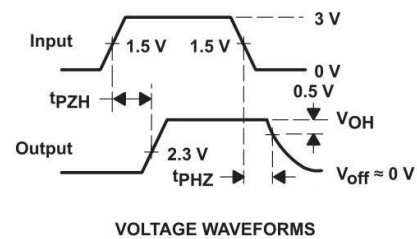
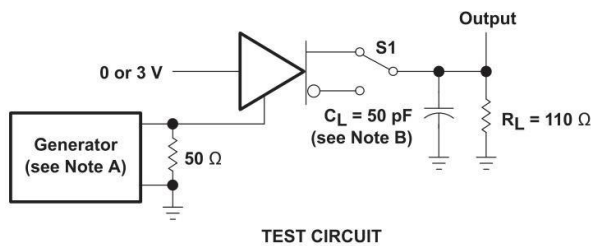


Figure 9. Receiver  $V_{OH}$  and  $V_{OL}$



- A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_o = 50 \Omega$ .
- B.  $C_L$  includes probe and jig capacitance.

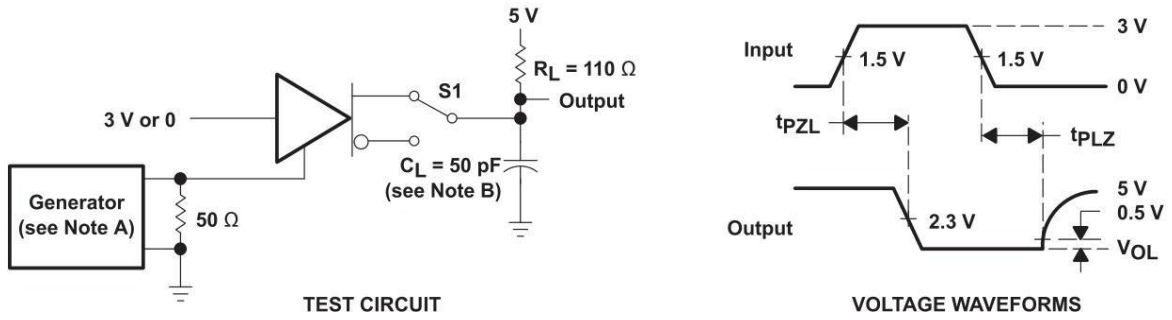
Figure 10. Driver Test Circuit and Voltage Waveforms



- A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_o = 50 \Omega$ .
- B.  $C_L$  includes probe and jig capacitance.

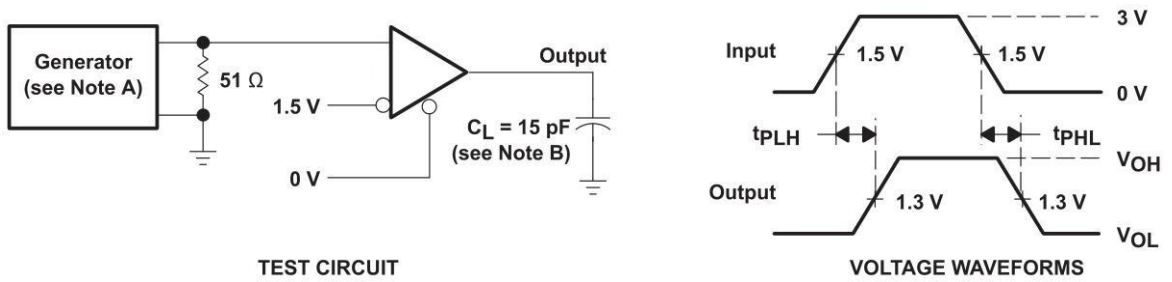
Figure 11. Driver Test Circuit and Voltage Waveforms





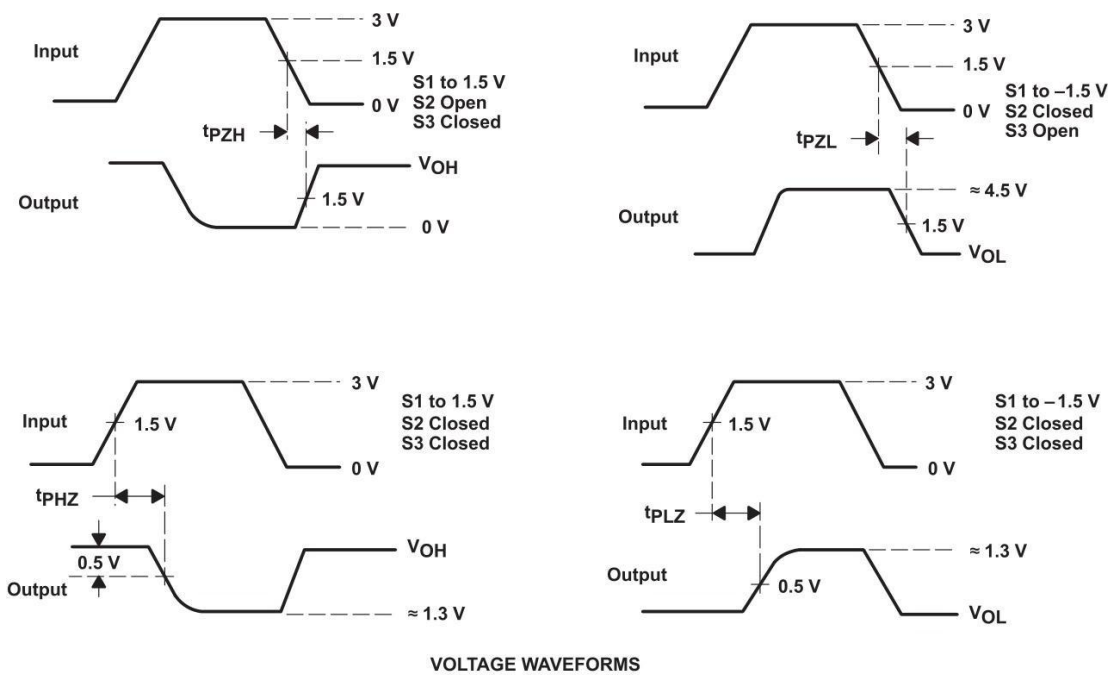
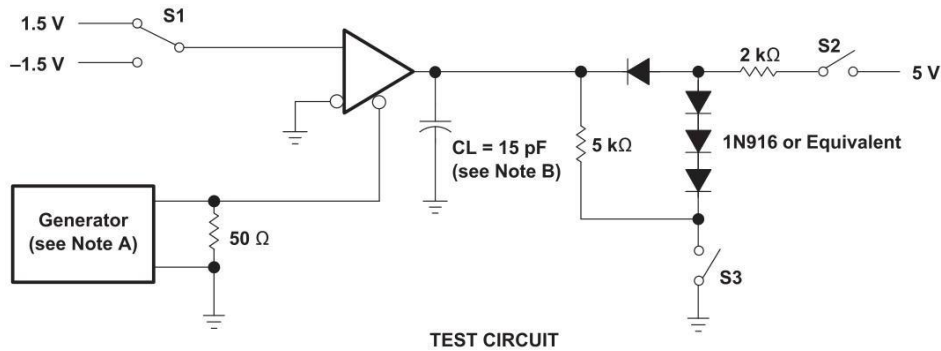
- A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_0 = 50$  Ω.
- B.  $C_L$  includes probe and jig capacitance.

**Figure 12. Driver Test Circuit and Voltage Waveforms**



- A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_0 = 50$  Ω.
- B.  $C_L$  includes probe and jig capacitance.

**Figure 13. Receiver Test Circuit and Voltage Waveforms**



- A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_0 = 50$   $\Omega$ .
- B.  $C_L$  includes probe and jig capacitance.

**Figure 14. Receiver Test Circuit and voltage Waveforms**

## 8. DETAILED DESCRIPTION

### 8.1. Overview

The XL75176 differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus-transmission lines. It is designed for balanced transmission lines and meets ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11.

The XL75176 combines a 3-state differential line driver and a differential input linereceiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or  $V_{CC} = 0$ . These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

### 8.2. Functional Block Diagrams

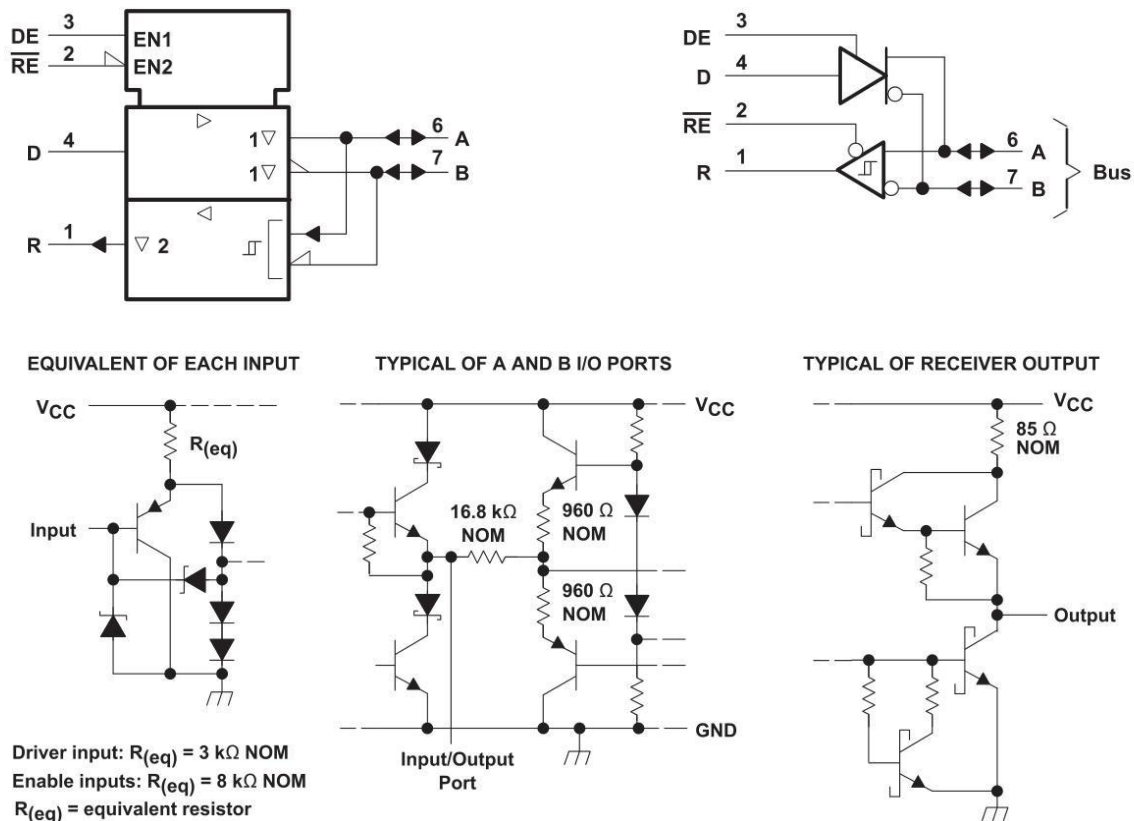


Figure 15. Schematics of Inputs and Outputs

### 8.3. Feature Description

#### 8.3.1 Driver

The driver converts a TTL logic signal level to RS-422 and RS-485 compliant differential output. The TTL logic input, DE pin, can be used to turn the driver on and off.

**Table 2. Driver Function Table<sup>(1)</sup>**

INPUT D	ENABLE DE	DIFFERENTIAL OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level,  
X = irrelevant, Z = high impedance (off)

#### 8.3.2 Receiver

The receiver converts a RS-422 or RS-485 differential input voltage to a TTL logic level output. The TTL logic input, RE pin, can be used to turn the receiver logic output on and off.

**Table 3. Receiver Function Table(1)**

DIFFERENTIAL INPUTS A-B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2 V$	L	H
$-0.2 V < V_{ID} < 0.2 V V_{ID}$	L	U
$\leq -0.2 V$	L	L
X	H	Z
Open	L	U

(1) H = high level,  
L = low level,  
U = unknown,  
Z = high impedance (off)

### 8.4. Device Functional Modes

#### 8.4.1 Device Powered

Both the driver and receiver can be individually enabled or disabled in any combination. DE and RE can be connected together for a single port direction control bit.

#### 8.4.2 Device Unpowered

The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or  $V_{CC} = 0$ .

## 9. APPLICATION AND IMPLEMENTATION

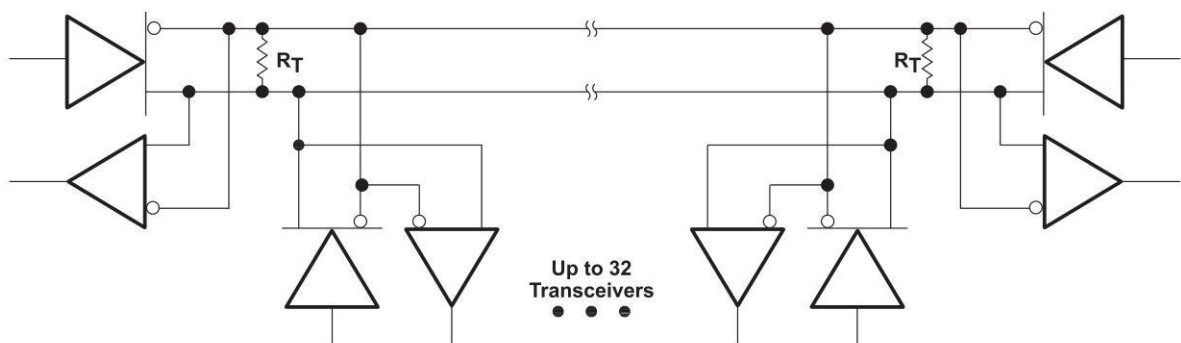
### NOTE

Information in the following applications sections is not part of the Xinluda component specification, and Xinluda does not warrant its accuracy or completeness. Xinluda's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1. Application Information

The device can be used in RS-485 and RS-422 physical layer communications.

### 9.2. Typical Application



The line should be terminated at both ends in its characteristic impedance ( $R_T = Z_0$ ). Stub lengths off the main line should be kept as short as possible.

**Figure 16. Typical Application Circuit**

#### 9.2.1 Design Requirements

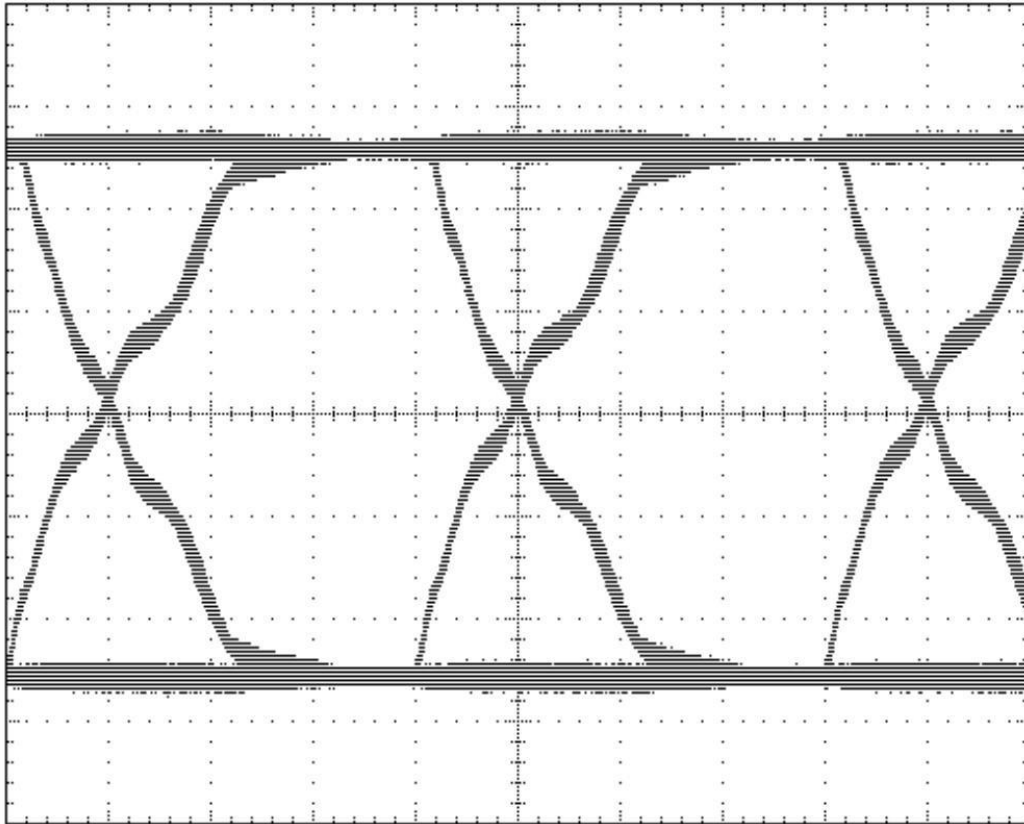
- 5-V power source
- RS-485 bus operating at 5 Mbps or less
- Connector that ensures the correct polarity for port pins
- External fail safe implementation

#### 9.2.2 Detailed Design Procedure

- Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line
- If desired, add external fail-safe biasing to ensure +200 mV on the A-B port.

## Typical Application (continued)

### 9.2.3 Application Curves



**Figure 17. Eye Diagram for 5-Mbps Over 100 feet of Standard CAT-5E cable  
120- $\Omega$  Termination at Both Ends.**

## 10. POWER SUPPLY RECOMMENDATIONS

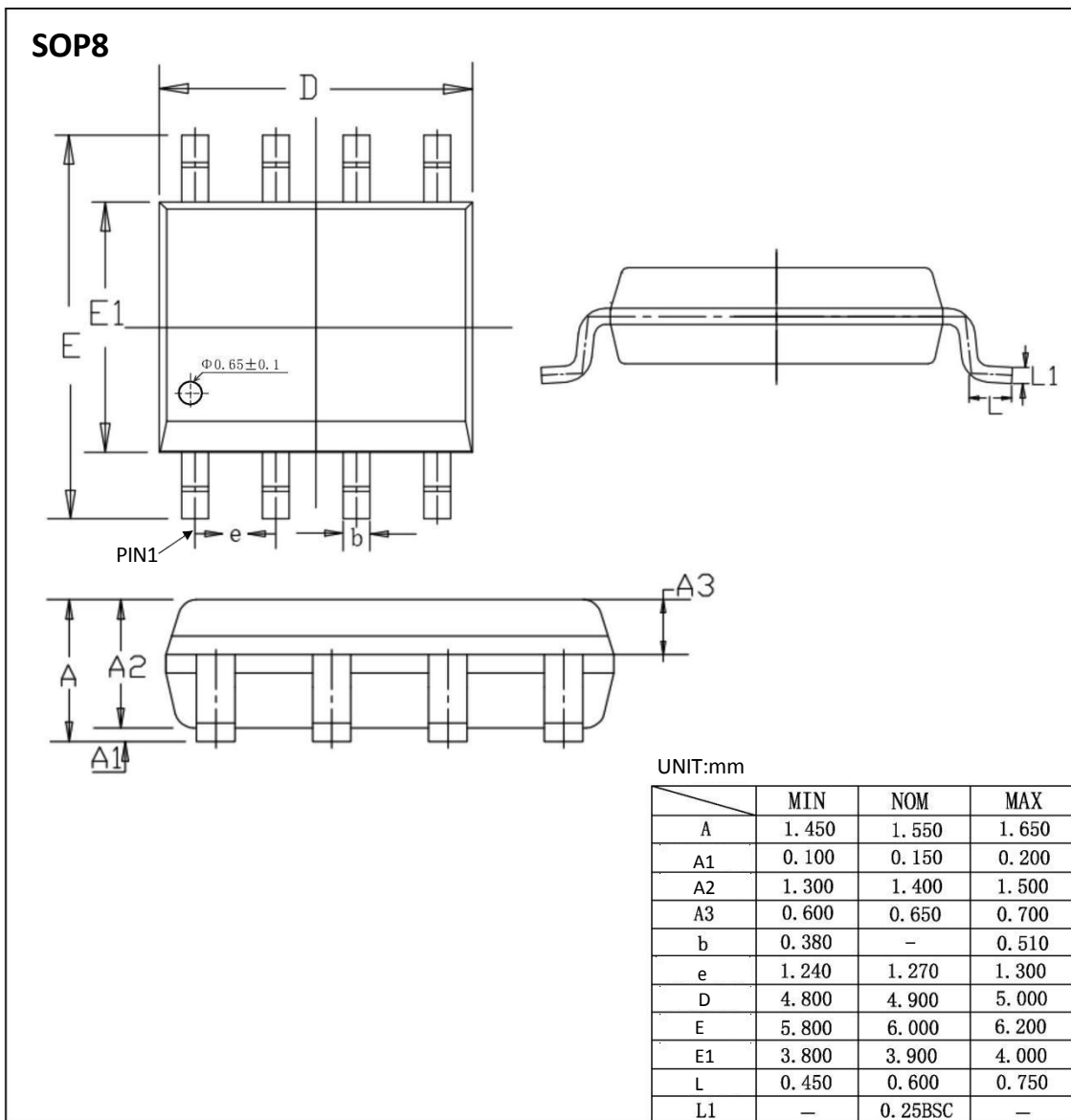
Power supply should be 5 V with a tolerance less than 10%

## 11. ORDERING INFORMATION

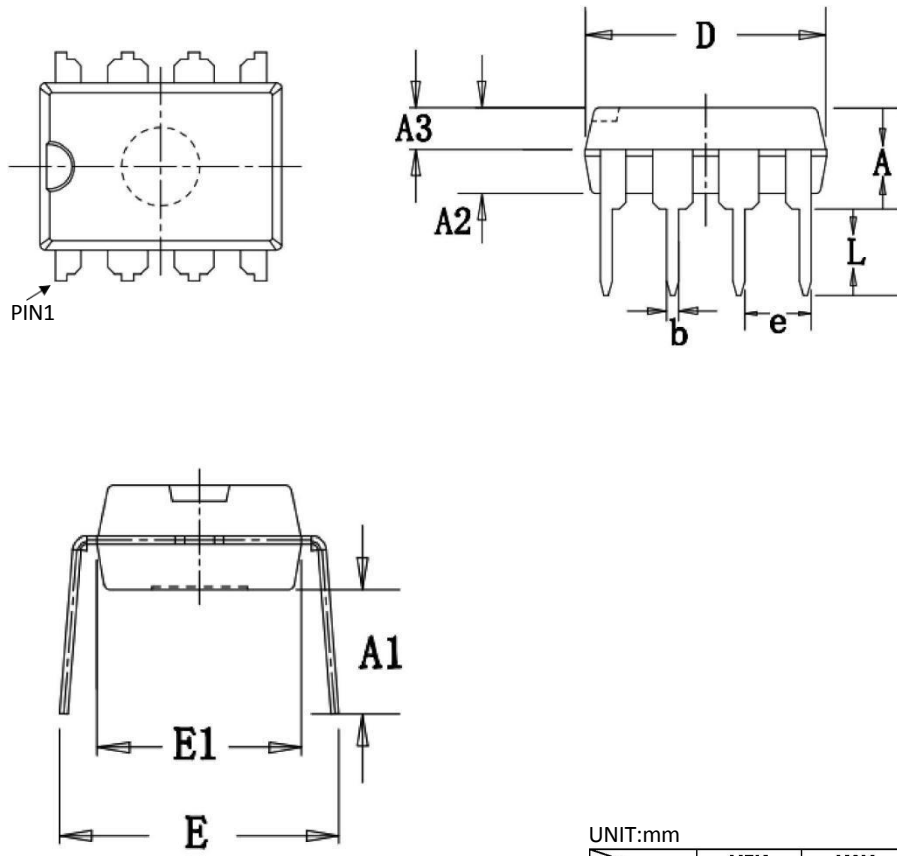
Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL75176AD	XL75176	SOP8	4.90 * 3.90	- 40 to 85	MSL3	T&R	2500
XL75176AP	XL75176AP	DIP8	9.25 * 6.38	- 40 to 85	MSL3	Tube 50	2000

## 12. DIMENSIONAL DRAWINGS



**DIP8**



UNIT:mm

	MIN	NOM	MAX
A	3.600	3.800	4.000
A1	3.786	3.886	3.986
A2	3.200	3.300	3.400
A3	1.550	1.600	1.650
b	0.440	—	0.490
e	2.510	2.540	2.570
D	9.150	9.250	9.350
E	7.800	8.500	9.200
E1	6.280	6.380	6.480
L	3.000	—	—

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