

1. DESCRIPTION

The XL65HVD08DR/XL65HVD08P combines a 3-state differential line driver and differential line receiver designed for balanced data transmission and interoperability with ANSI TIA/EIA-485-A and ISO-8482 Standard compliant devices.

The wide supply voltage range and low quiescent current requirements allow the XL65HVD08DR/XL65HVD08P to operate from a 5-V power bus in the cable with as much as a 2V line voltage drop. Busing power in the cable can alleviate the need for isolated power to be generated at each connection of a ground-isolated bus.

The driver differential outputs and receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or not powered. The drivers and receivers have active-high and active-low enables respectively, which can be externally connected together to function as a direction control.

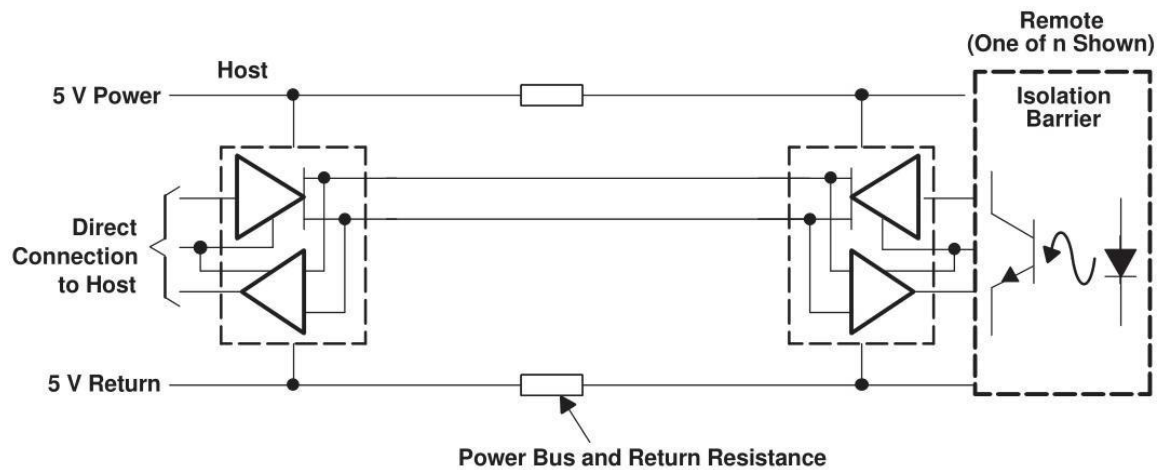
2. FEATURES

- Operates With a 3-V to 5.5-V Supply
- Consumes Less Than 90-mW Quiescent Power
- Open-Circuit, Short-Circuit, and Idle-Bus Failsafe Receiver
- 1/8th Unit-Load (up to 256 nodes on the bus)
- Bus-Pin ESD Protection Exceeds 16-kV HBM
- Driver Output Voltage Slew-Rate Limited for Optimum Signal Quality at 10 Mbps
- Electrically Compatible With ANSI TIA/EIA-485 Standard
- Package option: XL65HVD08DR (SOP8), XL65HVD08P (DIP8)

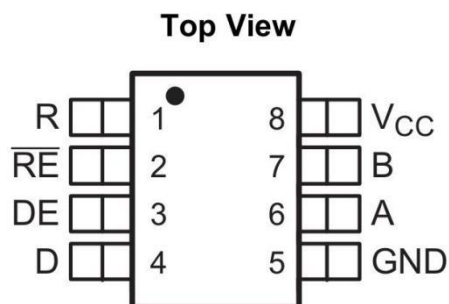
3. APPLICATIONS

- Data Transmission With Remote Stations Powered From the Host
- Isolated Multipoint Data Buses
- Industrial Process Control Networks
- Point-of-Sale Networks
- Electric Utility Metering

4. TYPICAL APPLICATION SCHEMATIC



5. PIN CONFIGURATIONS AND FUNCTIONS



PIN		TYPE	DESCRIPTION
NAME	NO.		
A	6	Bus input / output	Driver output and receiver input (complementary to B)
B	7	Bus input / output	Driver output and receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{\text{RE}}$	2	Digital input	Receiver enable low
V _{CC}	8	Supply	3-V to 5.5-V supply

6. SPECIFICATIONS

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted⁽¹⁾ ⁽²⁾

	MIN	MAX	UNIT
Supply voltage, V_{CC}	-0.3	6	V
Voltage at A or B	-9	14	V
Input voltage at D, DE, R or $\overline{RE}$	-0.5	$V_{CC} + 0.5$	V
Voltage input, transient pulse, A and B, through 100 Ω	-25	25	V
Receiver output current, I_O	-11	11	mA
Maximum Junction Temperature, T_J		150	°C
Storage Temperature, T_{STG}	-65	150	°C

[1] Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	A, B, and GND	16000
		All pins	4000
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾		1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommend Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3		5.5	V
Input voltage at any bus terminal (separately or common mode), V_I ⁽¹⁾	-7		12	V
High-level input voltage, V_{IH}	2.25		V_{CC}	V
Low-level input voltage, V_{IL}				
	0		0.8	
Differential input voltage, V_{ID}	-12		12	
High-level output current, I_{OH}	Driver		-60	mA
	Receiver		-8	
Low-level output current, I_{OL}	Driver		60	mA
	Receiver		8	
Operating free-air temperature, T_A	XL65HVD08		-40	85
				°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		65HVD08	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	175.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	44.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ V_{OD} $	Driver differential output voltage magnitude	$R_L = 60\ \Omega$, 375 Ω on each output to -7 V to 12 V, See Figure 7	1.5		V_{CC}	V
$\Delta V_{OD} $	Change in magnitude of driver differential output voltage	$R_L = 54\ \Omega$	-0.2		0.2	V
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27- Ω load resistors, See Figure 8		0.5		V
V_{IT+}	Positive-going receiver differential input voltage threshold				-10	mV
V_{IT-}	Negative-going receiver differential input voltage threshold			-200		mV
V_{hys}	Receiver differential input voltage threshold hysteresis($V_{IT+} - V_{IT-}$)			35		mV
V_{OH}	Receiver high-level output voltage	$I_{OH} = -8\ \text{mA}$		2.4		V
V_{OL}	Receiver low-level output voltage	$I_{OL} = 8\ \text{mA}$			0.4	V
I_{IH}	Driver input, driver enable, and receiver enable high-level input current		-100		100	μA
I_{IL}	Driver input, driver enable, and receiver enable low-level input current		-100		100	μA
I_{OS}	Driver short-circuit output current	7 V < V_O < 12 V	-265		265	mA

Electrical Characteristics (continued)

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Bus input current (disabled driver)	$V_I = 12\ \text{V}$			130	μA
		$V_I = -7\ \text{V}$	-100			
		$V_I = 12\ \text{V}$, $V_{CC} = 0\ \text{V}$			130	
		$V_I = -7\ \text{V}$, $V_{CC} = 0\ \text{V}$	-100			
I_{CC}	Supply current	Receiver enabled, driver disabled, no load			10	mA
		Driver enabled, receiver disabled, no load			16	
		Both disabled			5	μA
		Both enabled, no load			16	mA

6.6 Driver Switching Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL} Driver high-to-low propagation delay time	$R_L = 54 \Omega$, $C_L = 50 \text{ pF}$, See Figure 9	18		40	ns
t_{PLH} Driver low-to-high propagation delay time		18		40	
t_r Driver 10%-to-90% differential output rise time		10		55	
t_f Driver 90%-to-10% differential output fall time		10		55	
$t_{SK(P)}$ Driver differential output pulse skew, $ t_{PHL} - t_{PLH} $				2.5	
t_{en} Driver enable time	Receiver enabled, See Figures 4 and 5			55	ns
	Receiver disabled, See Figures 4 and 5			6	μs
t_{dis} Driver disable time	Receiver enabled, See Figures 4 and 5			90	ns

6.7 Receiver Switching Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL} Receiver high-to-low propagation delay time	$C_L = 15 \text{ pF}$, See Figure 12			70	ns
t_{PLH} Receiver low-to-high propagation delay time				70	
t_r Receiver 10%-to-90% differential output rise time				5	
t_f Receiver 90%-to-10% differential output fall time				5	
$t_{SK(P)}$ Receiver differential output pulse skew, $ t_{PHL} - t_{PLH} $				4.5	
t_{en} Receiver enable time	Driver enabled, See Figure 13			15	ns
	Driver disabled, See Figure 14			6	μs
t_{dis} Receiver disable time	Driver enabled, See Figure 13			20	ns

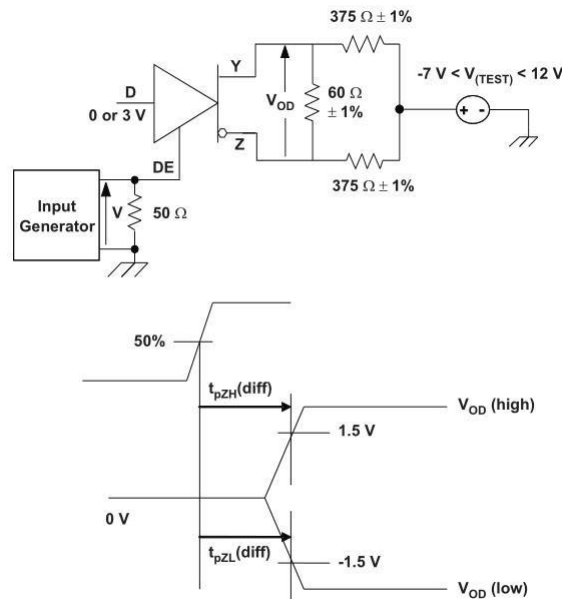


Figure 1. Driver Enable Time From DE to V_{OD}

The time $t_{pZL}(x)$ is the measure from DE to $V_{OD}(x)$. V_{OD} is valid when it is greater than 1.5 V.

6.8 Typical Characteristics

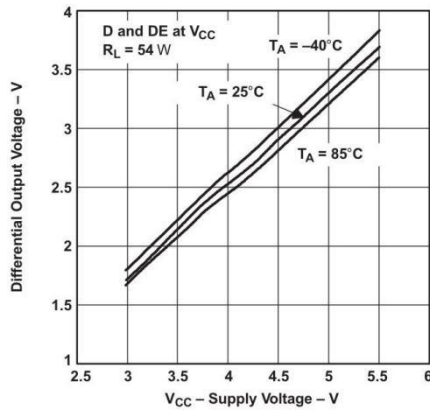


Figure 2. Differential Output Voltage vs Supply Voltage

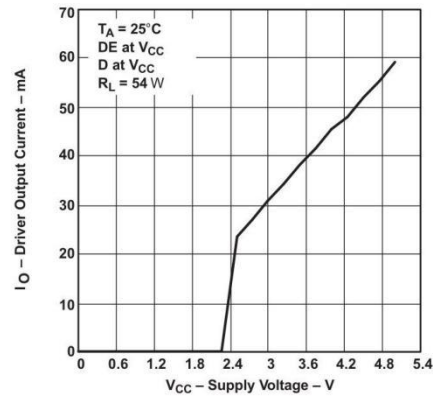


Figure 3. Driver Output Current vs Supply Voltage

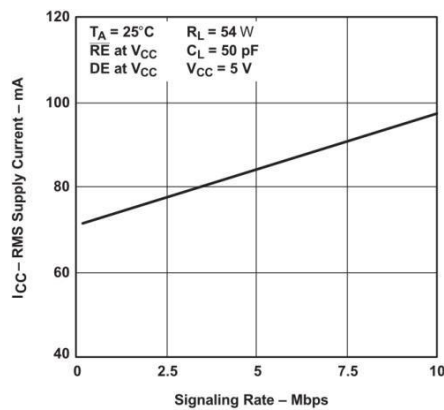


Figure 4. RMS Supply Current vs Signaling Rate

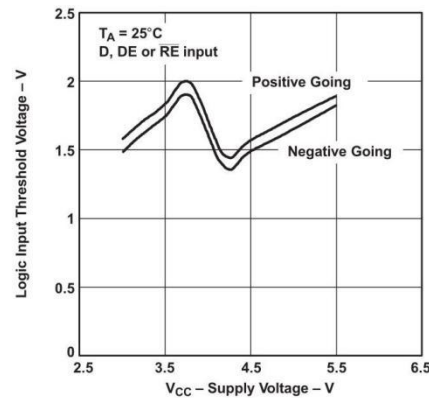


Figure 5. Logic Input Threshold Voltage vs Supply Voltage

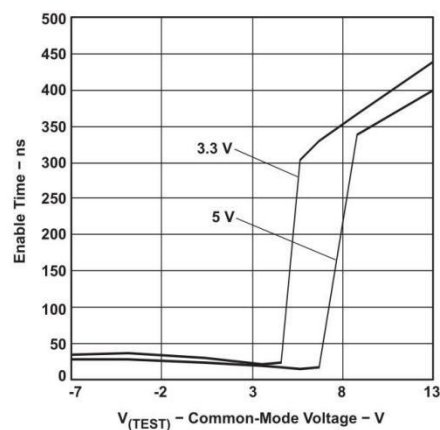


Figure 6. Enable Time vs Common-Mode Voltage (See Figure 1)

7. PARAMETER MEASUREMENT INFORMATION

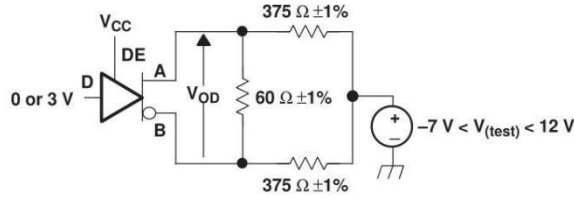


Figure 7. Driver V_{OD} With Common-Mode Loading Test Circuit

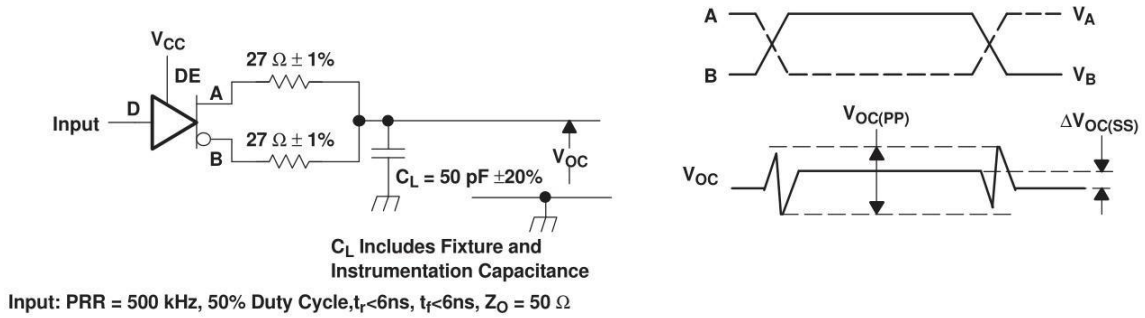


Figure 8. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

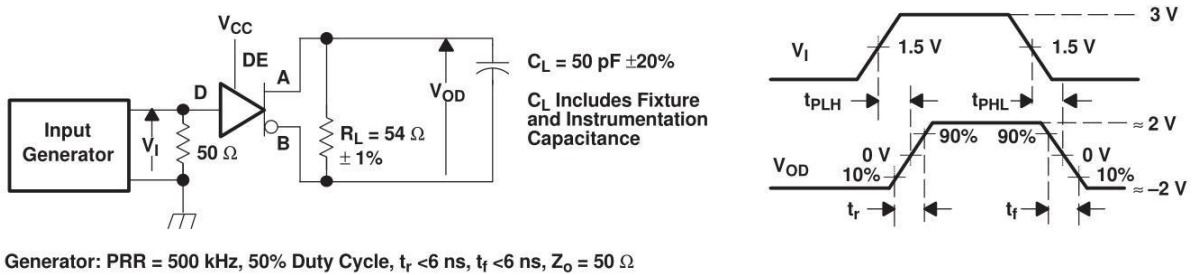


Figure 9. Driver Switching Test Circuit and Voltage Waveforms

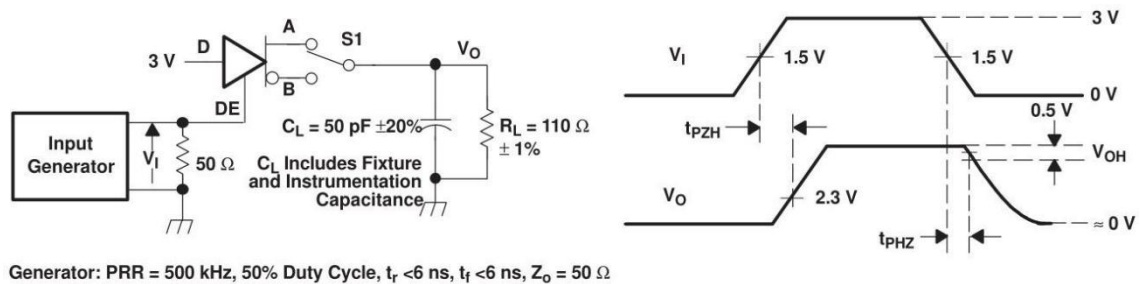


Figure 10. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms

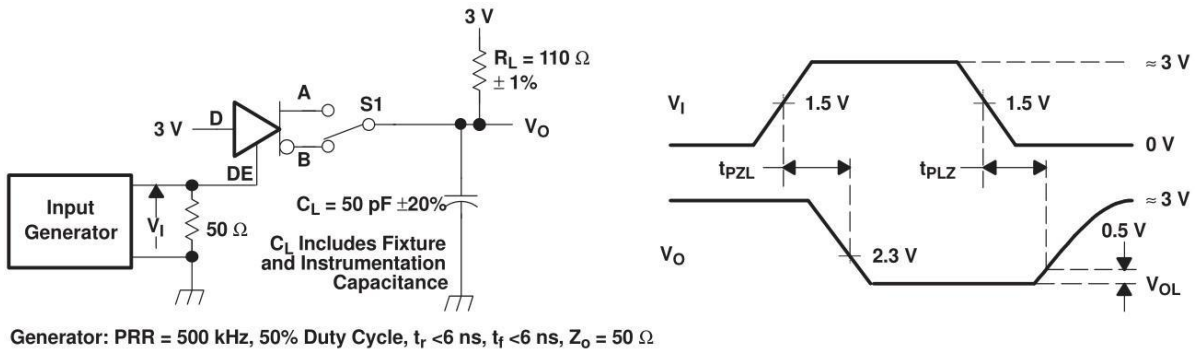


Figure 11. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

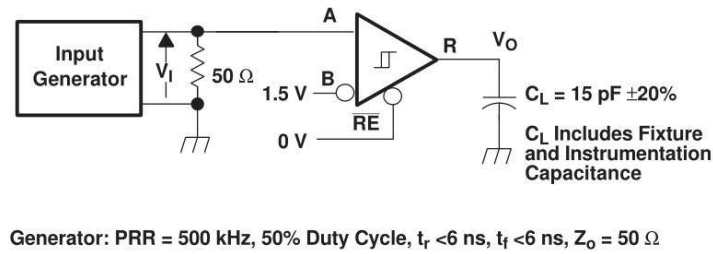


Figure 12. Receiver Switching Test Circuit and Voltage Waveforms

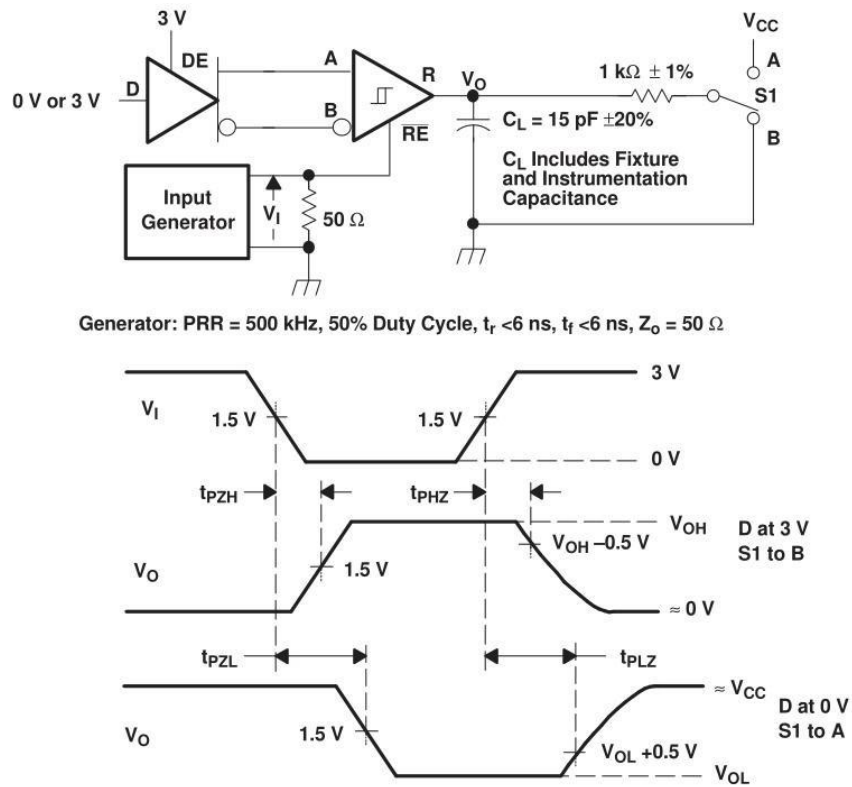


Figure 13. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled

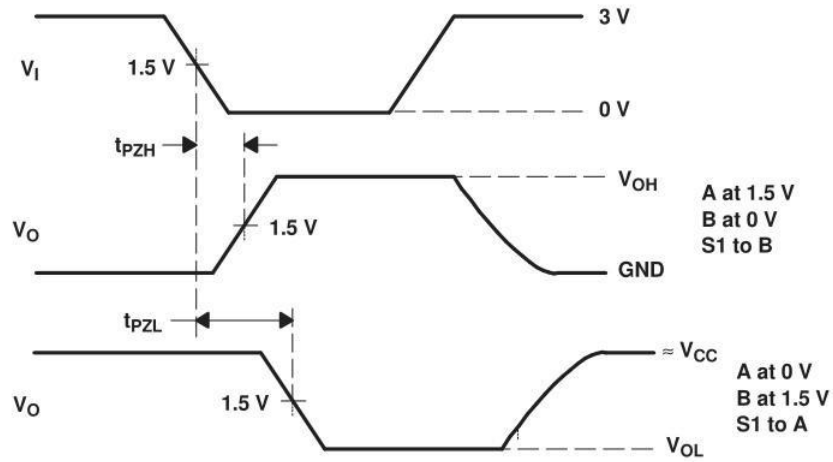
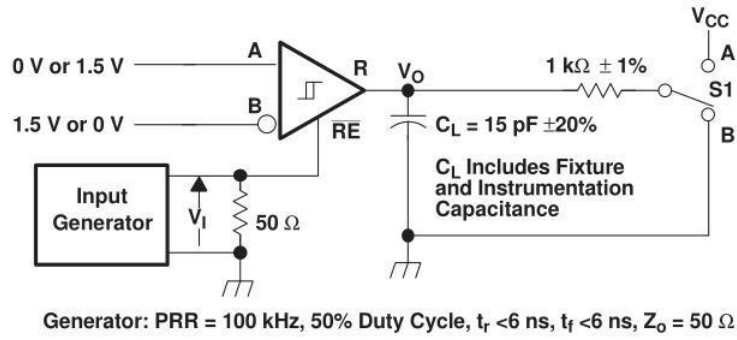


Figure 14. Receiver Enable Time From Standby (Driver Disabled)

8. DETAILED DESCRIPTION

8.1 Overview

The XL65HVD08 is a 3-V to 5.5-V, half-duplex, RS-485 transceiver suitable for data transmission up to 10 Mbps.

This device has an active-high driver enable and active-low receiver enable. A standby current of less than 5 μ A can be achieved by disabling both driver and receiver.

Device operation is specified over a wide temperature range from -40°C to +85°C.

8.2 Functional Block Diagram

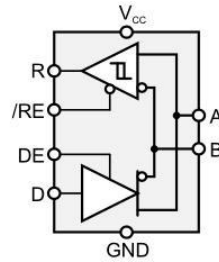


Figure 15. Logic Diagram (Positive)

8.3 Feature Description

Internal ESD protection circuits protect the transceiver bus terminals against ± 16 kV Human Body Model (HBM) electrostatic discharges and all other pins up to ± 4 kV.

The XL65HVD08 provides internal biasing of the receiver input thresholds for open-circuit, bus-idle, or short-circuit failsafe conditions, and a typical receiver hysteresis of 35 mV.

8.4 Device Functional Modes

Table 1. Function Table: Driver

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

Table 2. Function Table: Receiver

DIFFERENTIAL INPUTS	ENABLE ⁽¹⁾	OUTPUT ⁽¹⁾
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \leq -0.2$ V	L	L
-0.2 V $< V_{ID} < -0.01$ V	L	?
-0.01 V $\leq V_{ID}$	L	H
X	H	Z
Open Circuit	L	H
Short Circuit	L	H

(1) H = high level; L = low level; Z = high impedance; X = irrelevant;
? = indeterminate

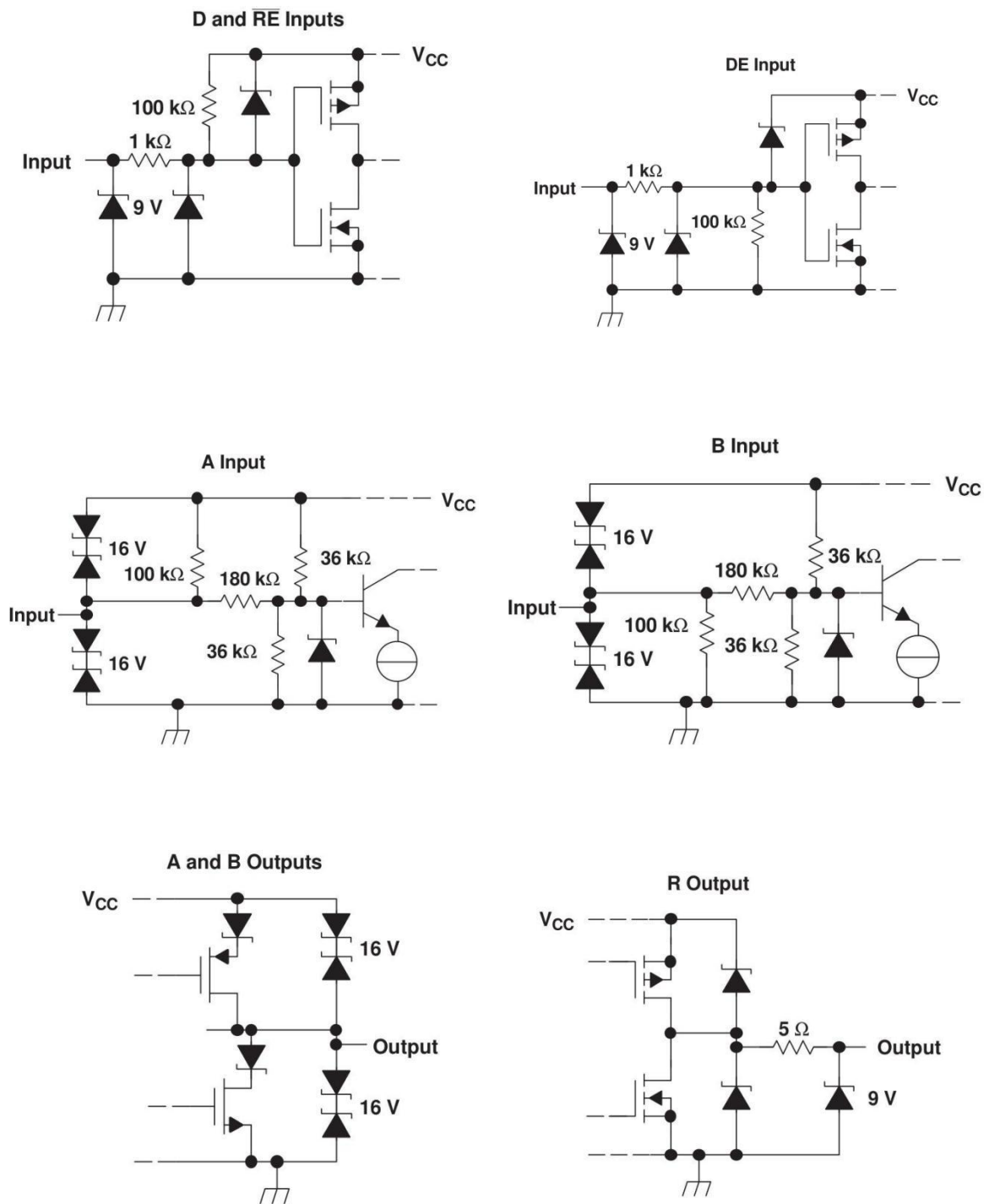


Figure 16. Equivalent Input and Output Schematic Diagrams

9. APPLICATION AND IMPLEMENTATION

NOTE

Information in the following applications sections is not part of the Xinluda component specification, and Xinluda does not warrant its accuracy or completeness. Xinluda's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1. Application Information

As electrical loads are physically distanced from their power source, the effects of supply and return line impedance and the resultant voltage drop must be accounted. If the supply regulation at the load cannot be maintained to the circuit requirements, it forces the use of remote sensing, additional regulation at the load, bigger or shorter cables, or a combination of these. The XL65HVD08 eases this problem by relaxing the supply requirements to allow for more variation in the supply voltage over typical RS-485 transceivers.

9.1.1 Supply Source Impedance

In the steady state, the voltage drop from the source to the load is simply the wire resistance times the load current as modeled in Figure 17.

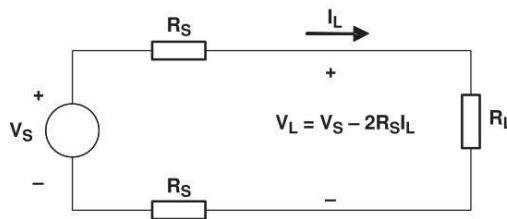


Figure 17. Steady-State Circuit Model

For example, if you were to provide 5-V $\pm 5\%$ supply power to a remote circuit with a maximum load requirement of 0.1 A (one XL65HVD08), the voltage at the load would fall below the 4.5-V minimum of most 5-V circuits with as little as 5.8 m of 28-GA conductors. Table 3 summarizes wire resistance and the length for 4.5 V and 3 V at the load with 0.1 A of load current. The maximum lengths would scale linearly for higher or lower load currents.

Table 3. Maximum Cable Lengths for Minimum Load Voltages at 0.1 A Load

WIRE SIZE	RESISTANCE	4.5-V LENGTH AT 0.1 A	3-V LENGTH AT 0.1 A
28 Gauge	0.213 Ω/m	5.8 m	41.1 m
24 Gauge	0.079 Ω/m	15.8 m	110.7 m
22 Gauge	0.054 Ω/m	23.1 m	162.0 m
20 Gauge	0.034 Ω/m	36.8 m	257.3 m
18 Gauge	0.021 Ω/m	59.5 m	416.7 m

Under dynamic load requirements, the distributed inductance and capacitance of the power lines may not be ignored and decoupling capacitance at the load is required. The amount depends upon the magnitude and frequency of the load current change but, if only powering the XL65HVD08, a 0.1 μF ceramic capacitor is usually sufficient.

9.1.2 Opto-Isolated Data Buses

Long RS-485 circuits can create large ground loops and pick up common-mode noise voltages in excess of the range tolerated by standard RS-485 circuits. A common remedy is to provide galvanic isolation of the data circuit from earth or local grounds.

Application Information (continued)

Transformers, capacitors, or phototransistors most often provide isolation of the bus and the local node. Transformers and capacitors require changing signals to transfer the information over the isolation barrier and phototransistors (opto-isolators) can pass steady-state signals. Each of these methods incurs additional costs and complexity, the former in clock encoding and decoding of the data stream and the latter in requiring an isolated power supply.

Quite often, the cost of isolated power is repeated at each node connected to the bus as shown in Figure 18. The possibly lower-cost solution is to generate this supply once within the system and then distribute it along with the data line(s) as shown in Figure 19.

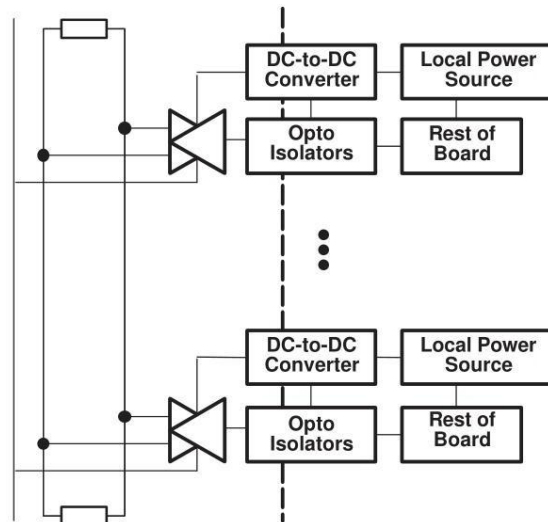


Figure 18. Isolated Power at Each Node

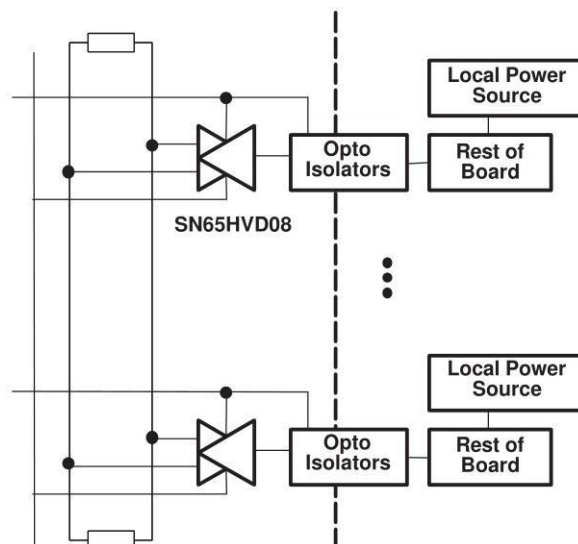


Figure 19. Distribution of Isolated Power

The features of the XL65HVD08 are particularly good for the application of Figure 19. Due to added supply source impedance, the low quiescent current requirements and wide supply voltage tolerance allow for the poorer load regulation.

Application Information (continued)

9.1.2 Opto Alternative

The ISO150 is a two-channel, galvanically isolated data coupler capable of data rates of 80 Mbps. Each channel can be individually programmed to transmit data in either direction.

Data is transmitted across the isolation barrier by coupling complementary pulses through high-voltage 0.4-pF capacitors. Receiver circuitry restores the pulses to standard logic levels. Differential signal transmission rejects isolation-mode voltage transients up to 1.6 kV/ms.

ISO150 avoids the problems commonly associated with opto-couplers. Optically-isolated couplers require high current pulses and allowance must be made for LED aging. The ISO150's Bi-CMOS circuitry operates at 25 mW per channel with supply voltage range matching that of the XL65HVD08 of 3 V to 5.5 V.

Figure 20 shows a typical circuit.

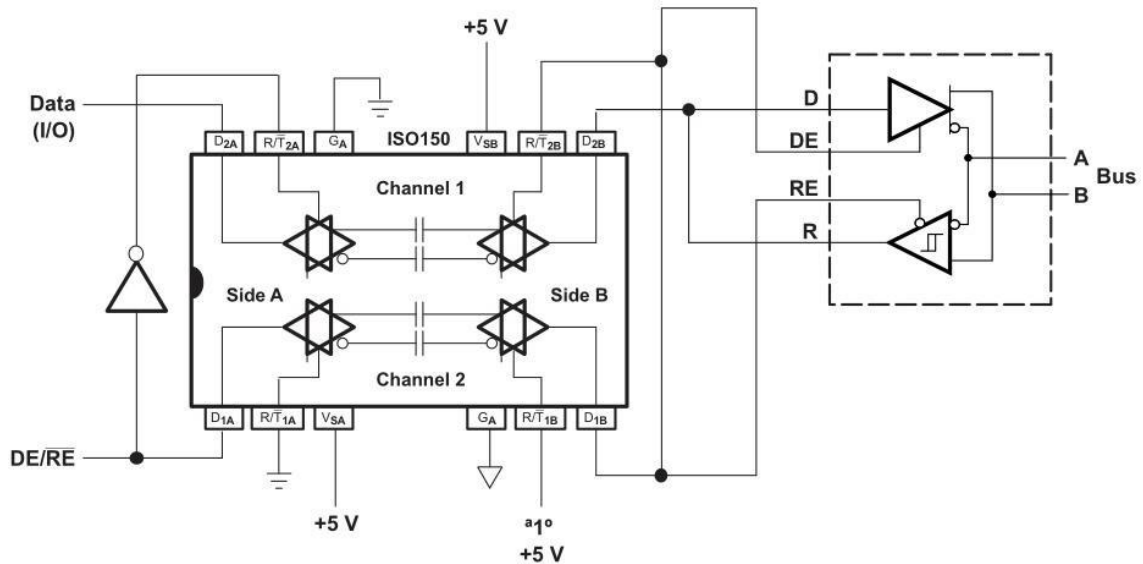


Figure 20. Isolated RS-485 Interface

9.2. Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T , whose value matches the characteristic impedance, Z_0 , of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

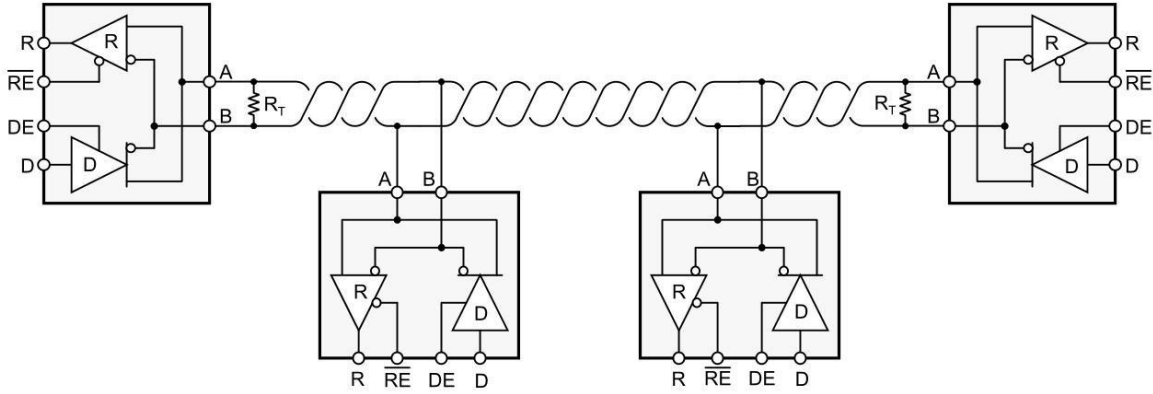


Figure 21. Typical Application Diagram

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, meaning the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable may be without introducing data errors. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

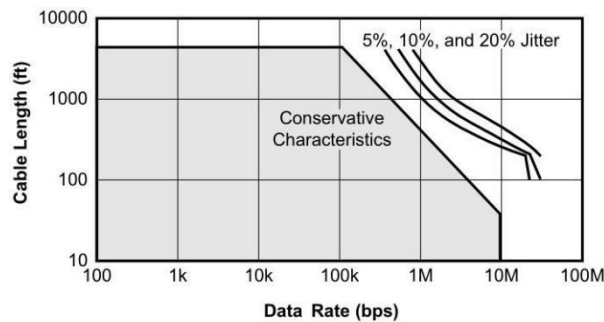


Figure 22. Cable Length vs Data Rate Characteristic

Typical Application (continued)

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in [Equation 1](#).

$$L_{\text{stub}} \leq 0.1 \times t_r \times v \times c$$

Where:

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

Per [Equation 1](#), the maximum recommended stub length for the minimum driver output rise time of the XL65HVD08 for a signal velocity of 78% is 0.23 meters (0.75 feet).

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 k Ω .

Because the XL65HVD08 are each 1/8 UL transceivers,

it is possible to connect up to 256 receivers to the bus.

9.2.1.4 Receiver Failsafe

The differential receivers of the XL65HVD08 family are “failsafe” to invalid bus states caused by:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic High state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the “input indeterminate” range does not include zero volts differential.

In order to comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input VID is more positive than +200 mV, and must output a Low when VID is more negative than -200 mV. The receiver parameters which determine the failsafe performance are VIT(+) and VIT(-).

As shown in the Electrical Characteristics table, differential signals more negative than -200 mV will always cause a Low receiver output, and differential signals more positive than -10 mV will always cause a High receiver output. Thus, when the differential input signal is close to zero, it is still above the maximum VIT(+) threshold of -10 mV, and the receiver output will be High.

Typical Application (continued)

9.2.2 Detailed Design Procedure

In order to protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary.

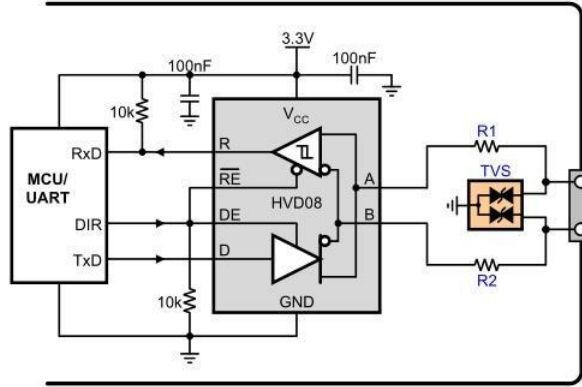


Figure 23. Transient protection against ESD, EFT, and Surge transients

Figure 23 suggests a protection circuit against 10 kV ESD (IEC 61000-4-2), 4 kV EFT (IEC 61000-4-4), and 1 kV surge (IEC 61000-4-5) transients. Table 4 shows the associated Bill of Materials.

Table 4. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	3.3 V to 5 V, 10 Mbps RS-485 Transceiver	XL65HVD08	XINLUDA
R1, R2	10 Ω , Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400 W Transient Suppressor	CDSOT23-SM712	Bourns

9.2.3 Application Curve

Figure 24 demonstrates operation of the XL65HVD08 at a signaling rate of 10 Mbps.

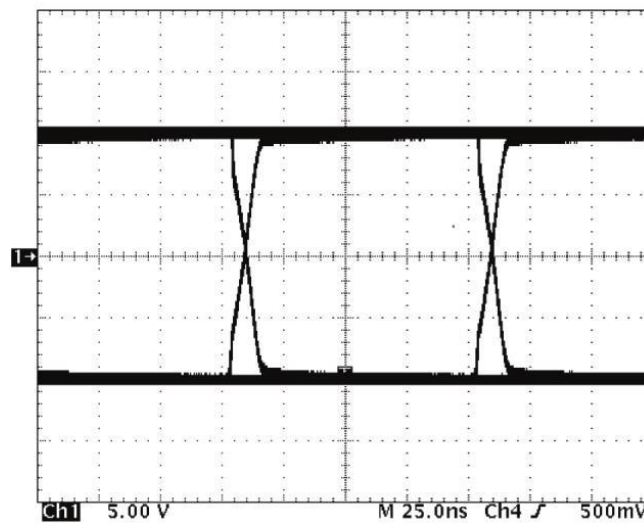


Figure 24. XL65HVD08 Differential Output Waveform

10. POWER SUPPLY RECOMMENDATIONS

To ensure reliable operation at all data rates and power supply voltages, each power supply should be buffered. The 100nF ceramic capacitor is located as close to the power pin as possible. TI manufacturer's TPS76333 and TPS76350 is paired with linear voltage regulators suitable for 3.3V and 5V power supplies, respectively.

11. LAYOUT 11.1. Layout Guidelines

On-chip IEC-ESD protection is sufficient for laboratory and portable equipment but insufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
2. Use VCC and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF bypass capacitors as close as possible to the VCC-pins of transceiver, UART, or controller ICs on the board.
5. Use at least two vias for VCC and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
6. Use 1-k Ω to 10-k Ω pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert series pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

11.2. Layout Example

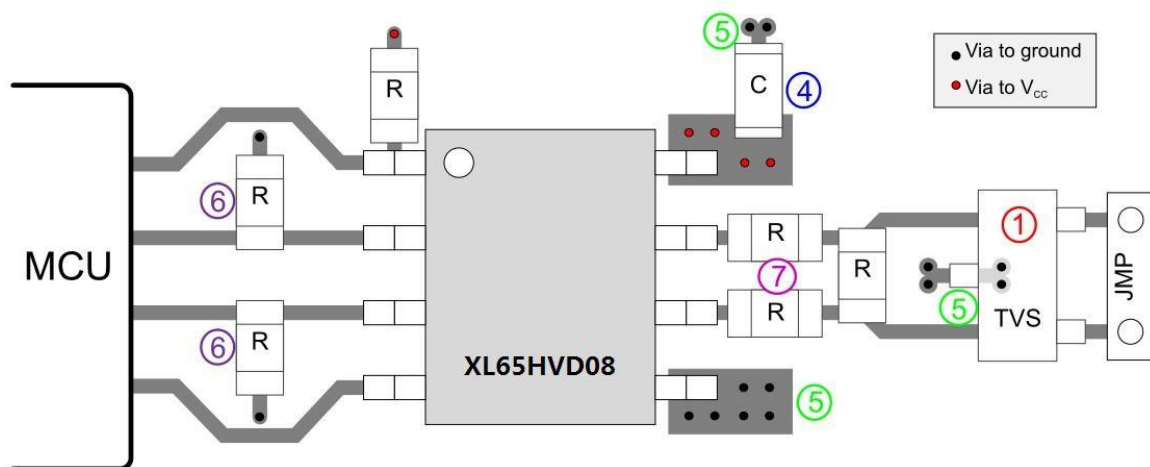


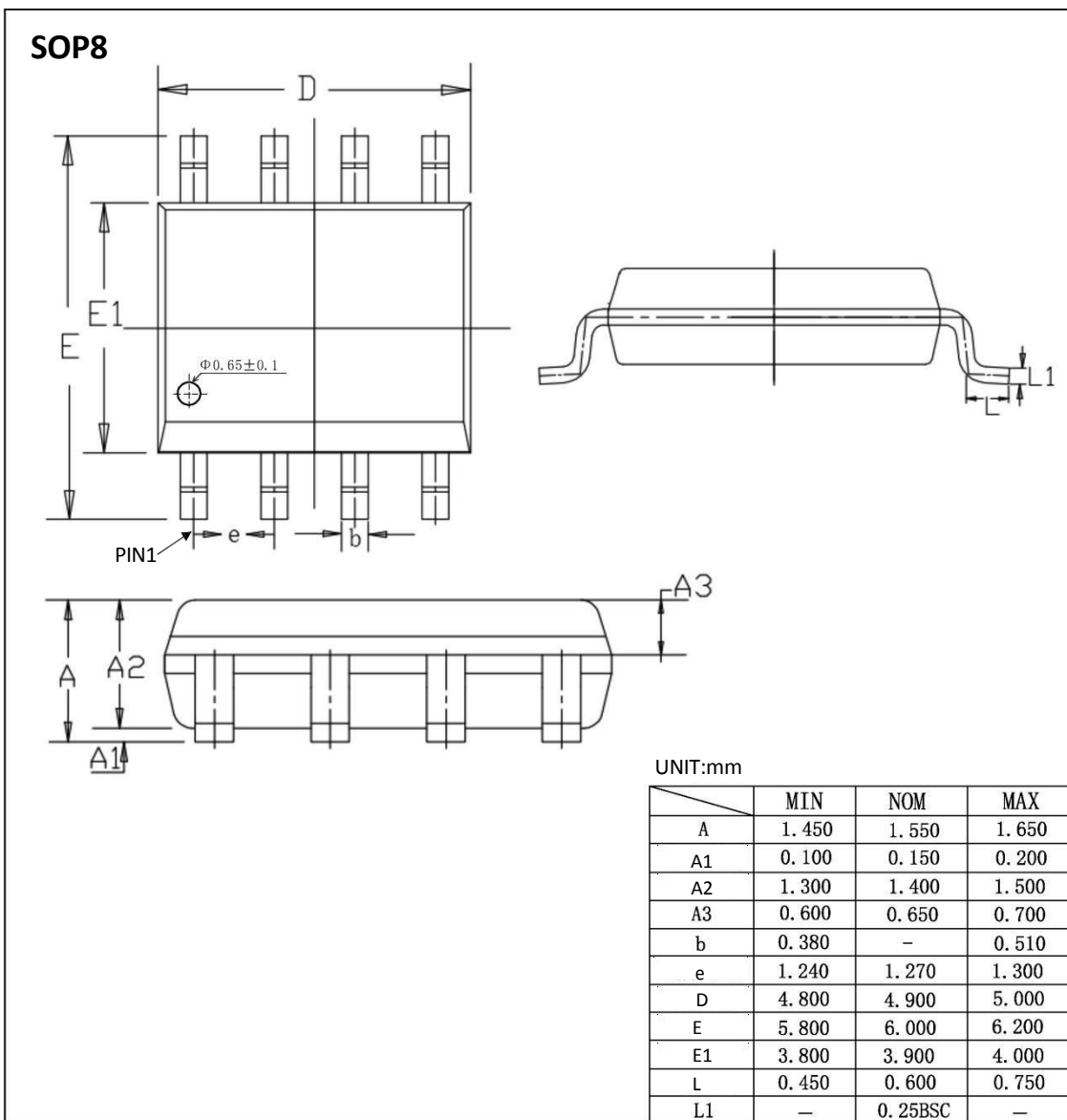
Figure 25. XL65HVD08 Layout example

12. ORDERING INFORMATION

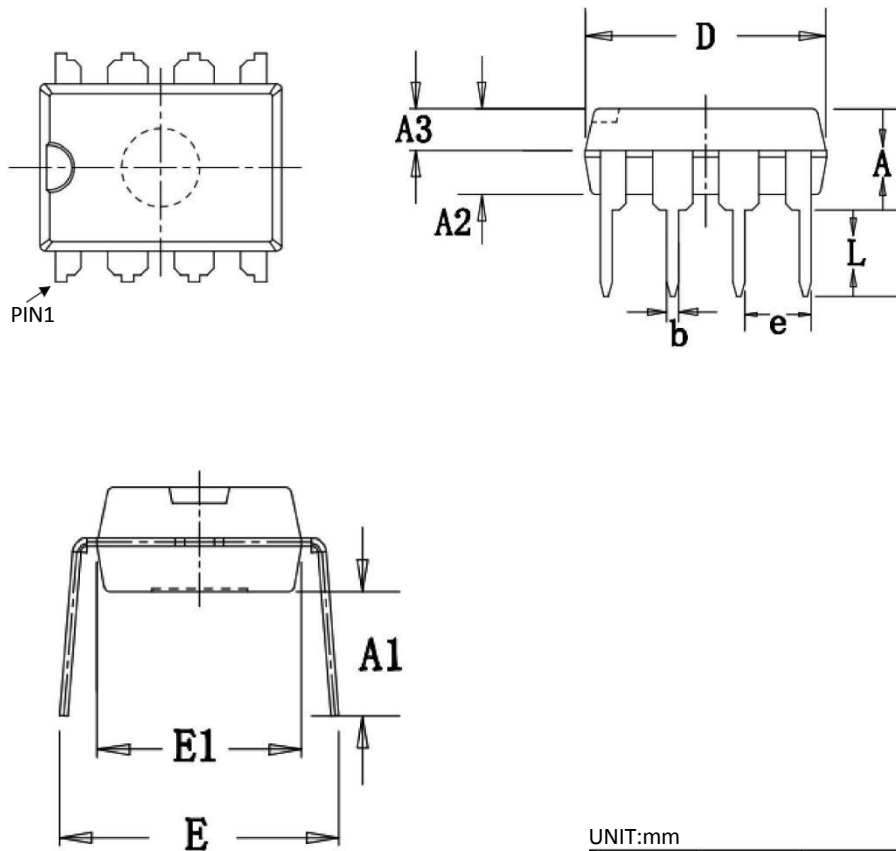
Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL65HVD08DR	XL65HVD08	SOP8	4.90 * 3.90	- 40 to 85	MSL3	T&R	2500
XL65HVD08P	65HVD08P	DIP8	9.25 * 6.38	- 40 to 85	MSL3	Tube 50	2000

13. DIMENSIONAL DRAWINGS



DIP8



UNIT:mm

	MIN	NOM	MAX
A	3.600	3.800	4.000
A1	3.786	3.886	3.986
A2	3.200	3.300	3.400
A3	1.550	1.600	1.650
b	0.440	—	0.490
e	2.510	2.540	2.570
D	9.150	9.250	9.350
E	7.800	8.500	9.200
E1	6.280	6.380	6.480
L	3.000	—	—

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