

DATASHEET

N-Channel Enhancement Mode Power MOSFET

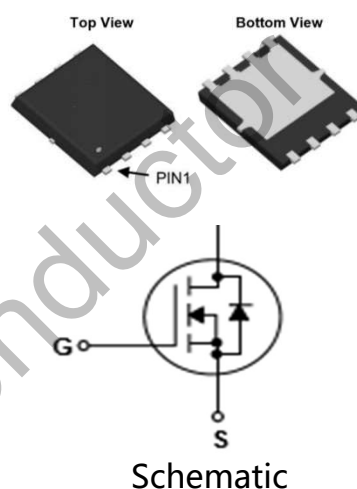
Description

This Power MOSFET is produced using advanced SGT technology. This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Features

- $V_{DS}=40V$, $I_D=200A$
- $R_{DS(ON)} TYP = 1.3m\Omega @ V_{GS}=10V$
- Very Low On-resistance $R_{DS(ON)}$
- Low C_{rss}
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

PDFN5*6-8L



Applications

- PWM Application
- Load Switch
- Power Management

100% UIS TESTED!

100% ΔV_{ds} TESTED!



Package Marking and Ordering Information

Device	Marking	Package	Packing	Reel size	Reel (pcs)	Per Carton (pcs)
200N04		PDFN5*6	Reel	13inch	5000	60000

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Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C=25^{\circ}\text{C}$	I_D	200	A
	$T_C=100^{\circ}\text{C}$		154	
Pulsed Drain Current($T_C=25^{\circ}\text{C}$, T_p Limited By T_{jmax}) ^(note1)		I_{DM}	800	A
Maximum Power Dissipation($T_C=25^{\circ}\text{C}$)		P_D	125	W
Avalanche energy , single Pulse($L=0.5\text{mH}$) ^(note2)		E_{AS}	120	mJ
Peak Diode Recovery dv/dt ^(note3)		dv/dt	4.5	V/ns
Thermal Resistance Junction to Case		$R_{\theta JC}$	1.2	$^{\circ}\text{C/W}$
Operating Junction And Storage Temperature		T_j, T_{stg}	-55 To 150	$^{\circ}\text{C}$
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		T_L	300	$^{\circ}\text{C}$

* Drain current limited by maximum junction temperature.

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: $T_J = 25^{\circ}\text{C}$, $V_{DD} = 32\text{V}$, $V_G = 10\text{V}$, $R_G = 25\ \Omega$, $L = 0.5\text{mH}$,
3. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 0.5\%$

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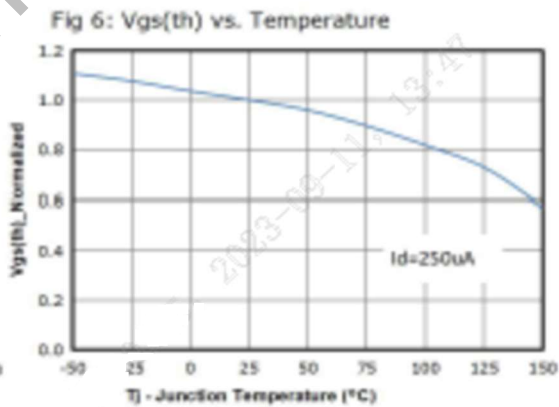
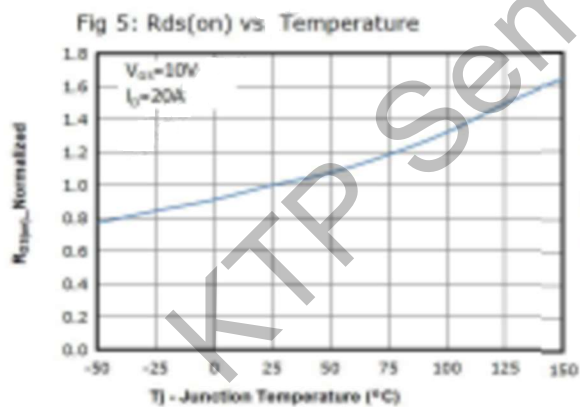
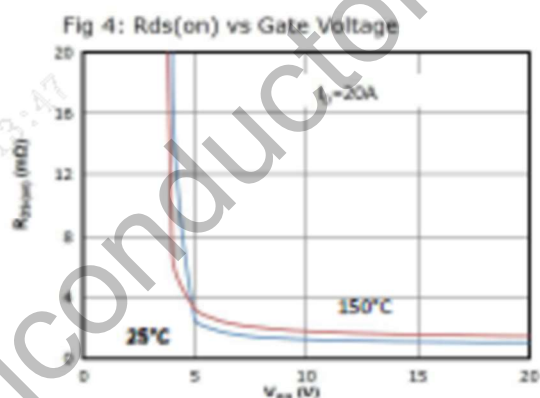
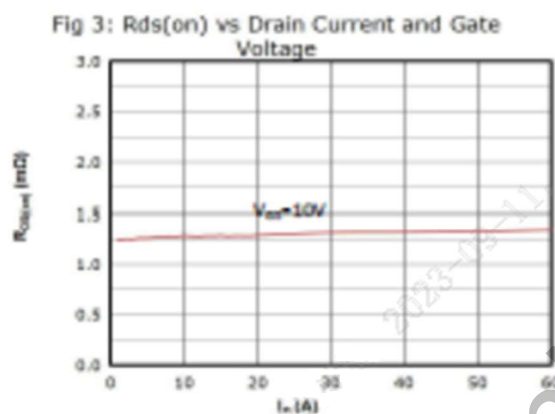
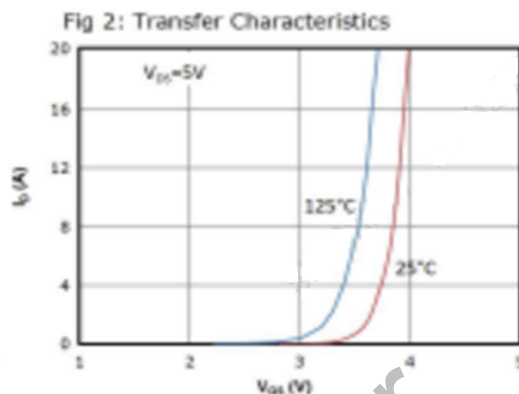
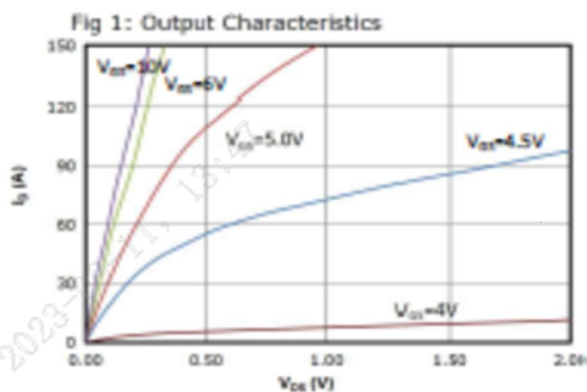
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Electrical Characteristic (TC=25°C unless otherwise noted)

Parameter	Symbol	Value			Unit	Test Condition
		Min.	Typ.	Max.		
Off Characteristic						
Drain-source breakdown voltage	BV_{DSS}	40	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=40V, V_{GS}=0V$
		-	-	100	μA	$V_{DS}=40V, TC=125^{\circ}C$
Gate-source leakage current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
On Characteristics						
Gate threshold voltage	$V_{GS(th)}$	1.0	1.6	2.2	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.3	1.6	m Ω	$V_{GS}=10V, I_D=20A$
Dynamic Characteristic						
Input Capacitance	C_{iss}	-	3900	-	PF	$V_{GS}=0V, V_{DS}=30V, f=1.0MHz$
Output Capacitance	C_{oss}	-	1000	-		
Reverse Transfer Capacitance	C_{rss}	-	55	-		
Switching Characteristics						
Turn-on delay time	$t_{d(on)}$	-	18	-	nS	$V_{GS}=10V, V_{DS}=30V, I_D=30A, R_G=25\Omega$
Turn-on Rise time	t_r	-	10	-		
Turn-off delay time	$t_{d(off)}$	-	64	-		
Turn-off Fall time	t_f	-	16	-		
Gate Total Charge	Q_G	-	60	-	nC	$V_{GS}=10V, V_{DS}=30V, I_D=30A$
Gate-Source Charge	Q_{gS}	-	20	-		
Gate-Drain Charge	Q_{gd}	-	9	-		
Drain-Source Diode Characteristics						
Body Diode Forward Voltage	V_{SD}	-	-	1.2	V	$V_{GS}=0V, I_{SD}=20A, T_J=25^{\circ}C$
Body Diode Forward Current	I_S	-	-	110	A	-
Body Diode Reverse Recovery Time	T_{rr}	-	76	-	ns	$T_J=25^{\circ}C, I_{SD}=20A, V_{GS}=0V, di/dt=100A/\mu s$
Body Diode Reverse Recovery Charge	Q_{rr}	-	80	-	nC	

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Fig 7: BVdss vs. Temperature

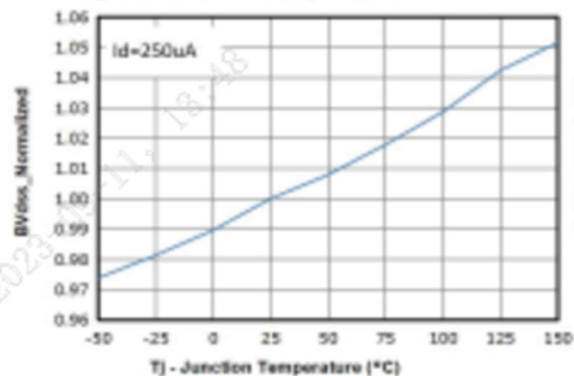


Fig 8: Capacitance Characteristics

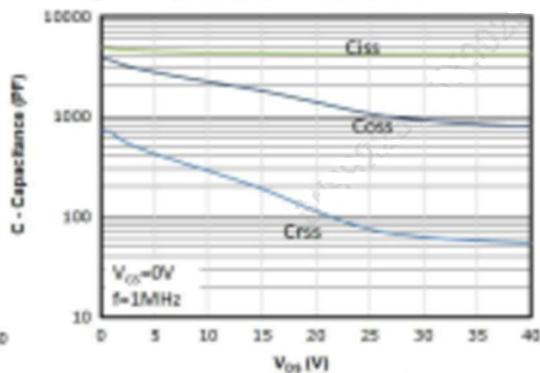


Fig 9: Gate Charge Characteristics

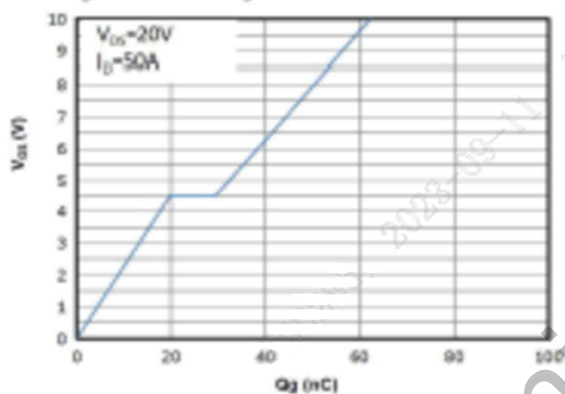


Fig 10: Body-diode Forward Characteristics

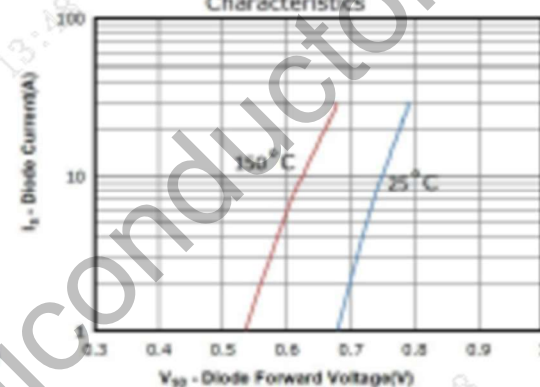


Fig 11: Power Dissipation

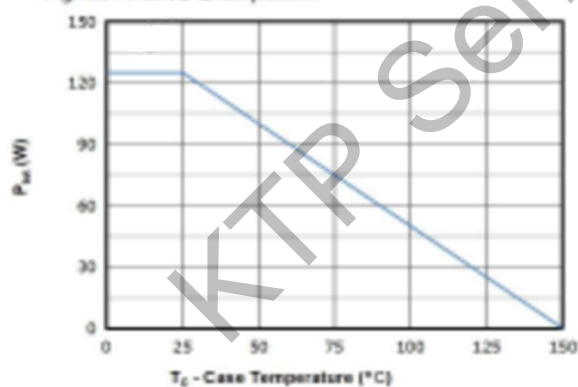
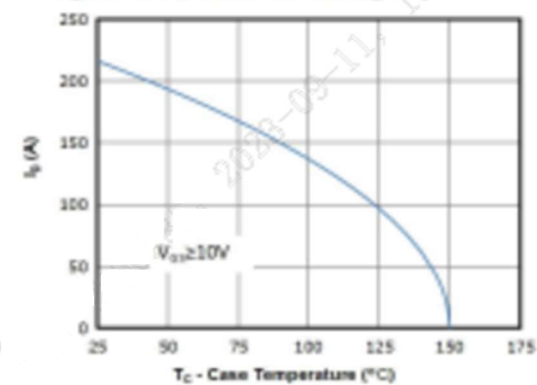


Fig 12: Drain Current Derating



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Fig 13: Safe Operating Area

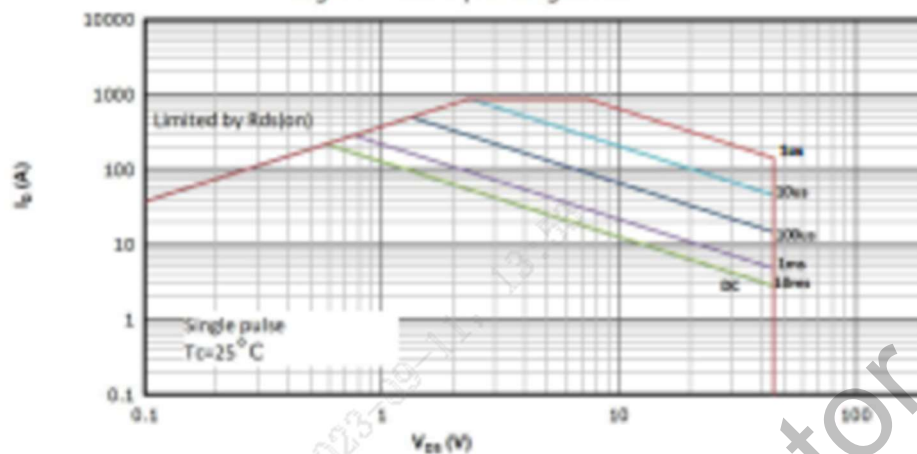
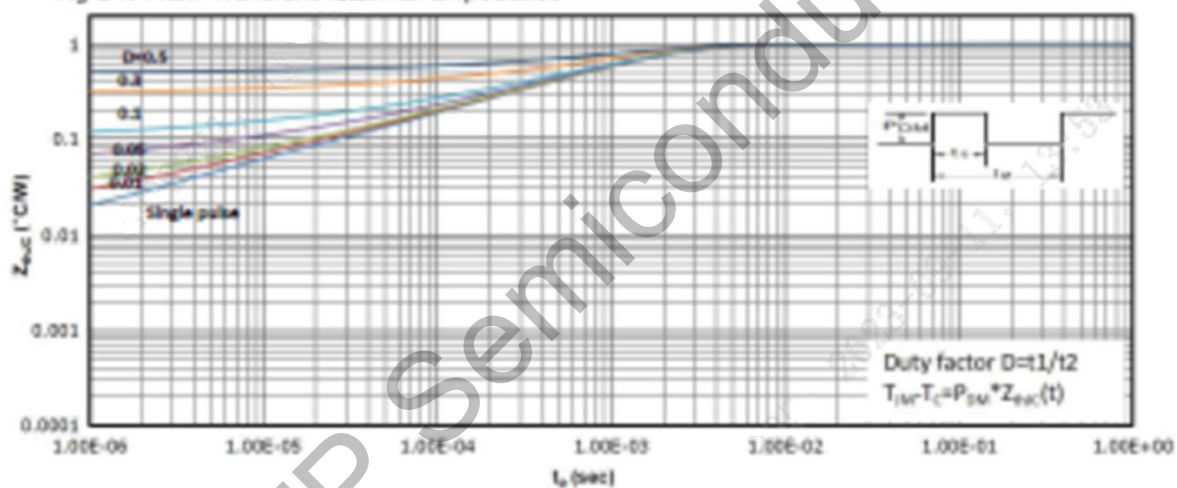


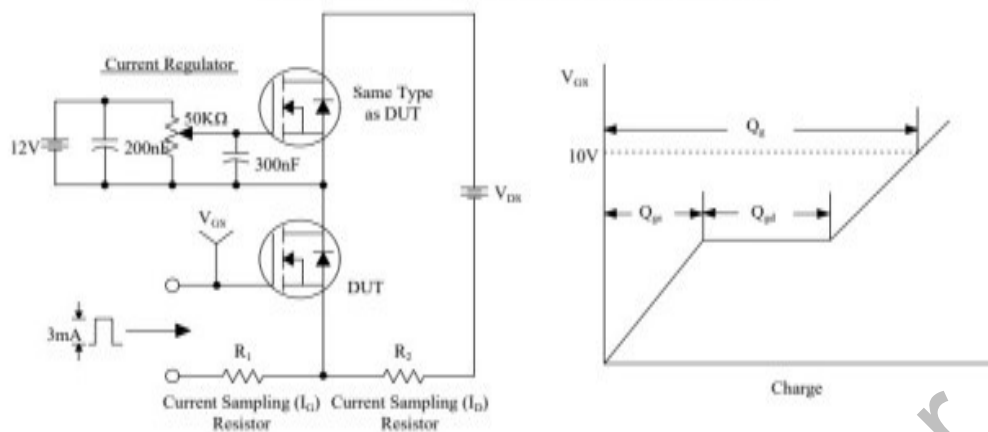
Fig 14: Max. Transient Thermal Impedance



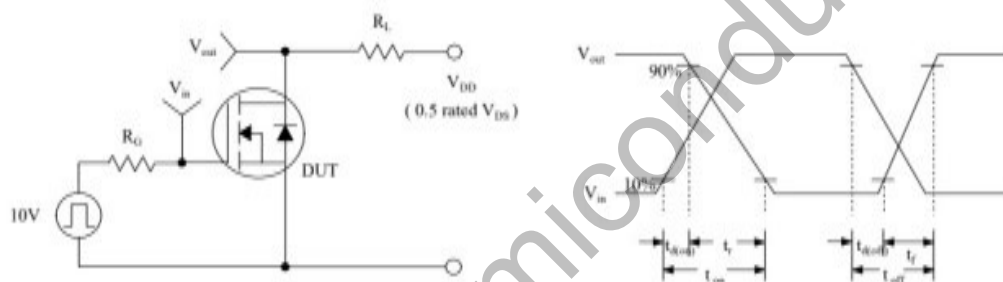
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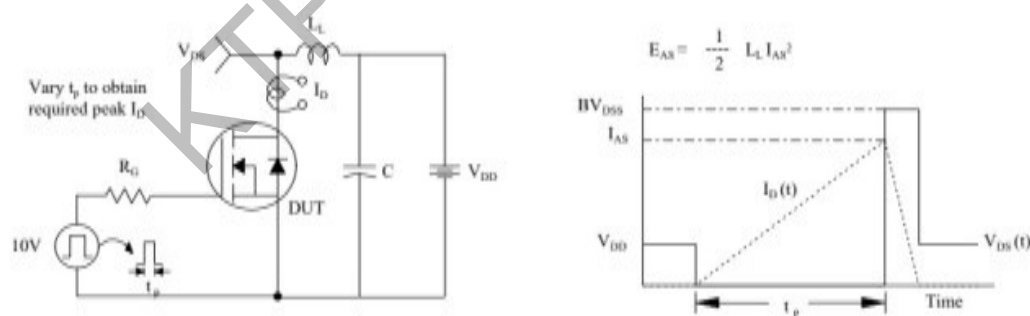
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



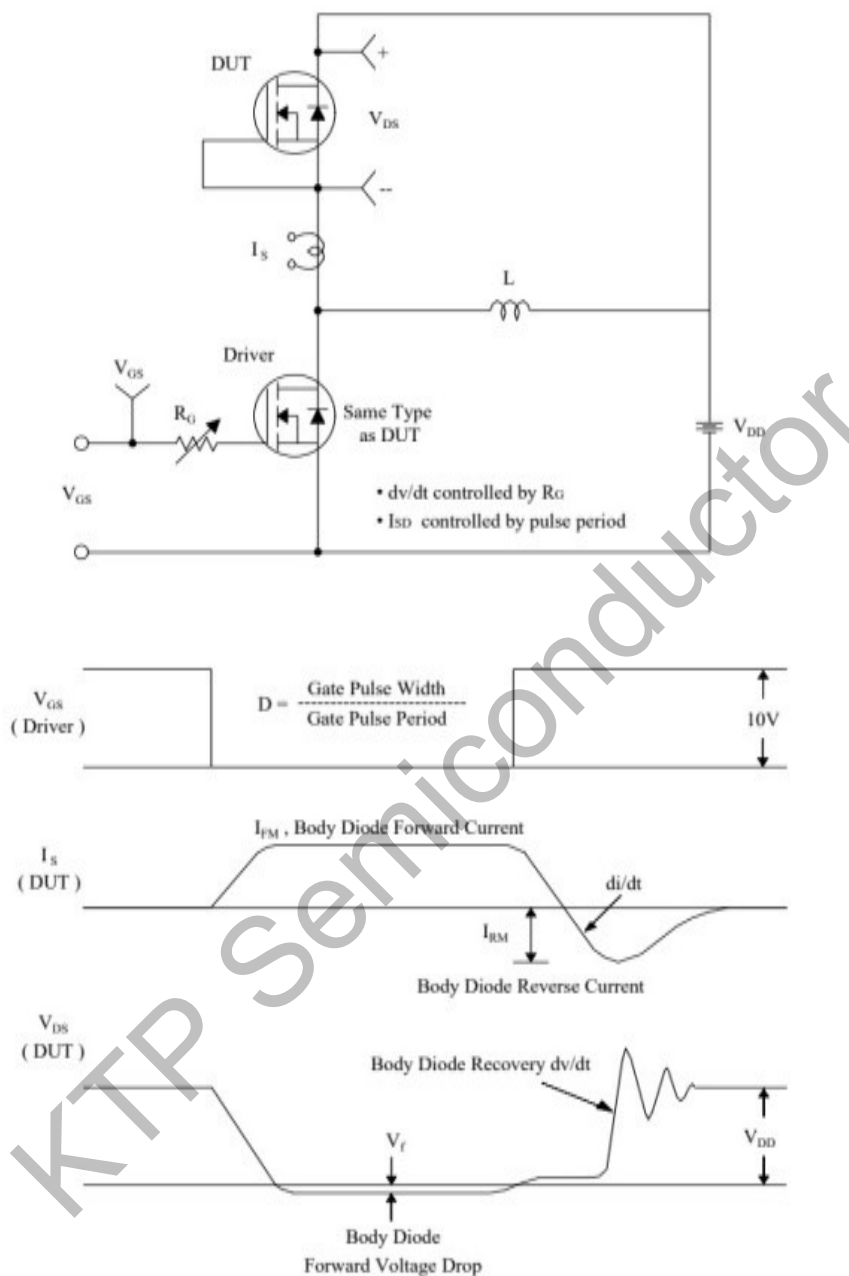
Unclamped Inductive Switching Test Circuit & Waveforms



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Peak Diode Recovery dv/dt Test Circuit & Waveforms

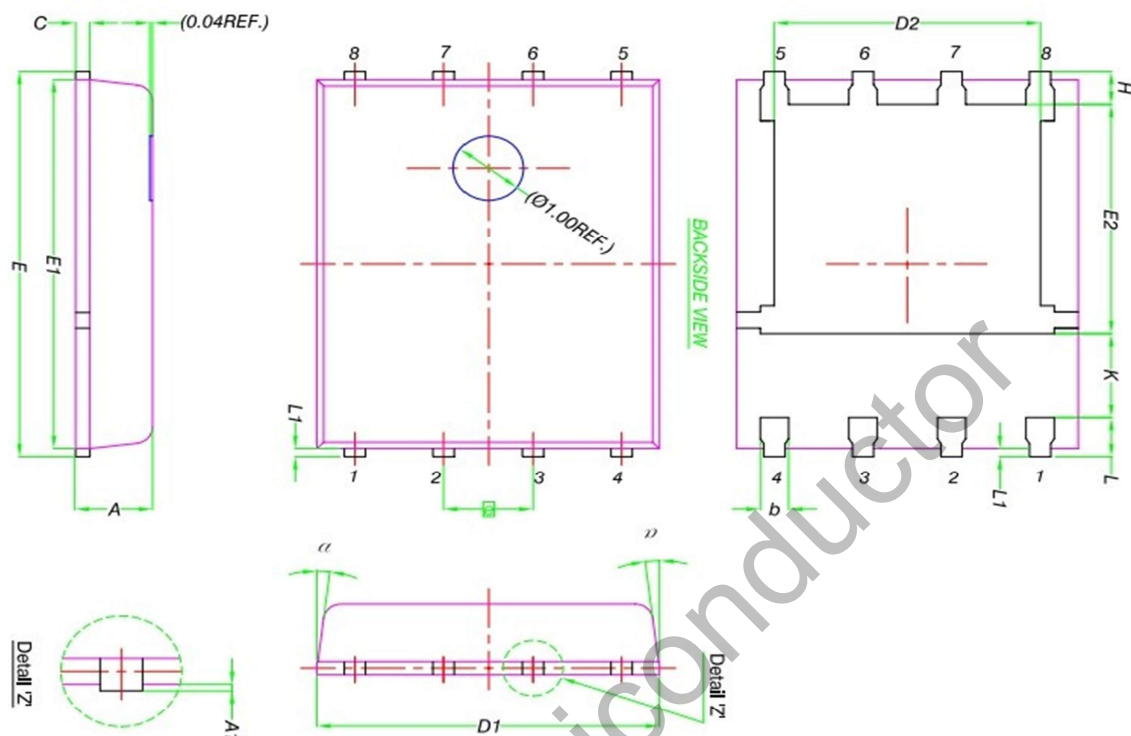


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Package Information

PDFN5*6-8L



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°

