

N-channel 600 V, 0.35 Ω typ., 11 A MDmesh™ M2 Power MOSFET in a TO-220FP wide creepage package

Datasheet - production data

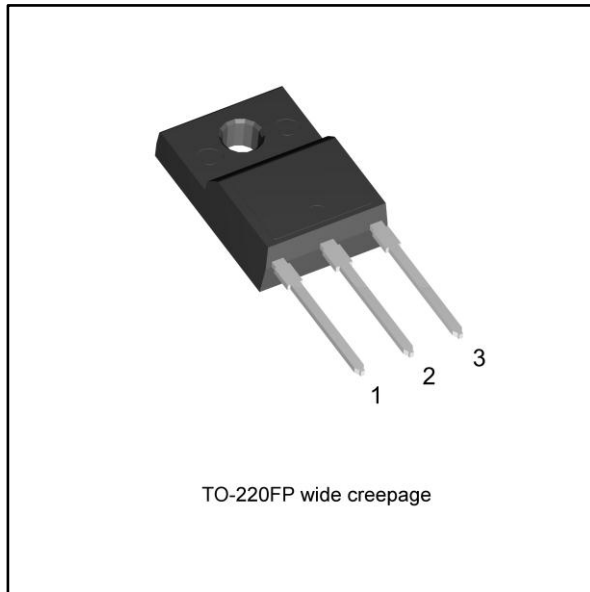
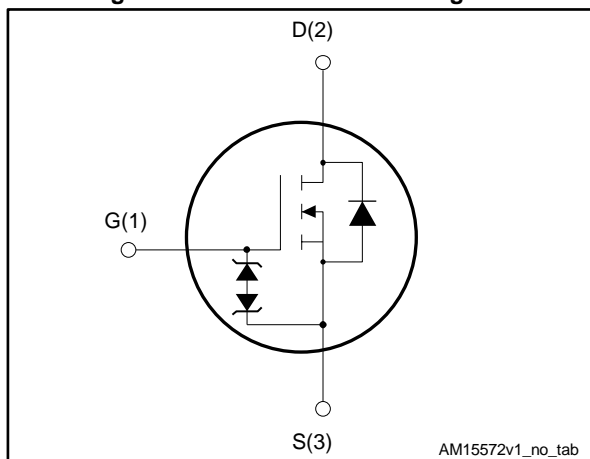


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
FH13N60K	600 V	0.38 Ω	11 A

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected
- Wide distance of 4.25 mm between the pins

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

The TO-220FP wide creepage package provides increased surface insulation for Power MOSFETs to prevent failure due to arcing, which can occur in polluted environments.

Table 1: Device summary

Order code	Marking	Package	Packaging
FH13N60K	FH13N60K	TO-220FP wide creepage	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate-source voltage	± 25	V
I _D	Drain current (continuous) at T _C = 25 °C	11 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100 °C	7 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	44	A
P _{TOT}	Total dissipation at T _C = 25 °C	25	W
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)	2500	V
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15	V/ns
dv/dt ⁽⁴⁾	MOSFET dv/dt ruggedness	50	
T _{stg}	Storage temperature range	- 55 to 150	°C
T _j	Operating junction temperature range		

Notes:

(1)Limited by maximum junction temperature.

(2)Pulse width limited by safe operating area.

(3)|I_{SD} ≤ 11 A, di/dt ≤ 400 A/μs; V_{DS(peak)} < V_{(BR)DSS}, V_{DD} = 400 V

(4)V_{DS} ≤ 480 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case max	5	°C/W
R _{thj-amb}	Thermal resistance junction-ambient max	62.5	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T _{jmax})	2.8	A
E _{AS}	Single pulse avalanche energy (starting T _j = 25°C, I _D = I _{AR} ; V _{DD} = 50 V)	125	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	600			V
I _{DSS}	Zero gate voltage drain current	V _{DS} = 600 V, V _{GS} = 0 V			1	μA
		V _{DS} = 600 V, V _{GS} = 0 V, T _C = 125 °C ⁽¹⁾			100	μA
I _{GSS}	Gate-body leakage current	V _{GS} = ± 25 V, V _{DS} = 0 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 5.5 A		0.35	0.38	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V	-	580	-	pF
C _{oss}	Output capacitance		-	32	-	pF
C _{riss}	Reverse transfer capacitance		-	1.1	-	pF
C _{oss eq.} ⁽¹⁾	Equivalent output capacitance	V _{DS} = 0 to 480 V, V _{GS} = 0 V	-	120	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz open drain	-	6.6	-	Ω
Q _g	Total gate charge	V _{DD} = 480 V, I _D = 11 A, V _{GS} = 10 V (see Figure 15: "Test circuit for gate charge behavior")	-	17	-	nC
Q _{gs}	Gate-source charge		-	2.5	-	nC
Q _{gd}	Gate-drain charge		-	9	-	nC

Notes:

⁽¹⁾C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 300 V, I _D = 5.5 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform")	-	11	-	ns
t _r	Rise time		-	10	-	ns
t _{d(off)}	Turn-off delay time		-	41	-	ns
t _f	Fall time		-	9.5	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 11 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 11 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	297		ns
Q_{rr}	Reverse recovery charge		-	2.8		μC
I_{RRM}	Reverse recovery current		-	18.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 11 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$, (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	394		ns
Q_{rr}	Reverse recovery charge		-	3.8		μC
I_{RRM}	Reverse recovery current		-	19		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

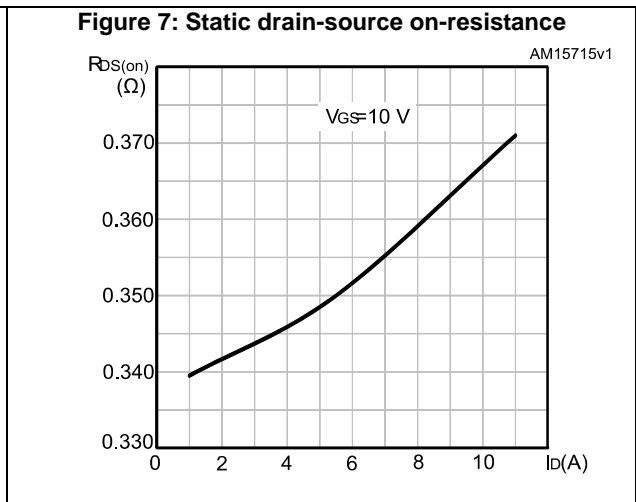
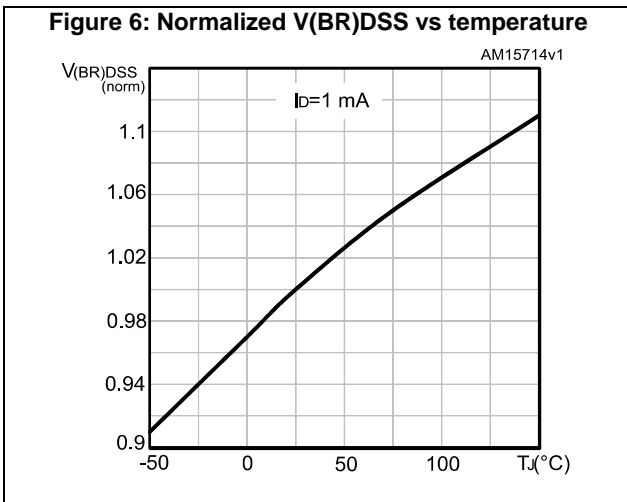
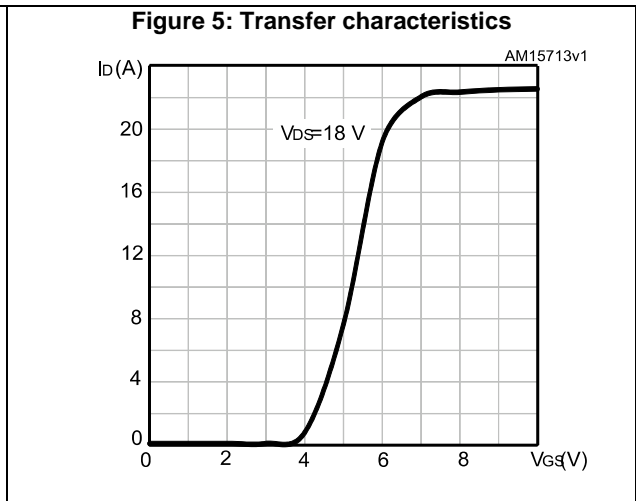
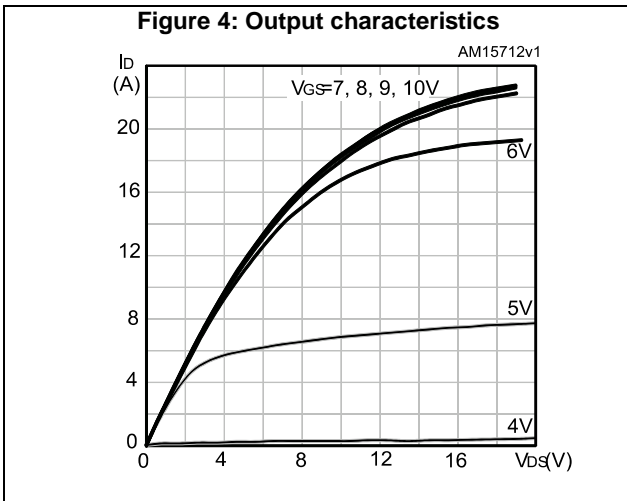
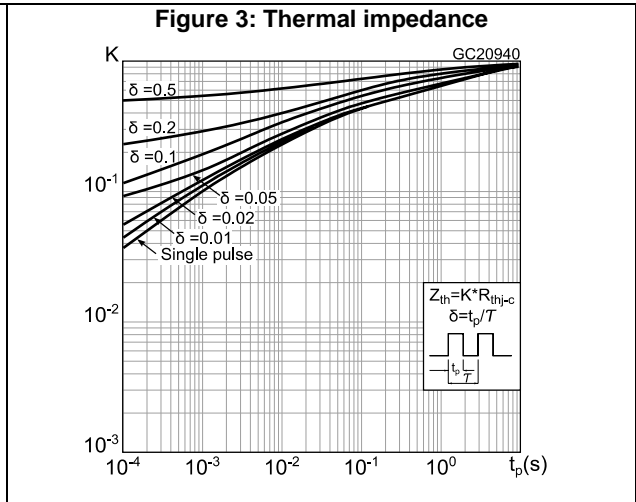
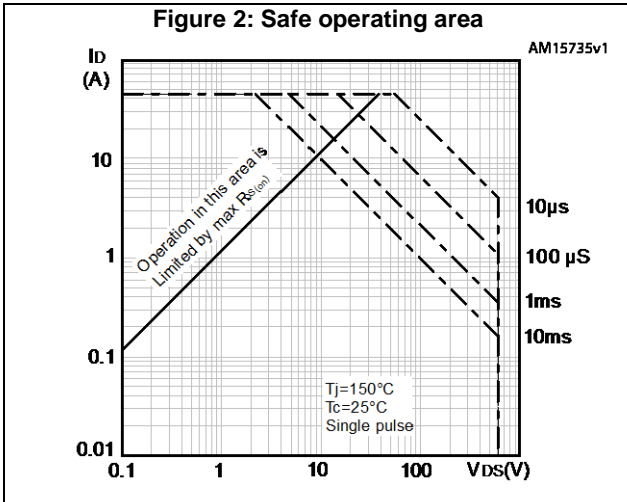


Figure 8: Gate charge vs gate-source voltage

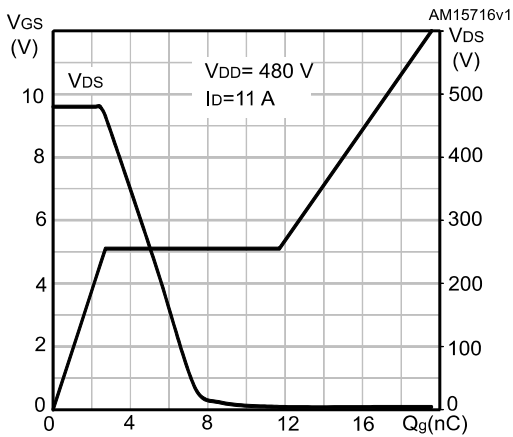


Figure 9: Capacitance variations

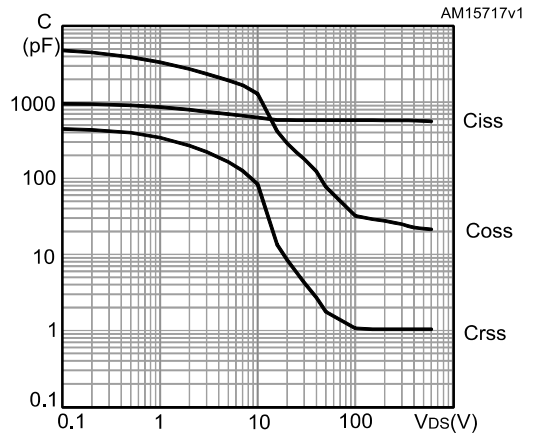


Figure 10: Normalized gate threshold voltage vs temperature

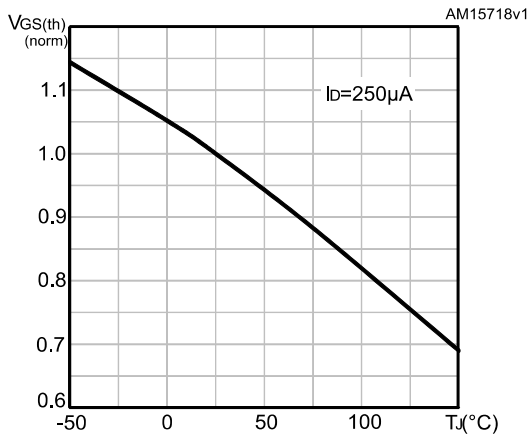


Figure 11: Normalized on-resistance vs temperature

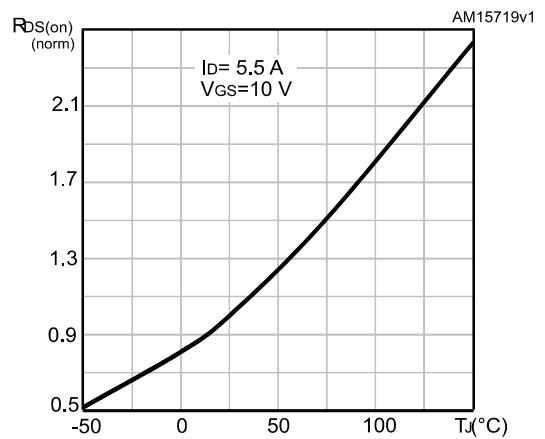


Figure 12: Source-drain diode forward characteristics

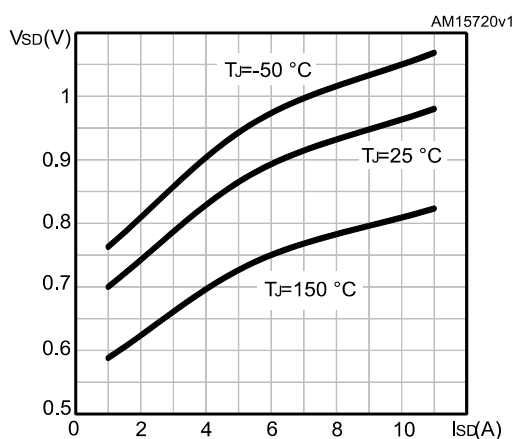
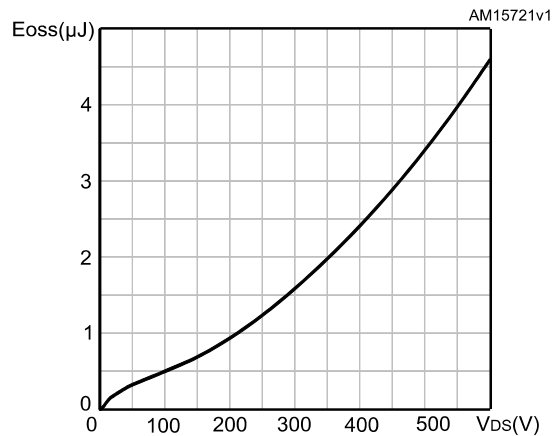


Figure 13: Output capacitance stored energy



3 Test circuits

Figure 14: Test circuit for resistive load switching times



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Figure 15: Test circuit for gate charge behavior



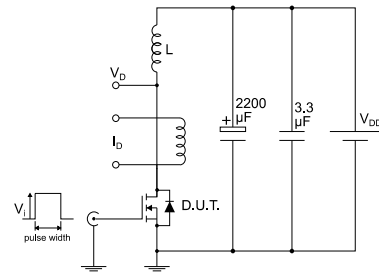
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Figure 16: Test circuit for inductive load switching and diode recovery times



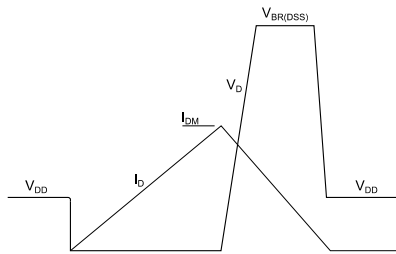
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Figure 17: Unclamped inductive load test circuit



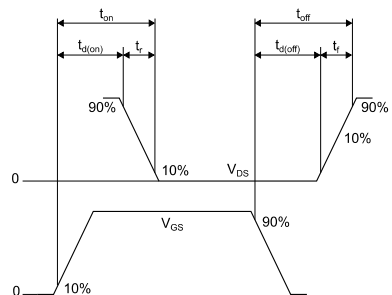
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Figure 18: Unclamped inductive waveform



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Figure 19: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP wide creepage package information

Figure 20: TO-220FP wide creepage package outline

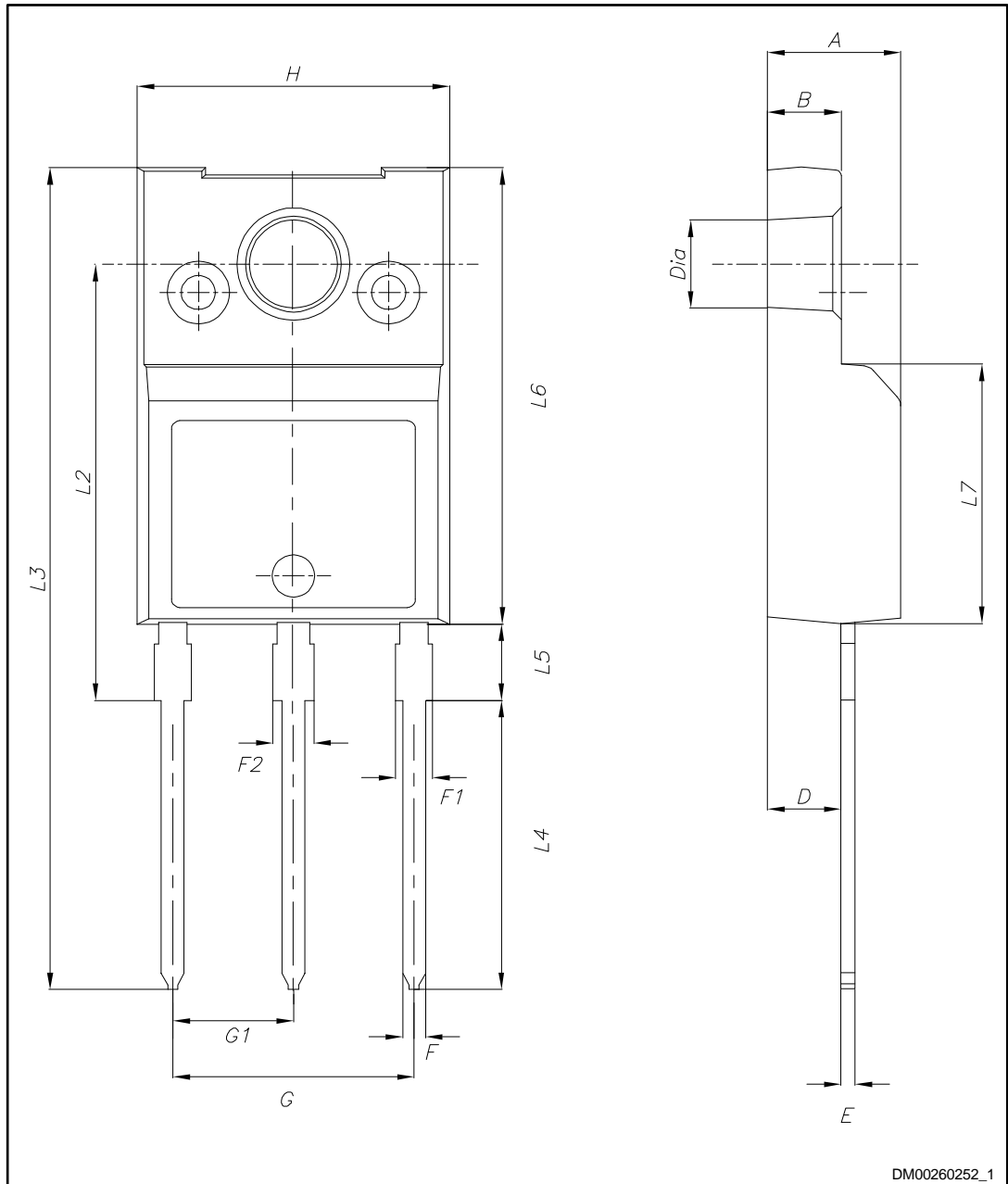


Table 9: TO-220FP wide creepage package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.60	4.70	4.80
B	2.50	2.60	2.70
D	2.49	2.59	2.69
E	0.46		0.59
F	0.76		0.89
F1	0.96		1.25
F2	1.11		1.40
G	8.40	8.50	8.60
G1	4.15	4.25	4.35
H	10.90	11.00	11.10
L2	15.25	15.40	15.55
L3	28.70	29.00	29.30
L4	10.00	10.20	10.40
L5	2.55	2.70	2.85
L6	16.00	16.10	16.20
L7	9.05	9.15	9.25
Dia	3.00	3.10	3.20

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
11-Oct-2016	1	Initial release

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