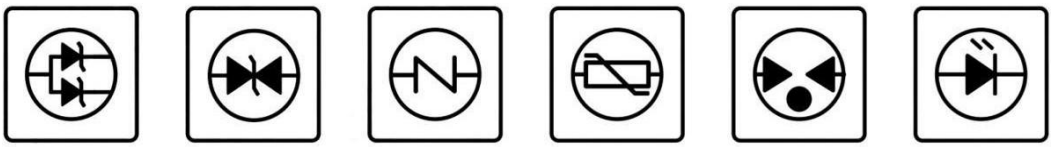
MSKSEMI 美森科
SEMICONDUCTOR



MS16N65S

Product specification

Description

The MS16N65S uses advanced trench technology to provide excellent RDS(ON), low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

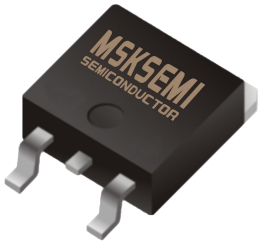
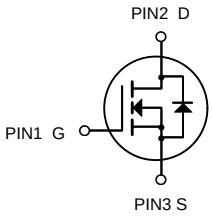
General Features

- V_{DS}= 650V I_D =16A
- $R_{DS(ON)}$< 0.55Ω @ V_{GS}=10V

Application

- Battery protection
- Load switch
- Uninterruptible power supply

Reference News

PACKAGE OUTLINE	N-Channel MOSFET	Marking
		MSKSEMI 16N65 MS ***
TO-263		MS16N65S

Note : ****Representative production cycle

Absolute Maximum Ratings

Symbol	Parameter	Limit	Units
V_{DS}	Drain-Source Voltage	650	V
V_{GS}	Gate-Source Voltage	±30	V
I_D	Drain Current-Continuous	16	A
I_{DM}	Drain Current-Pulsed [a]	64	A
P_D	Maximum Power Dissipation @ T_C = 25° C	180	W
	- Derate above 25° C	1.1	W/ C
E_{AS}	Single Pulsed Avalanche Energy [d]	1000	mJ
I_{AS}	Single Pulsed Avalanche Current [d]	64	A
T_J,T_{stg}	Operating and Store Temperature Range	-55 to 175	°C
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.69	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	°C/W

Electrical Characteristics T_C = 25° C unless otherwise noted

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	650	--	--	V	V_{GS}=0V, I_D=250uA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1.0	uA	V_{DS}=650V, V_{GS}=0V
		--	--	100		V_{DS}=520V, V_{GS}=0V, T_J =125℃
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	V_{GS}=+30V, V_{DS}=0V
		--	--	-100		V_{GS}=-30V, V_{DS}=0V
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance[4]	--	0.45	0.55	Ω	V_{GS}=10V, I_D=8A
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=V_{GS}, I_D=250uA
gfs	Forward Transconductance[4]	--	15	--	S	V_{DS}=15V,I_D=8A
C_{iss}	Input Capacitance	--	2442	--	pF	V_{GS}=0V, V_{DS}=25V, f=1.0MHz
C_{rss}	Reverse Transfer Capacitance	--	18.5	--		
C_{oss}	Output Capacitance	--	218	--		
Q_g	Total Gate Charge	--	54	--	nC	V_{DD}=325V, I_D=16A, V_{GS}=0 to 10V
Q_{gs}	Gate-to-Source Charge	--	12	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	21	--		
$t_{d(ON)}$	Turn-on Delay Time	--	15	--	nS	V_{DD}=325V, I_D=16A, V_{GS}= 10V R_G=6.1 Ω
t_{rise}	Rise Time	--	52	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	59	--		
t_{fall}	Fall Time	--	72	--		
I_{SD}	Continuous Source Current[4]	--	--	16	A	Integral PN-diode in MOSFET
I_{SM}	Pulsed Source Current[4]	--	--	64		
V_{SD}	Diode Forward Voltage	--	--	1.5	V	I_S=16A, V_{GS}=0V
trr	Reverse recovery time	--	380	--	V	V_{GS}=0V ,I_F=16A, di_F/dt=100A/μs
Qrr	Reverse recovery charge	--	2.6	--	uC	

Note:

[1] T_J=+25℃ to +150℃

[2] Repetitive rating; pulse width limited by maximum junction temperature.

[3] I_{SD}= 16Adi/dt < 100 A/μs, V_{DD} < BV_{DSS}, T_J=+150℃.

[4] Pulse width≤380μs; duty cycle≤2%.

Typical Characteristics

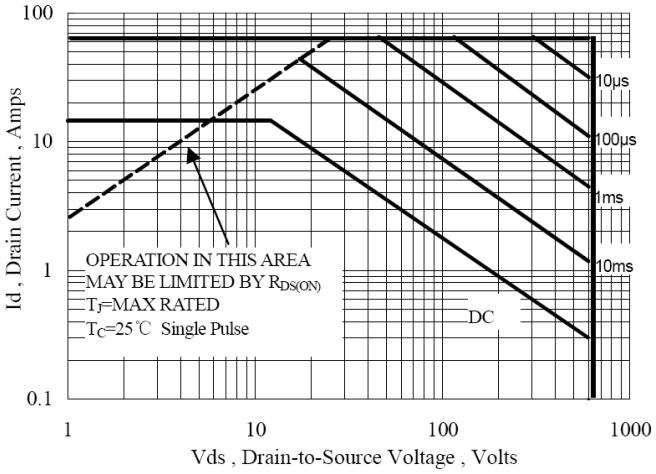


Figure 1 Maximun Forward Bias Safe Operating Area

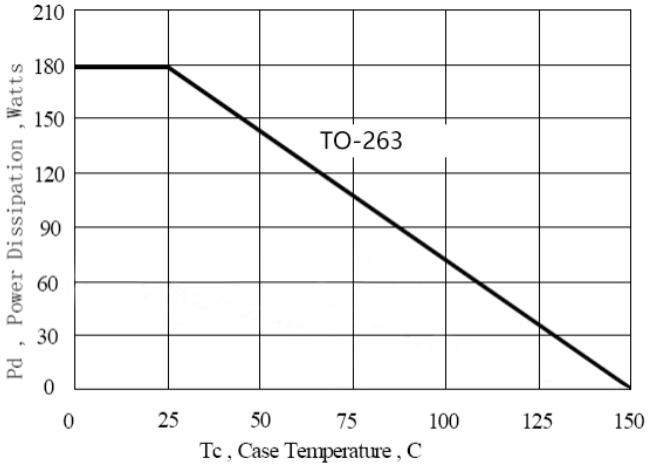


Figure 2 Maximun Power Dissipation vs Case Temperature

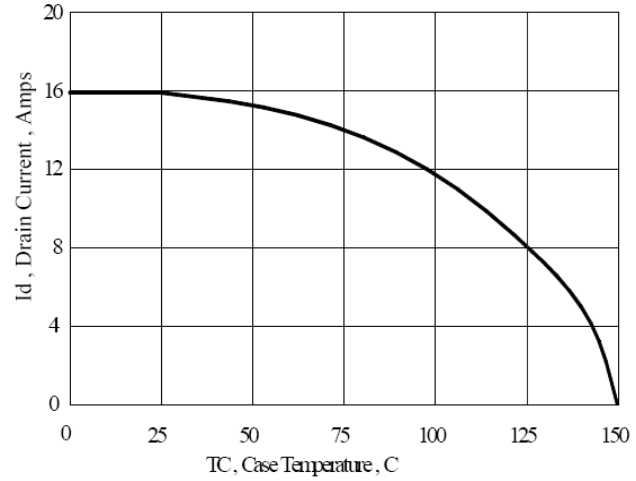


Figure 3 Maximum Continuous Drain Current vs Case Temperatur

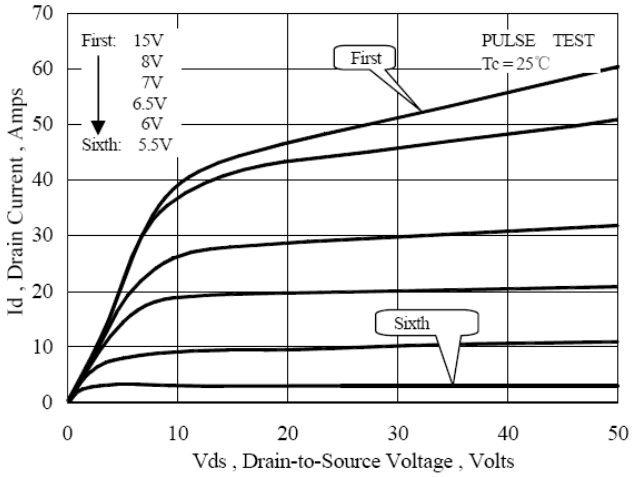


Figure 4 Typical Output Characteristics

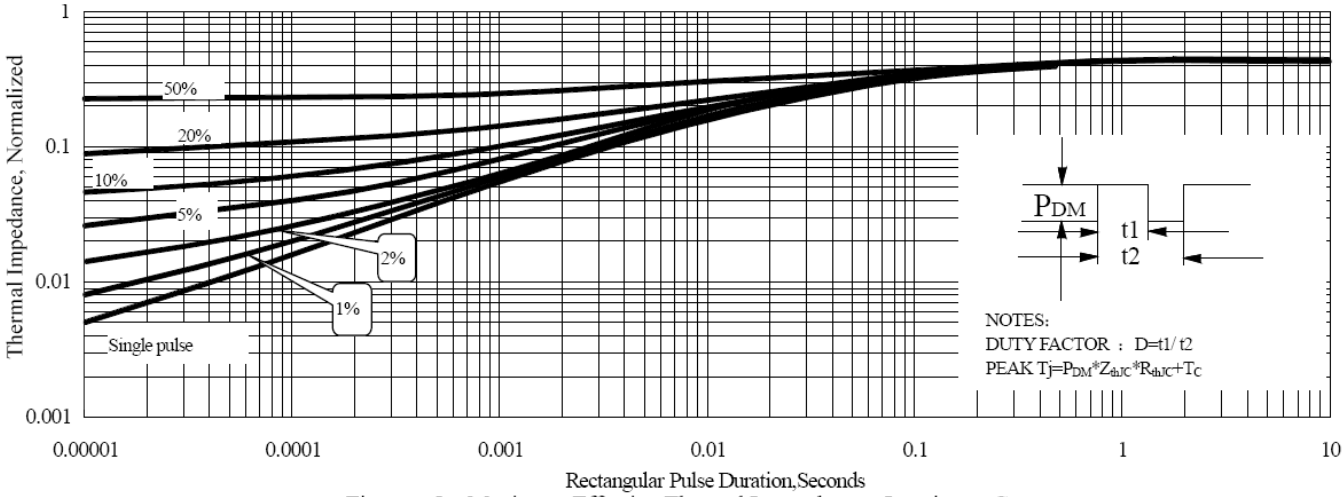


Figure 5 Maximum Effective Thermal Impendance , Junction to Case

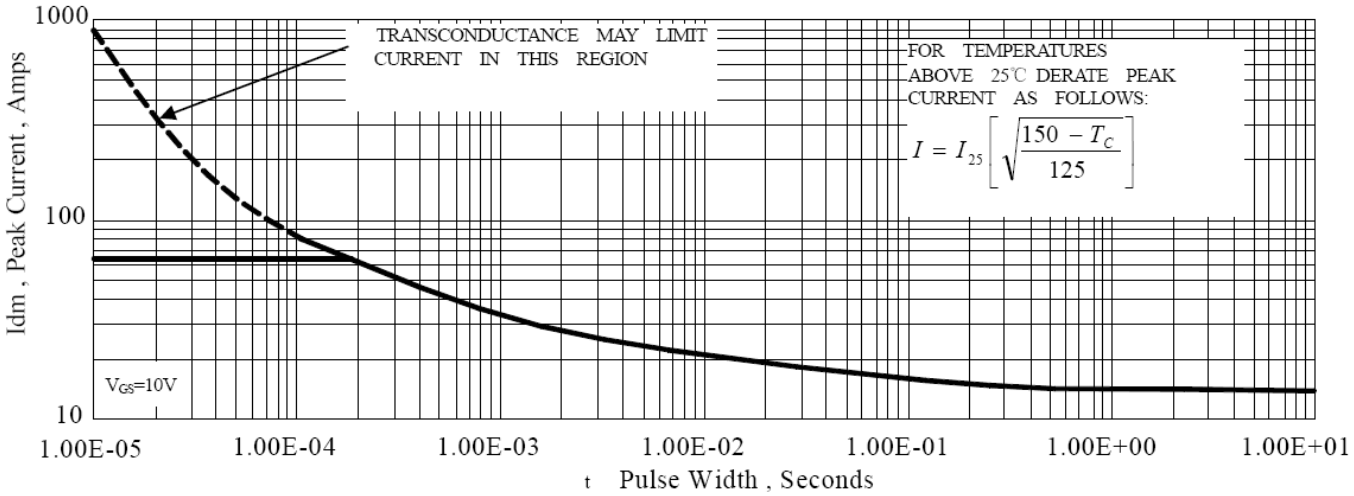


Figure 6 Maximun Peak Current Capability

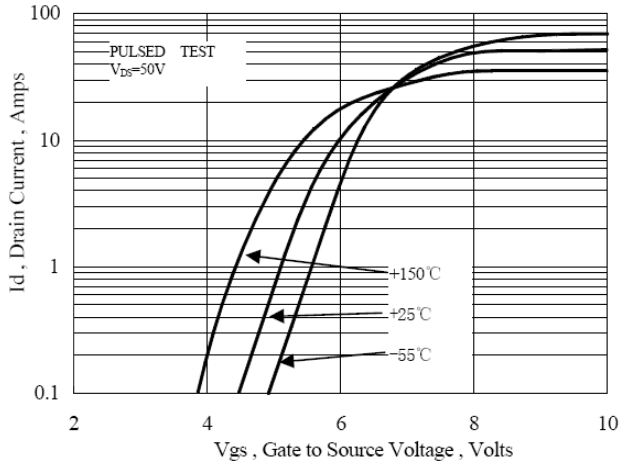


Figure 7 Typical Transfer Characteristics

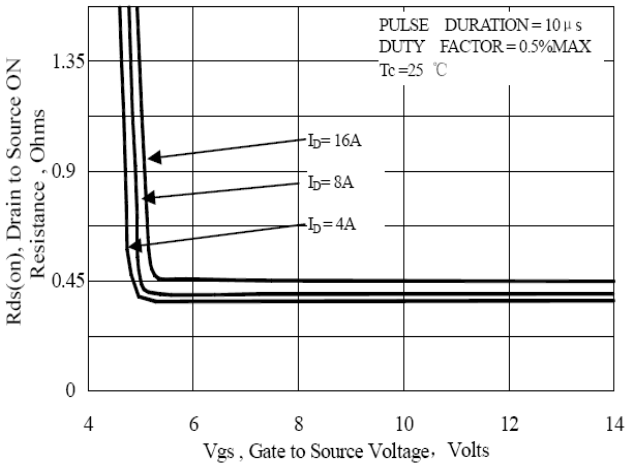


Figure 8 Typical Drain to Source ON Resistance vs Gate Voltage

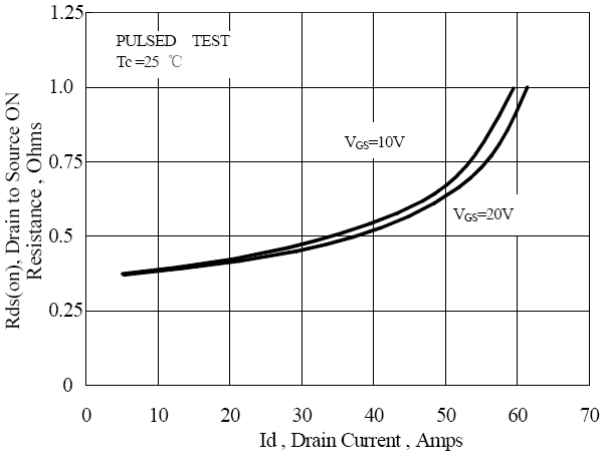


Figure 9 Typical Drain to Source ON Resistance vs Drain Current

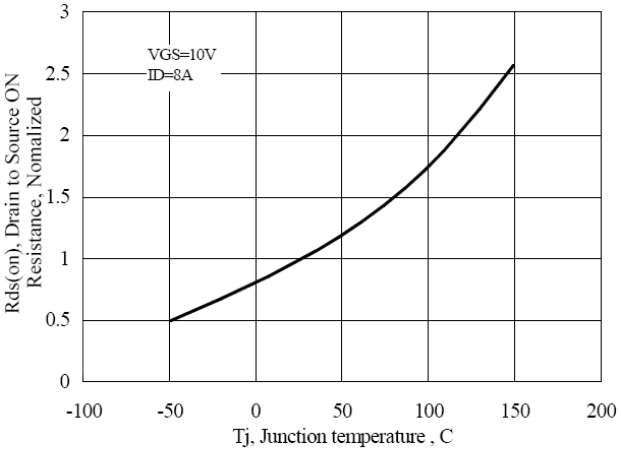


Figure 10 Typical Drian to Source on Resistance vs Junction Temperature

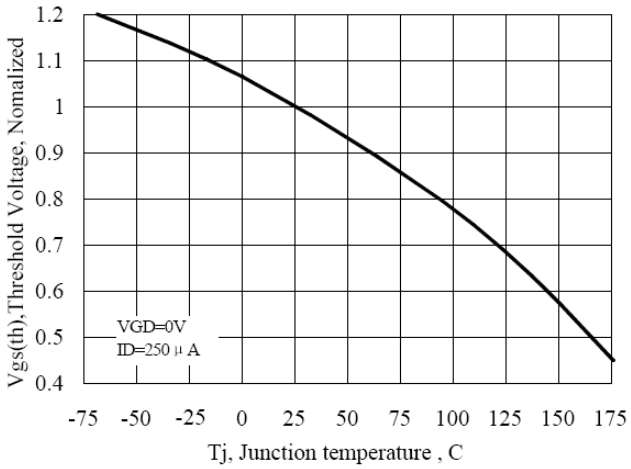


Figure 11 Typical Theshold Voltage vs Junction Temperature

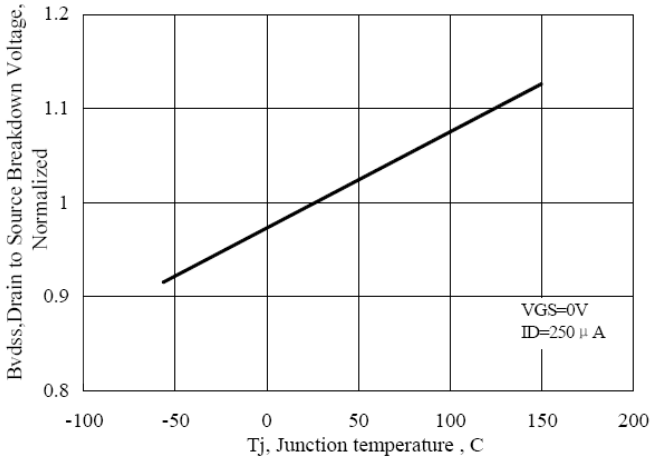


Figure 12 Typical Breakdown Voltage vs Junction Temperature

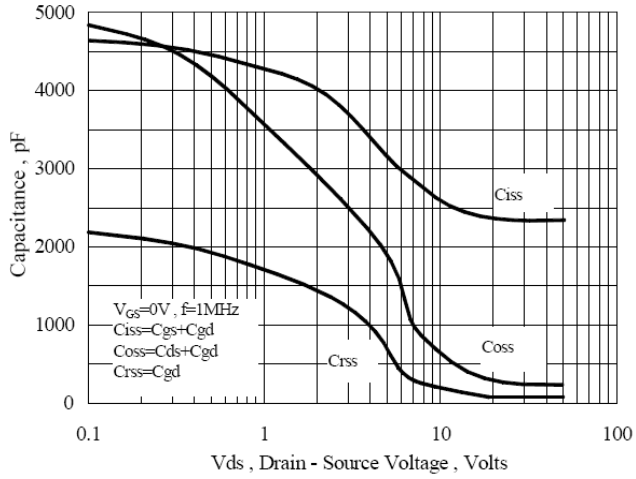


Figure 13 Typical Capacitance vs Drain to Source Voltage

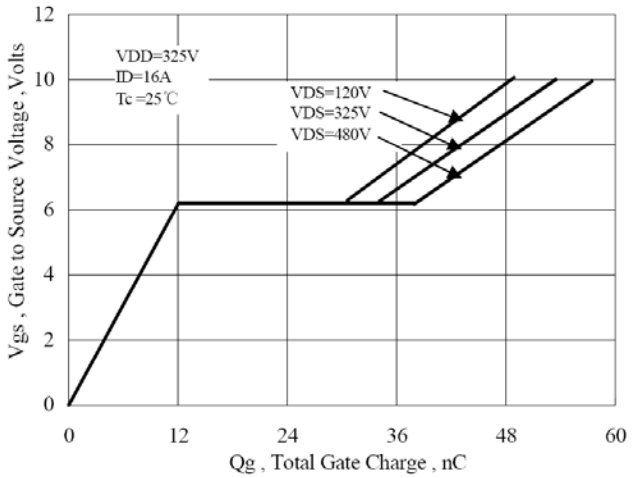


Figure 14 Typical Gate Charge vs Gate to Source Voltage

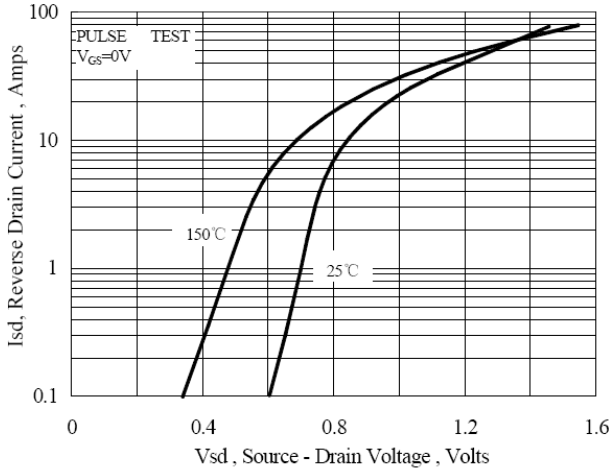


Figure 15 Typical Body Diode Transfer Characteristics

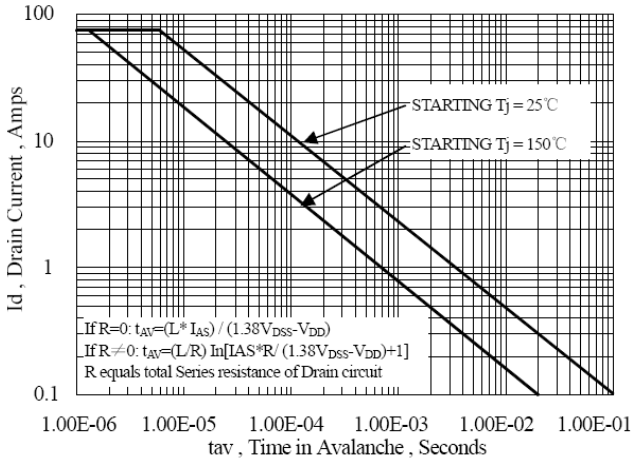


Figure 16 Unclamped Inductive Switching Capability

Test Circuits and Waveforms

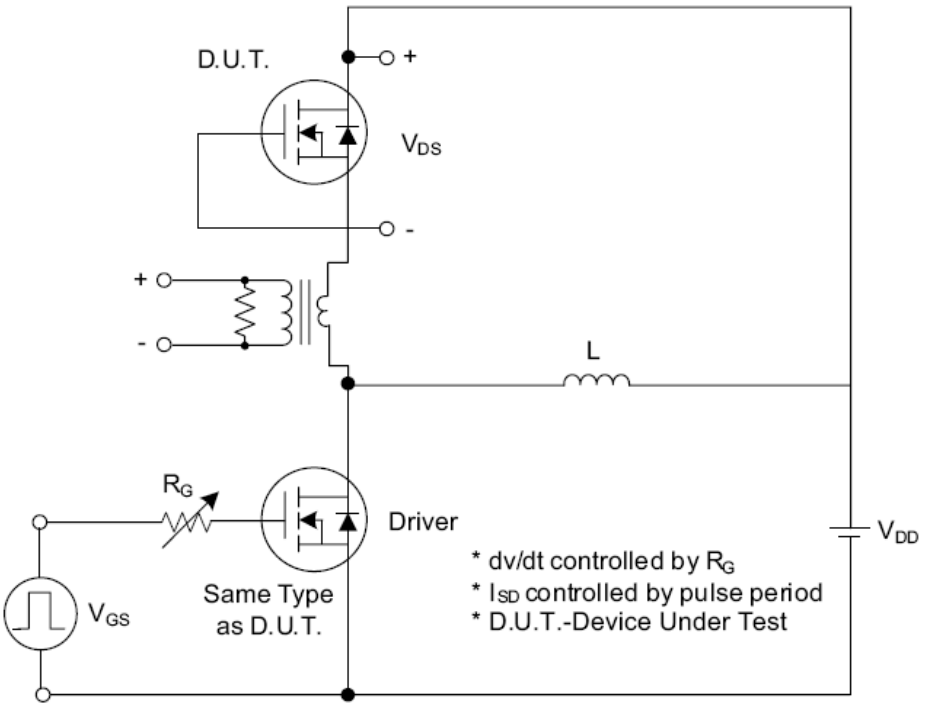


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

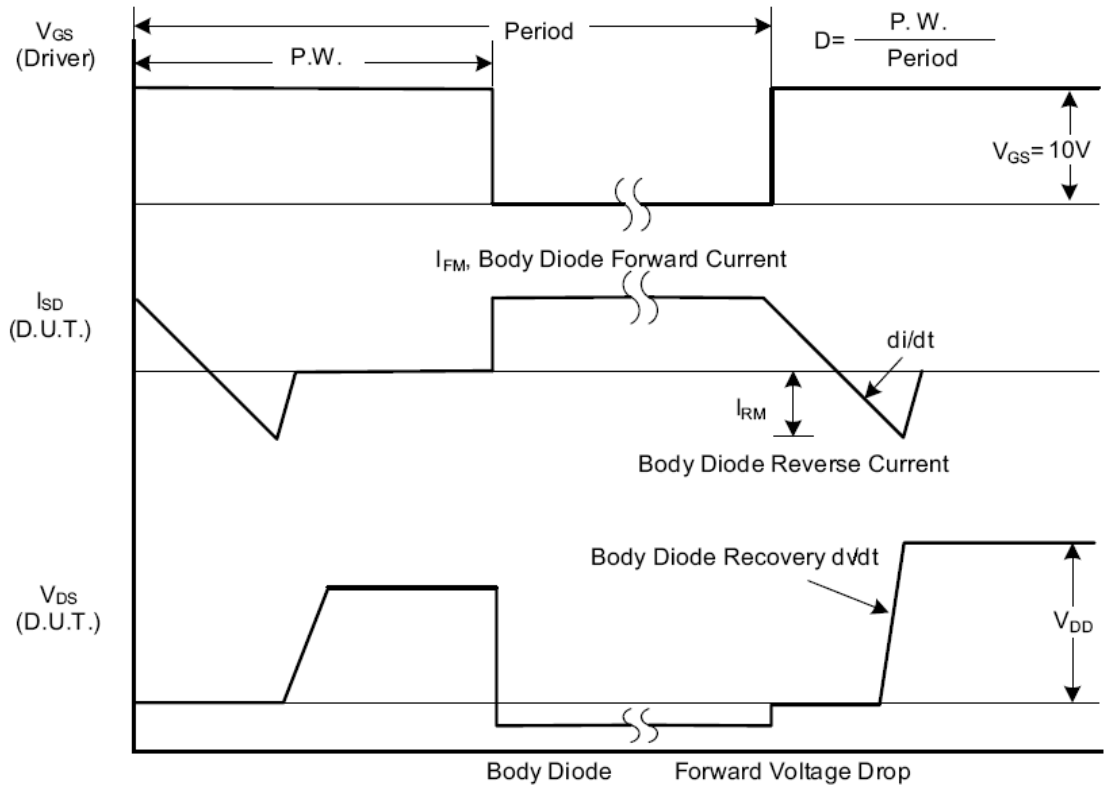


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

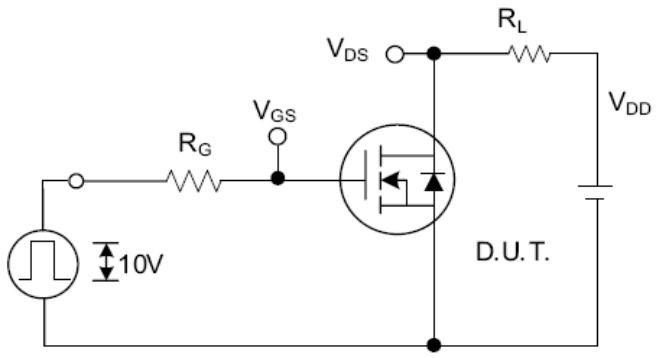


Fig. 2.1 Switching Test Circuit

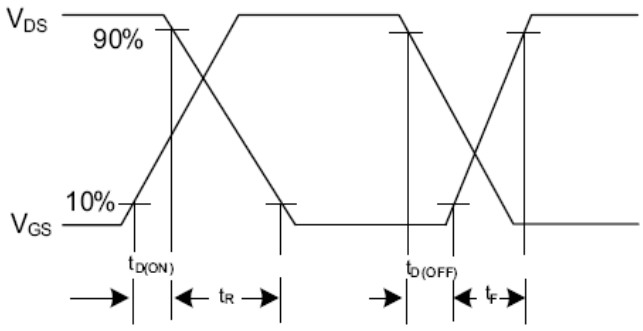


Fig. 2.2 Switching Waveforms

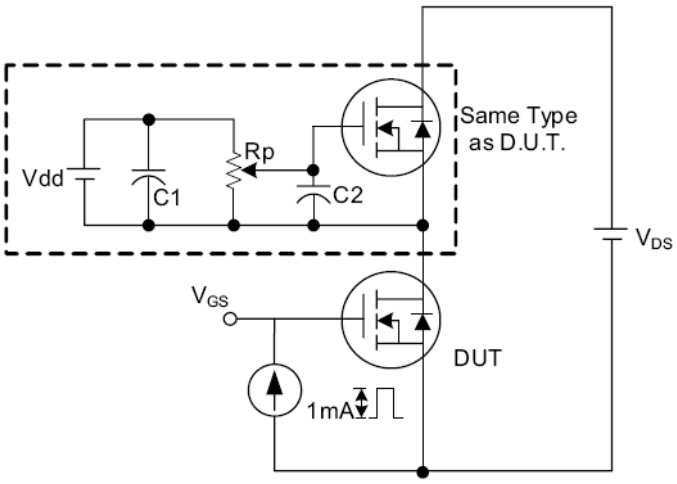


Fig. 3 . 1 Gate Charge Test Circuit

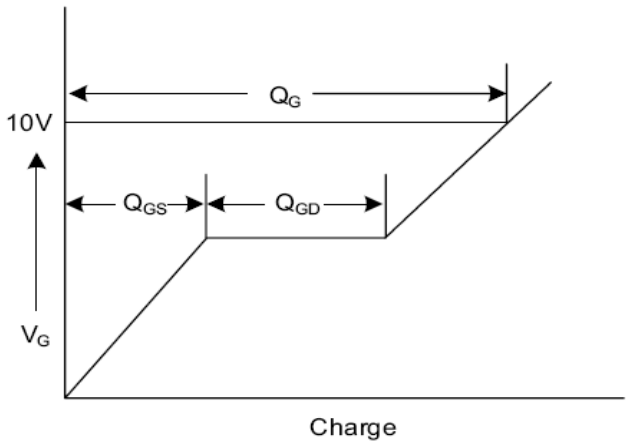


Fig. 3 . 2 Gate Charge Waveform

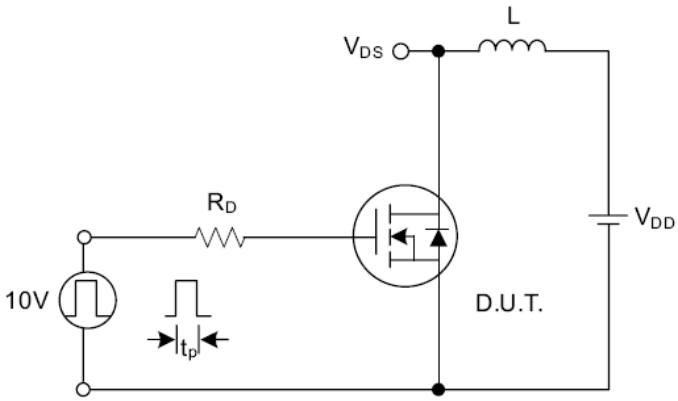


Fig. 4.1 Unclamped Inductive Switching Test Circuit

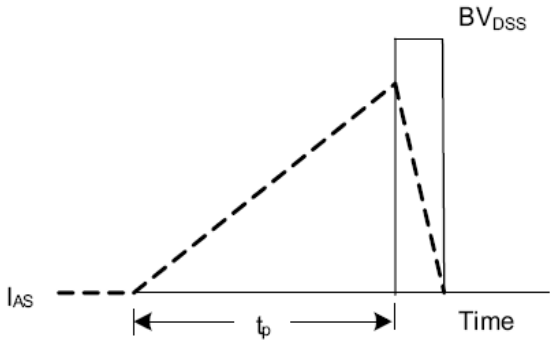
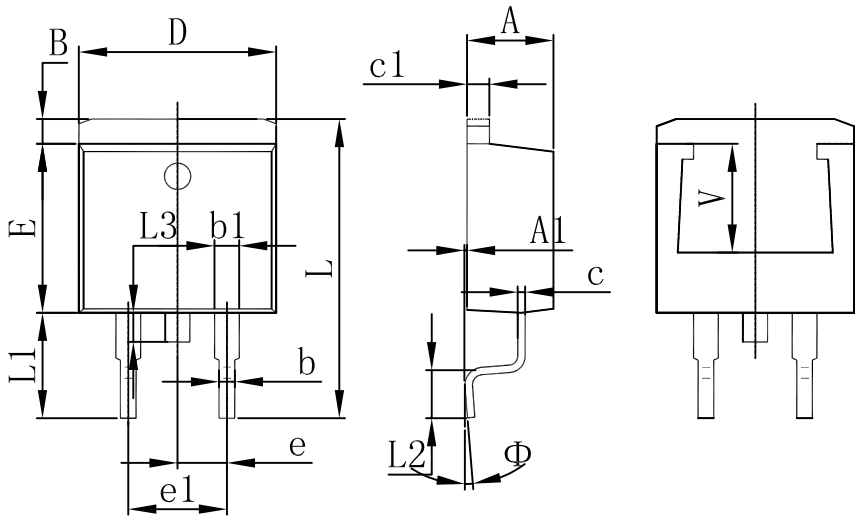


Fig. 4.2 Unclamped Inductive Switching Waveforms

TO-263 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.	4.	0.	0.184
A1	4700.	6700.	1760.	0.006
B	0001.	1501.	0000.	0.056
b	1200.	4200.	0440.	0.036
b1	7101.	9101.	0280.	0.054
c	1700.	3700.	0460.	0.021
c1	3101.	5301.	0120.	0.054
D	10.010	10.370	0.394	0.406
E	8.500	8.900	0.335	0.350
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
L	14.940	15.500	0.588	0.610
L1	4.	5.	0.	0.215
L2	9502.	4502.	1950.	0.108
L3	3401.	7401.	0920.	0.067
Φ	300	700	051	8°
V	0° 5.600 REF. 8°		0° 0.220REF.	

REEL SPECIFICATION

P/N	PKG	QTY
MS16N65S	TO-263	800

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