

# **JL7012A 6 Datasheet**

**Zhuhai Jieli Technology Co.,LTD**

**Version: 1.0**

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## JL7012A 6 Features

### CPU

- 32bit Dual-Core DSP
- Maximum speed 160MHz
- 32KB ICache and 16KB DCache
- IEEE754 Single precision FPU
- Mathematical accelerate engine
- Interrupts with 8 priority level

### Memory

- On-chip 640KB SRAM
- Support MMU
- Built-In Flash
- SPI PSRAM controller

### Clocks

- On-chip 16 MHz clock oscillator
- On-chip 200 kHz lower-temperature-drift clock oscillator
- 24 MHz crystal oscillator
- 32.768 kHz crystal oscillator

### DSP Audio Processing

- SBC/mSBC encoder and decoder
- Support MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV, AIF, AIFC audio decoding
- Packet Loss Concealment (PLC) for voice processing
- Single/Dual MIC Environmental Noise Cancellation (ENC)
- Multi-band DRC limiter
- Multi-band EQ configuration for voice Effects

### Audio Codec

- Two channels 24-bit DAC, SNR  $\geq$  104dB
- Four channels 24-bit ADC, SNR  $\geq$  95dB
- Audio DAC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz/64kHz/88.2kHz/96kHz are supported

- Audio ADC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz are supported
- Support four digital/analog MIC inputs
- Four channels analog audio inputs
- Audio DAC support differential cap-less mode or single-ended mode
- Direct drive 16ohm/32ohm Speaker loading

### Bluetooth

- Compliant with Bluetooth V5.3+BR+EDR+BLE specification
- Support AoA/AoD direction finding
- Support LE audio BIS/CIS full function
- Meet class2 and class3 transmitting power requirement
- Maximum +9dbm transmitting power
- EDR receiver with minimum -95dBm sensitivity
- Support a2dp\avctp\avdtp\avrcp\hfp\spp\smpl\att\gap\gatt\rfcomm\sdpl2cap profile bap 1.0\pacs 1.0\ccp 1.0\mcp 1.0\micp 1.0\vcp 1.0\csip 1.0 a2dp 1.3.2\avctp 1.4\avdtp 1.3\avrcp 1.6.2\hfp 1.8\spp 1.2\rfcomm 1.1\pnp 1.3\hid 1.1.1\sdp core5.3\l2cap core 5.3

### Graphics

- 2D Graphics accelerator
- Support crop, scale, rotation process
- Support multiple data format graphics
- SPI and QSPI display driver

### Peripherals

- One full speed USB OTG controller
- One SD host controller for eMMC/SD
- Six multi-function 32-bit timers, support capture and PWM mode
- Four UART interface, UART0,UART1&UART2 support DMA
- Two I2C Master/Slave interface

- Four SPI Master/Slave interface
- I2S Master/Slave interface
- QDEC
- Low power CapSense
- 13-channel 10-bit ADC for analog sampling
- 4-channel Motor PWM controller
- 40 Individually programmable and multiplexed GPIO pins
- Up to 12 external interrupt/wake-up source(low power available,can be multiplexed to any I/O)

### PMU

- Built-in lithium battery charging manager,up to 200mA charging current
- Built-in LDO and Buck DC-DC converter

- Less than 2uA sleep current
- VPWR range : 4.5V to 5.5V
- VBAT range : 2.2V to 4.5V
- IOVDD range : 2.2V to 3.6V

### Packages

- QFN52(6mm\*6mm)

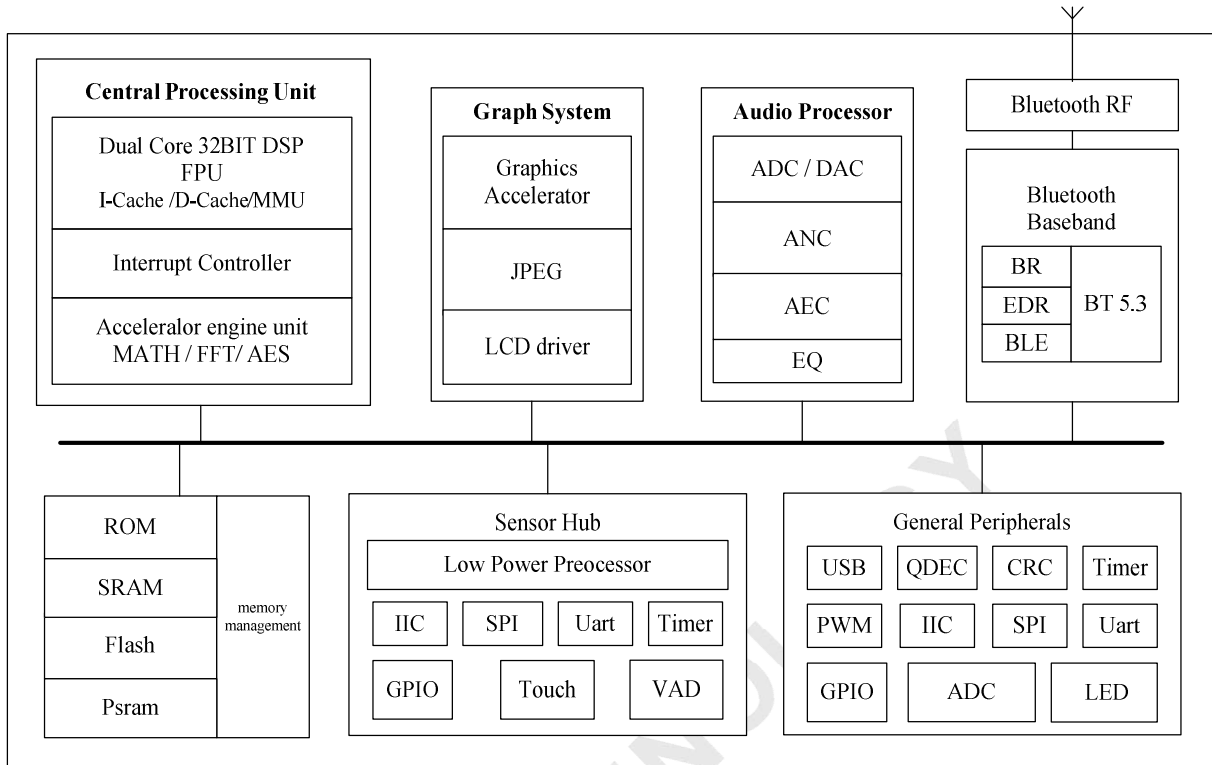
### Temperature

- Operating temperature: -40°C to +85°C
- Storage temperature: -65°C to +150°C

### Applications

- Bluetooth Smart Watch
- Bluetooth Smart Home
- Bluetooth Intelligent Voice

# 1、Block Diagram



**Figure 1-1 JL7012A Block Diagram**

## 2、Pin Definition

### 2.1 Pin Assignment

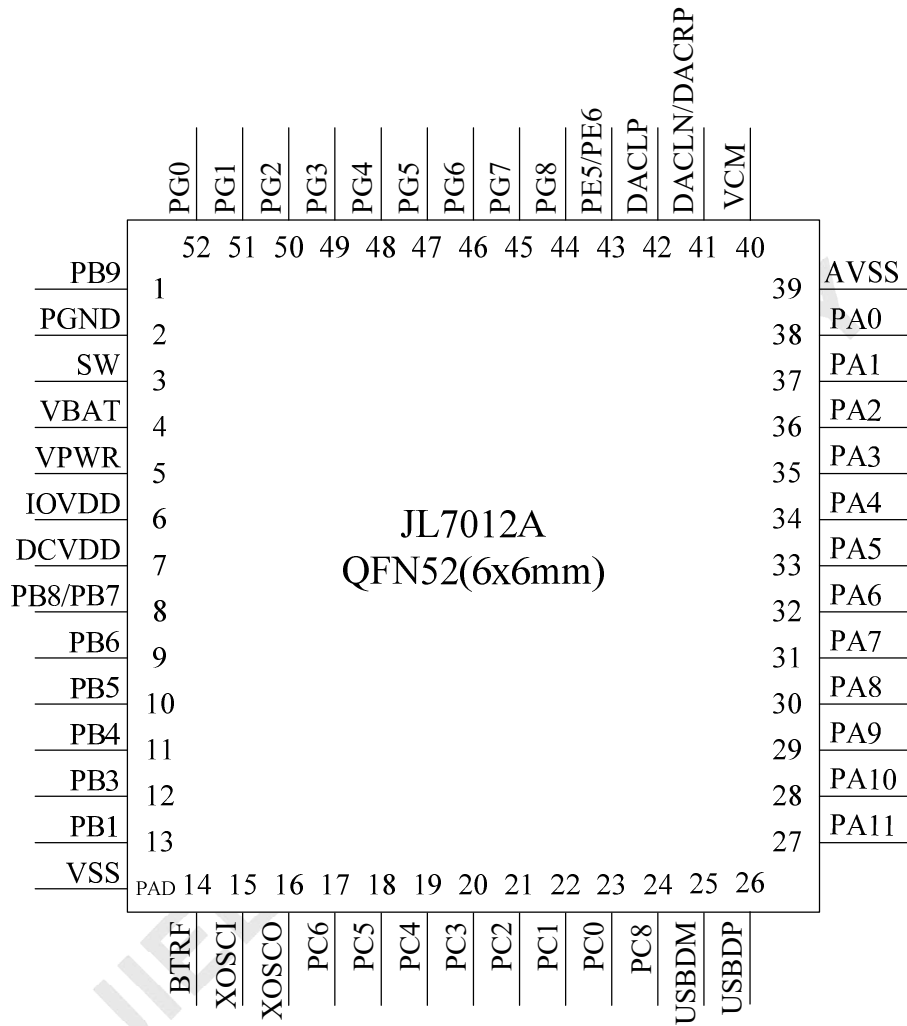


Figure 2-1 JL7012A 6 Package Diagram

## 2.2 Pin Description

**Table 2-1 JL7012A 6 Pin Description**

PIN NO.	Name	Type	Function	Other Function
1	PB9	I/O	GPIO (High Voltage Resistant)	ADC9:ADC Input Channel 9;
2	PGND	G		The ground of Buck DC-DC converter;
3	SW	PO		Switch signal of the Buck converter,connected to inductor;
4	VBAT	P		Battery interface;
5	VPWR (PB0)	PI (I/O)	GPIO (High Voltage Resistant)	Charging power input; UART0TXB:Uart0 Data Output(B); UART0RXB:Uart0 Data Input(B); CAP1:Timer1 Capture; PWM3:Timer3 PWM Output;
6	IOVDD	PO		Built-in linear voltage regulator output;
7	DCVDD	P		Internal power;
8	PB8	I/O	GPIO (High Voltage Resistant)	CAP4:Timer4 Capture;
	PB7	I/O	GPIO (High Voltage Resistant)	OSC32KI:32.768khz crystal oscillator input;
9	PB6	I/O	GPIO (High Voltage Resistant)	OSC32KO:32.768khz crystal oscillator output; PWM2:Timer2 PWM Output;
10	PB5	I/O	GPIO (High Voltage Resistant)	LP_Touch4:Low Power Touch Channel 4; IIC1_SDA_A:IIC1 SDA(A); ADC8:ADC Input Channel 8; UART3RXB:Uart3 Data Input(B);
11	PB4	I/O	GPIO (High Voltage Resistant)	LP_Touch3:Low Power Touch Channel 3; CLKOUT0:Clock Out0; IIC1_SCL_A:IIC1 SCL(A); UART3TXB:Uart3 Data Output(B); TMR2:Timer2 Clock Input;
12	PB3	I/O	GPIO (High Voltage Resistant)	UART3RXA:Uart3 Data Input(A);
13	PB1	I/O	GPIO (pull up) (High Voltage Resistant)	Hold down 0 to reset; LP_Touch1:Low Power Touch Channel 1; ADC6:ADC Input Channel 6;
14	BTRF	RFI		Bluetooth RF antenna interface;
15	XOSCI	I		System Crystal Oscillator Input;
16	XOSCO	O		System Crystal Oscillator Output;

17	PC6	I/O	GPIO (High Voltage Resistant)	ALNK_MCLKB:ALNK Master Clock(B);
18	PC5	I/O	GPIO	SFC1_D2:SFC1 Data2 Out(nor flash); SPI0_DAT2C(2):SPI0 Data2 Out(C); SD0_CLKA:SD0 Clock(A); SPI1DOB:SPI1 Data Out(B); IIC0_SDA_B:IIC0 SDA(B); ALNK_DAT3(B):Audio Link Data3(B); ADC5:ADC Input Channel 5; UART2RXA:Uart2 Data Input(A);
19	PC4	I/O	GPIO	SFC1_DI(D1):SFC1 Data In(nor flash); SPI0_DIC(1):SPI0 Data In(C); SD0_CMDA:SD0 CMD(A); SPI1CLKB:SPI1 Clock(B); IIC0_SCL_B:IIC0 SCL(B); ALNK_DAT2(B):Audio Link Data2(B); ADC4:ADC Input Channel 4; UART2TXA:Uart2 Data Output(A); PWM4:Timer4 PWM Output;
20	PC3	I/O	GPIO	SFC1_CS:SFC1 Chip Select(nor flash); LNA_EN:LNA Enable; SPI0_CSC:SPI0 Chip Select(C); SD0_DATA:SD0 Data(A); SPI1DIB:SPI1 Data In(B); ALNK_LRCK(B):Audio Link Word Select(B); TMR3:Timer3 Clock Input;
21	PC2	I/O	GPIO	SFC1_DO(D0):SFC1 Data Out(nor flash); PA_EN:PA Enable; SPI0_DOC(0):SPI0 Data Out(C); ALNK_SCLK(B):Audio Link Serial Clock(B); TMR1:Timer1 Clock Input;
22	PC1	I/O	GPIO	SFC1_CLK:SFC1 Clock(nor flash); SPI0_CLKC:SPI0 Clk(C); ALNK_DAT1(B):Audio Link Data1(B); TMR5:Timer5 Clock Input; PWMCH1L:Motor PWM Channel1(L);
23	PC0	I/O	GPIO	SFC1_D3:SFC1 Data3 Out(nor flash); SPI0_DAT3C(3):SPI0 Data3 Out(C); ALNK_DAT0(B):Audio Link Data0(B); PWMCH1H:Motor PWM Channel1(H);
24	PC8	I/O	GPIO	SPI2DIB:SPI2 Data In(B);

25	UDBDM	I/O	USB Negative Data (pull down)	SPI2DOB:SPI2 Data Out(B); IIC0_SDA_A:IIC0 SDA(A); ADC11:ADC Input Channel 11; UART1RXB:Uart1 Data Input(B);
26	USBDP	I/O	USB Positive Data (pull down)	SPI2CLKB:SPI2 Clk(B); IIC0_SCL_A:IIC0 SCL(A); ADC10:ADC Input Channel 10; UART1TXB:Uart1 Data Output(B);
27	PA11	I/O	GPIO	LCD_SPID3(A); FPIN0;
28	PA10	I/O	GPIO	LCD_SPID2(A); FPIN3;
29	PA9	I/O	GPIO	LCD_SPID1(DI)(A); PWMCH0H:Motor PWM Channel0(H);
30	PA8	I/O	GPIO	LCD_SPID0(DO)(A); PLNK_DAT1/ANCDE; ALNK_LRCK(A):Audio Link Word Select(A); ADC3:ADC Input Channel 3; UART2RXB:Uart2 Data Input(B);
31	PA7	I/O	GPIO	LCD_SPICLK(A); ALNK_SCLK(A):Audio Link Serial Clock(A); UART2TXB:Uart2 Data Output(B); TMR0:Timer0 Clock Input;
32	PA6	I/O	GPIO	PLNK_DAT0/ANCDR; SPI2DOA:SPI2 Data Out(A); ALNK_DAT3(A):Audio Link Data3(A); ADC2:ADC Input Channel 2; UART0RXA:Uart0 Data Input(A); CAP0:Timer0 Capture;
33	PA5	I/O	GPIO	PLNK_SCLK/ANCCK; SPI2CLKA:SPI2 Clk(A); ALNK_DAT2(A):Audio Link Data2(A); ADC1:ADC Input Channel 1; UART0TXA:Uart0 Data Output(A); PWM5:Timer5 PWM Output;
34	PA4	I/O	GPIO	MIC_BIAS1:MIC1 Bias Output(Built-in resistor); MIC1_N:Different MIC1 Negative; AMUX_B1:Analog Channel B1 input; SPI2DIA:SPI2 Data In(A); ALNK_DAT1(A):Audio Link Data1(A); CAP2:Timer2 Capture;



35	PA3	I/O	GPIO	MICIN1:MIC1 Input Channel 1; MIC1_P:Different MIC1 Positive; AMUX_B0:Analog Channel B0 input; SPI1DOA:SPI1 Data Out(A); ALNK_DAT0(A):Audio Link Data0(A); PWM1:Timer1 PWM Output;
36	PA2	I/O	GPIO	MIC_BIAS0:MIC0 Bias Output(Built-in resistor); MIC0_N:Different MIC0 Negative; AMUX_A1:Analog Channel A1 input; CLKOUT1:Clock Out1; SPI1CLKA:SPI1 Clk(A); ALNK_MCLKA:ALNK Master Clock(A); UART1RXA:Uart1 Data Input(A); CAP3:Timer3 Capture;
37	PA1	I/O	GPIO	MICIN0:MIC0 Input Channel 0; MIC0_P:Different MIC0 Positive; AMUX_A0:Analog Channel A0 input; SPI1DIA:SPI1 Data In(A); UART1TXA:Uart1 Data Output(A); PWM0:Timer0 PWM Output;
38	PA0	I/O	GPIO	MICLDO:Microphone linear voltage regulator output; ADC0:ADC Input Channel 0;
39	AVSS	G		Audio analog ground;
40	VCM	P		Audio analog reference bias;
41	DACLN	AO		Left channel audio output negative;
	DACRP	AO		Right channel audio output positive;
42	DACLP	AO		Left channel audio output positive;
43	PE6	I/O	GPIO	SDPG:SD card power gate;
	PE5	I/O	GPIO	
44	PG8	I/O	GPIO	MICIN2:MIC2 Input Channel 2; MIC2_P:Different MIC2 Positive; AMUX_C0:Analog Channel C0 input;
45	PG7	I/O	GPIO	LCD_SPID3(B); MIC_BIAS2:MIC2 Bias Output(Built-in resistor); MIC2_N:Different MIC2 Negative; AMUX_C1:Analog Channel C1 input; ADC15:ADC Input Channel 15;
46	PG6	I/O	GPIO	LCD_SPID2(B); MICIN3:MIC3 Input Channel 3; MIC3_P:Different MIC3 Positive; AMUX_D0:Analog Channel D0 input; FPIN2;

47	PG5	I/O	GPIO	LCD_SPID1/DI(B); MIC_BIAS3:MIC3 Bias Output(Built-in resistor); MIC3_N:Different MIC3 Negative; AMUX_D1:Analog Channel D1 input; ADC14:ADC Input Channel 14; TMR3CK;
48	PG4	I/O	GPIO (pull up)	LCD_SPID0/DO(B); SFC_CSB:SFC Chip Select(B); SPI0_CSB:SPI0 Chip Select(B); PWMCH3L:Motor PWM Channel3(L);
49	PG3	I/O	GPIO	LCD_SPICLK(B); TDM_MCLK; SFC_DIB(1):SFC Data In(B); SPI0_DIB(1):SPI0 Data In(B); PWMCH3H:Motor PWM Channel3(H);
50	PG2	I/O	GPIO	TDM_DAT; SFC_DAT2B(2):SFC Data2 Out(B); SPI0_DAT2B(2):SPI0 Data2 Out(B); SD0_CLKB:SD0 Clock(B); PWMCH2L:Motor PWM Channel2(L);
51	PG1	I/O	GPIO	TDM_SYN; SD0_CMDB:SD0 CMD(B); ADC13:ADC Input Channel 13; PWMCH2H:Motor PWM Channel2(H);
52	PG0	I/O	GPIO	TDM_CLK; LVD:Low Voltage Detect; SD0_DATB:SD0 Data(B); ADC12:ADC Input Channel 12; TMR2CK;
PAD	VSS	G		System ground;

Pin Type	Description	Pin Type	Description
P	Power	I/O	Input or Output
PO	Power Output	I	Input
PI	Power Input	O	Output
G	Ground	RFI	Radio frequency interface
AO	Analog Output		

### 3、Electrical Characteristics

#### 3.1 Absolute Maximum Ratings

**Table 3-1**

Symbol	Parameter	Min	Max	Unit
T <sub>opt</sub>	Operating temperature	-40	+85	°C
T <sub>stg</sub>	Storage temperature	-65	+150	°C
V <sub>BAT</sub>	Supply Voltage	-0.3	4.5	V
V <sub>PWR</sub>	Charger Voltage	-0.3	6	V
V <sub>IOVDD</sub>	Voltage applied at IOVDD	-0.3	3.6	V
V <sub>GPIO</sub>	Voltage applied to GPIO	-0.3	IOVDD+0.3	V
V <sub>HVIO</sub>	Voltage applied to High Voltage Resistant IO	-0.3	+5.5	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

#### 3.2 PMU Characteristics

**Table 3-2**

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V <sub>BAT</sub>	Voltage Input	2.2	3.7	4.5	V	
V <sub>PWR</sub>	Charger supply Voltage	4.5	5.0	5.5	V	
Operating mode						
IOVDD	Voltage output	2.0	3.0	3.4	V	V <sub>BAT</sub> = 4.2V, 10mA loading
	Loading current	–	–	120	mA	IOVDD=3V@V <sub>BAT</sub> = 4.2V
DCVDD	Voltage output	1.0	1.25	1.4	V	IOVDD=3.0V, 10mA loading
	Loading current	–	–	100	mA	DCVDD=1.25V@IOVDD=3.0v On LDO mode
–		–	180	mA	DCVDD=1.25V@IOVDD=3.0v On DC-DC mode	
V <sub>LVD</sub>	Voltage input	1.8	2.5	2.5	V	Low-Voltage Detection for IOVDD
Low Power mode						
IOVDD	Loading current	–	–	10	mA	IOVDD=3V@V <sub>BAT</sub> = 4.2V

### 3.3 Battery Charge

Table 3-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VPWR	Charge Input Voltage	4.5	5	5.5	V	-
V <sub>bat float</sub>	Charge Voltage	4.15	4.2	4.25	V	VPWR > 4.5V
		4.30	4.35	4.40	V	VPWR > 4.65V
I <sub>bat</sub>	Charge Current	15	-	200	mA	Charge current at fast charge mode VBAT=4.0V@VPWR=5.0V
I <sub>end</sub>	End Of Charge Current	2	-	30	mA	End of charge current
V <sub>Trickl</sub>	Trickle Charge Voltage	-	3.0	-	V	VPWR > 4.5V
I <sub>Trickl</sub>	Trickle Charge Current	1.5	-	30	mA	V <sub>BAT</sub> < V <sub>Trickl</sub>

### 3.4 IO Input/Output Electrical Logical Characteristics

Table 3-4

GPIO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V <sub>IL</sub>	Low-Level Input Voltage	-0.3	-	0.3* IOVDD	V	IOVDD = 3.0V
V <sub>IH</sub>	High-Level Input Voltage	0.7* IOVDD	-	IOVDD+0.3	V	IOVDD = 3.0V
High Voltage Resistant IO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V <sub>IL</sub>	Low-Level Input Voltage	-0.3	-	0.3* IOVDD	V	IOVDD = 3.0V
V <sub>IH</sub>	High-Level Input Voltage	0.7* IOVDD	-	+5V	V	IOVDD = 3.0V
GPIO & High Voltage Resistant IO output characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V <sub>OL</sub>	Low-Level Output Voltage	-	-	0.1* IOVDD	V	IOVDD = 3.0V
V <sub>OH</sub>	High-Level Output Voltage	0.9* IOVDD	-	-	V	IOVDD = 3.0V

### 3.5 Internal Resistor Characteristics

Table 3-5

Port	Drive Current		Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA0~PA11	HD,HD0==0,0	2.4mA	10K	10K	1、PB1, PG4 default pull up 2、USBDM & USBDP default pull down 3、internal pull-up/pull-down resistance   accuracy ±20%
PC0~PC5,PC8	HD,HD0==0,1	8mA			
PG0~PG8	HD,HD0==1,0	26mA			
PE5,PE6	HD,HD0==1,1	46mA			
PB1~PB9 PC6 PP0(VPWR)	8mA (High Voltage Resistant)		10K	10K	
USBDP	4mA		1.5K	15K	
USBDM	4mA		180K	15K	

### 3.6 Audio DAC Characteristics

Table 3-6

Parameter	Min	Typ	Max	Unit	Audio Format	Test Conditions
Frequency Response	20	—	20K	Hz	—	Differential Mode 1KHz/0dB 10k ohm loading With A-Weighted Filter
Output Swing	—	1.7	—	Vrms	—	
THD+N	—	-77	—	dB	PCM	
	—	-70	—	dB	SBC	
S/N	—	104	—	dB	PCM	
	—	104	—	dB	SBC	
Dynamic Range	—	103	—	dB	PCM	
	—	103	—	dB	SBC	
Noise Floor	—	9.8	—	uVrms	—	A-Weighted Filter

### 3.7 Audio ADC Characteristics

Table 3-7

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range		94		dB	Fsample=44.1kHz,Gain=0dB Fin=1KHz 590mVrms
S/N	—	95	—	dB	Fsample=44.1kHz,Gain=0dB Fin=1KHz 590mVrms
THD+N	—	-75	—	dB	
S/N	—	76	—	dB	Fsample=44.1kHz,Gain=18dB Fin=1KHz 75mVrms
THD+N	—	-73	—	dB	

### 3.8 BT Characteristics

#### 3.8.1 Transmitter

##### Basic Data Rate

**Table 3-8**

Parameter		Min	Typ	Max	Unit	Test Conditions
RF Transmit Power			7.0		dBm	25°C, Power Supply VBAT=3.7V 2441MHz
RF Power Control Range			18.2		dB	
20dB Bandwidth			950		KHz	
Adjacent Channel	+2MHz		-28		dBm	
	-2MHz		-34		dBm	
Transmit Power	+3MHz		-30		dBm	
	-3MHz		-43		dBm	

##### Enhanced Data Rate

**Table 3-9**

Parameter		Min	Typ	Max	Unit	Test Conditions
Relative Power			-2.5		dB	25°C, Power Supply VBAT=3.7V 2441MHz
$\pi/4$ DQPSK Modulation Accuracy	DEVM RMS		6		%	
	DEVM 99%		11		%	
	DEVM Peak		16		%	
Adjacent Channel	+2MHz		-28		dBm	
	-2MHz		-34		dBm	
Transmit Power	+3MHz		-30		dBm	
	-3MHz		-43		dBm	

#### 3.8.2 Receiver

##### Basic Data Rate

**Table 3-10**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-92		dBm	25°C, Power Supply VBAT=3.7V 2441MHz DH5
Co-channel Interference Rejection			10		dB	
Adjacent Channel	+1MHz		-4		dB	
	-1MHz		-3		dB	
	+2MHz		-39		dB	
Interference Rejection	-2MHz		-29		dB	
	+3MHz		-45		dB	
	-3MHz		-23		dB	

**Enhanced Data Rate**

**Table 3-11**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity		-95	-94		dBm	25°C, Power Supply VBAT=3.7V 2441MHz 2DH5
Co-channel Interference Rejection			10		dB	
Adjacent Channel Interference Rejection	+1MHz		-4		dB	
	-1MHz		-3		dB	
	+2MHz		-39		dB	
	-2MHz		-29		dB	
	+3MHz		-45		dB	
	-3MHz		-23		dB	

JIELI TECHNOLOGY

## 4、Package Information

### 4.1 QFN52\_6×6mm

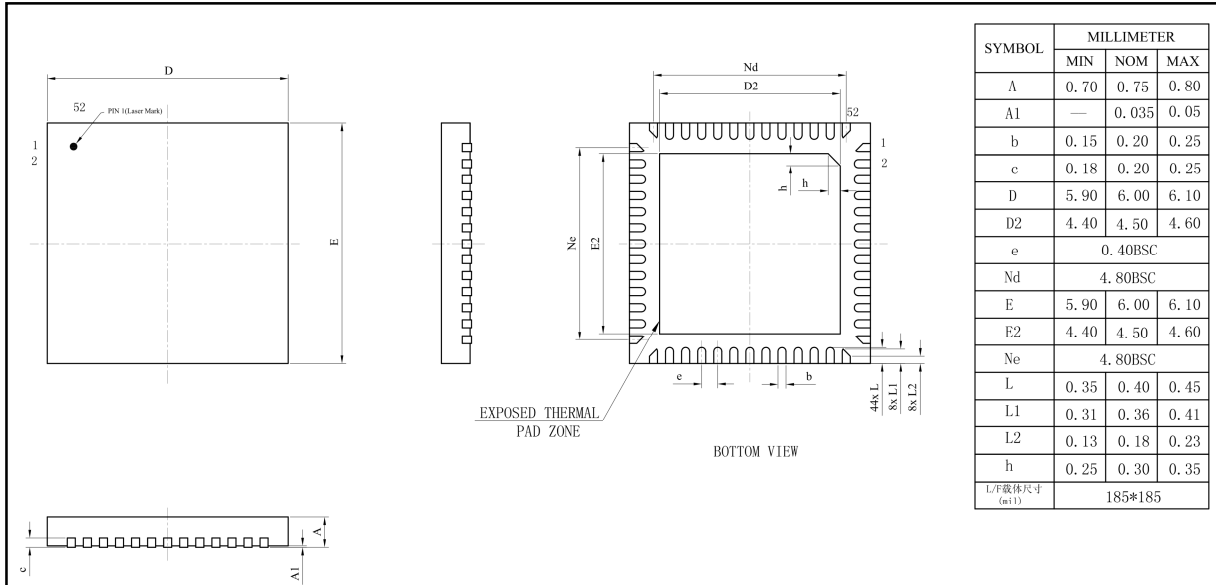


Figure 4-1 JL7012A 6 Package



## 5、 Revision History

Date	Revision	Description
2022.02.09	V1.0	Initial Release

JIELI TECHNOLOGY