AC7023D2/D4 Datasheet

Zhuhai Jieli Technology Co.,LTD

Version：1.2

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AC7023D2/D4 Features

CPU

- 32-bit DSP
- with IEEE754 Single precision FPU
- Mathematic alaccelerate engine
- Up to 160MHz programmable processor
- 64Vectored interrupts
- 8 Levels interrupt priority

Clocks

- 24 MHz crystal oscillator

DSP Audio Processing

- SBC, AAC Audio decodes supported for BT audio
- mSBC voice codec supported for BT phone
- Packet Loss Concealment (PLC) for voice processing
- Single MIC Environmental Noise Cancellation (ENC)
- Single-band DRC limiter
- Multi-band EQ configuration for voice Effects

Audio Codec

- Two channels 24-bit DAC,SNR ≥ 102dB
- One channels 16-bit ADC,SNR ≥ 90dB
- Audio DAC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/ 32kHz/44.1kHz/48kHz are supported
- Audio ADC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/32 kHz/44.1kHz/48kHz are supported
- One channels analog audio inputs
- Audio DAC supports differential cap-less mode or single-ended mode
- Direct drive 16ohm/32ohm Speaker loading

Bluetooth

- Compliant with Bluetooth V5.3+BR+EDR+BLE specification
- Meet class2 and class3 transmitting power requirement
- Maximum +8dbm transmitting power
- EDR receiver with minimum -94dBm sensitivity
- Support a2dp\avctp\avdtp\avrcp\hfp\spp\smp\ att\gap\gatt\rfcomm\sdp\l2cap profile
- a2dp 1.3.2\avctp 1.4\avdtp 1.3\ avrcp 1.6.2\hfp 1.8 \spp 1.2\rfcomm 1.1\pnp 1.3\hid 1.1.1\sdp core5.3\l2cap core 5.3

Peripherals

- full speed USB OTG controller
- multi-function 32-bit timers, support capture and PWM mode
- Uart interface support DMA
- Low power CapSense
- 10-bit ADC for analog sampling
- Individually programmable and multiplexed GPIO pins
- external interrupt/wake-up source(low power available,can be multiplexed to any I/O)

PMU

- Built-in lithium battery charging manager,up to 200mA charging current
- Built-in LDO and Buck DC-DC converter
- Soft-off mode current
  Build-in LP_Touch off：
  ≤3uA(AC702N_FLASH_SDK_vx.x.x)
  ≤7uA(AC702N_release_vx.x.x)
  Build-in LP_Touch on： ≤13uA
- VPWR range : 4.5V to 5.5V
- VBAT range : 2.7V to 4.5V
- IOVDD range : 2.0V to 3.4V

Packages

- QFN20(3mm*3mm)

Temperature

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

Applications

- Bluetooth TWS Earphones

1 Block Diagram

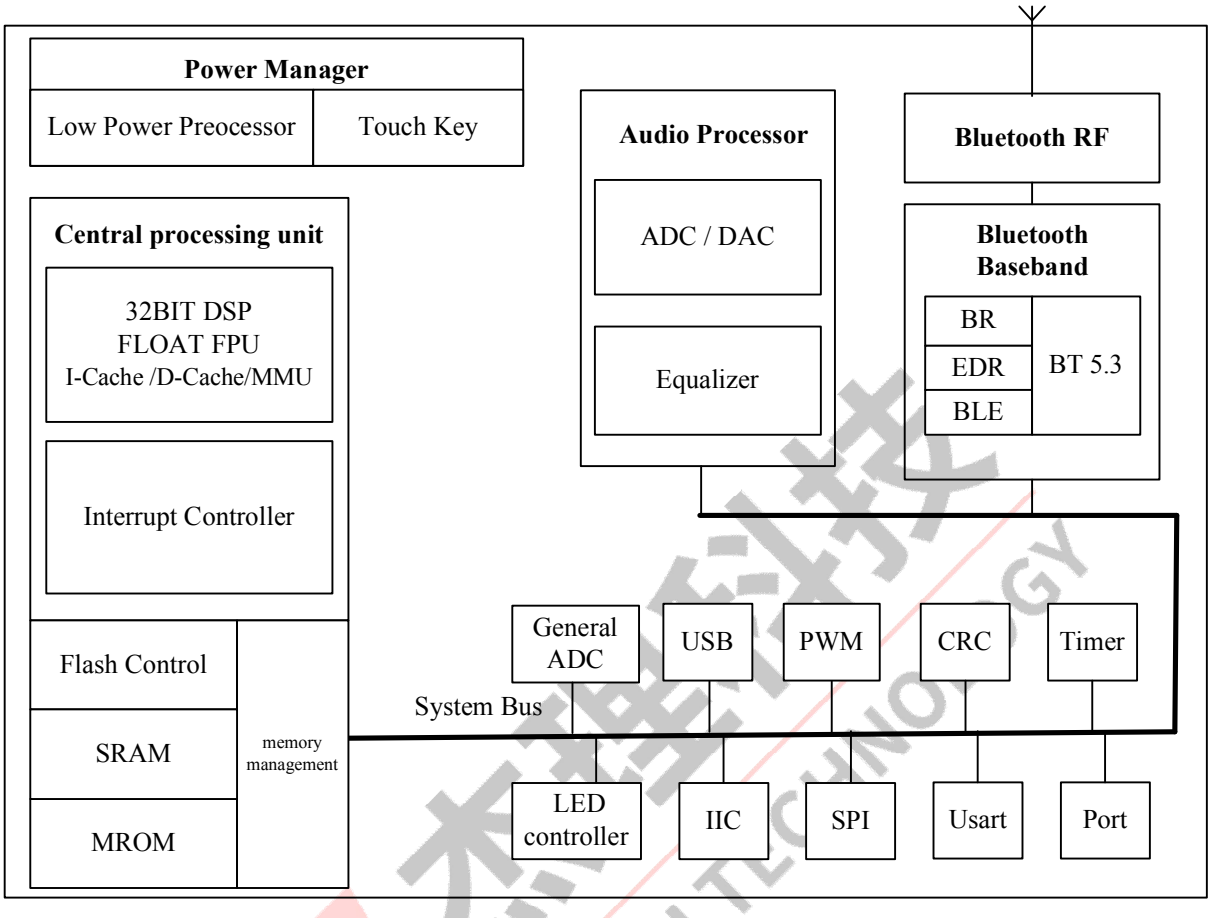


Figure 1-1 AC7023D Block Diagram

2 Pin Definition

2.1 Pin Assignment

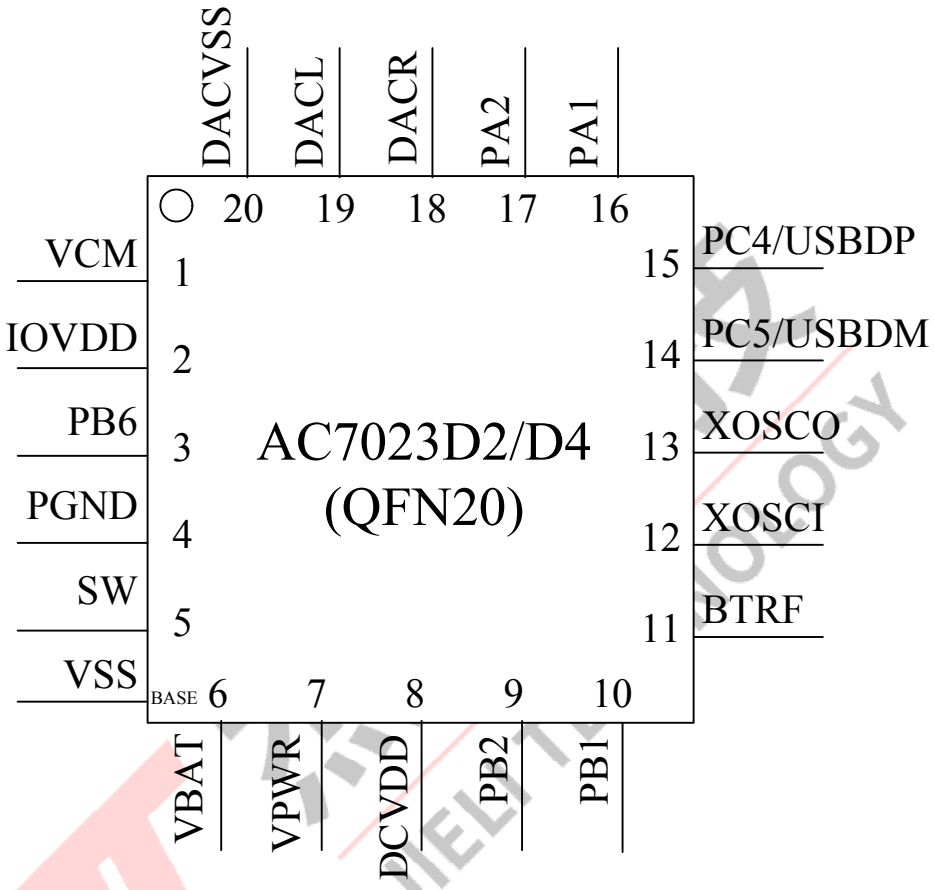


Figure 2-1 AC7023D Package Diagram

2.2 Pin Description

Table 2-1 AC7023D Pin Description

Pin No.	Pin name	Type	Function	Other function
1	VCM	P		Audio analog reference bias;
2	IOVDD	PO		IO Power;
3	PB6	I/O	GPIO	ADC9 :ADC Input Channel 9; UART1RXA :Uart1 Data In(A); PWM2 :Timer2 PWM Output;
4	PGND	G		The ground of Buck DC-DC converter;
5	SW	PO		Switch signal of the Buck converter, connected to inductor;
6	VBAT	PI	GPIO	Battery interface;
7	VPWR (PP0)	PI (I/O)	GPIO (High Voltage Input)	Charge Power Input; UART0TXC：Uart0 Data Output(C); UART0RXC：Uart0 Data Input(C); PWM3：Timer3 PWM Output； CAP1：Timer1 Capture;
8	DCVDD	P		DCDC power 1.25V;
9	PB2	I/O	GPIO	LP_Touch1 :Low Power Touch Channel 1; UART2RXC: Uart2 Data In(C); CAP5: Timer5 Capture;
10	PB1	I/O	GPIO	LP_Touch0 :Low Power Touch Channel 0; UART2TXC :Uart2 Data Out(C); TMR0 :Timer0 Clock In;
11	BTRF	RFI		Bluetooth RF antenna interface;
12	XOSCI	I		System Crystal Oscillator Input;
13	XOSCO	O		System Crystal Oscillator Output;
14	PC5	I/O	GPIO	IIC_SDA_B : IIC Data(B); ADC5 :ADC Input Channel 5; UART2RXD :Uart2 Data In(D);
	USBDM	I/O	USB Negative Data (pull down)	IIC_SDA_A：IIC SDA(A); ADC11：ADC Input Channel 11; UART1RXD：UART1 Data In(D);

15	PC4	I/O	GPIO	IIC_SCL_B：IIC Serial Clock(B); ADC4 : ADC Input Channel 4; UART2TXD: Uart2 Data Out(D); PWM4 :Timer4 PWM Output;
	USBDP	I/O	USB Positive Data (pull down)	IIC_SCL_A：IIC Clock(A); ADC10 :ADC Input Channel 10; UART1TXD :Uart1 Data Out(D);
16	PA1	I/O	GPIO	MICIN0 :MIC0 Input Channel 0; UART1TXC :Uart1 Data Out(C); PWM0 :Timer0 PWM Output;
17	PA2	I/O	GPIO	CLKOUT1：Clock Out1; MICBIAS0 : MIC0 Bias Output(Built-in resistor); UART1RXC :Uart1 Data In(C); CAP3: Timer3 Capture;
18	DACR	AO	Analog Output	Right channel audio output positive;
19	DACL	AO	Analog Output	Left channel audio output positive;
20	DACVSS	G		Analog Ground;
BASE	VSS	G		Ground;

Pin Type	**Description**	**Pin Type**	**Description**
P	Power	I/O	Input or Output
PO	Power Output	I	Input
PI	Power Input	O	Output
G	Ground	RFI	Radio frequency interface
AO	Analog Output		

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1

Symbol	Parameter	Min	Max	Unit
Topt	Operating temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	-0.3	4.5	V
VPWR	Charger Voltage	-0.3	6	V
V_{IOVDD}	Voltage applied at IOVDD	-0.3	3.6	V
V_{GPIO}	Voltage applied to GPIO	-0.3	IOVDD+0.3	V
V_{HVIO}	Voltage applied to High Voltage Resistant IO	-0.3	+5.5	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

3.2 PMU Characteristics

Table 3-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.2	3.7	4.5	V	
VPWR	Charger supply Voltage	4.5	5.0	5.5	V	
Operating mode						
IOVDD	Voltage output	_	3.0	_	V	VBAT = 4.2V, 10mA loading
	Loading current	_	_	200	mA	IOVDD=3.2V@VBAT = 3.5V
DCVDD	Voltage output	_	1.25	_	V	IOVDD=3.0V, 10mA loading
	Loading current	_	_	60	mA	DCVDD=1.25V@IOVDD=3.0v on LDO mode
		_	_	150	mA	DCVDD=1.25V@VBAT=3.0v on DCDC mode
Low Power mode						
IOVDD	Loading current	_	_	10	mA	IOVDD=3V@VBAT = 4.2V

3.3 Battery Charge

Table 3-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VPWR	Charge Input Voltage	4.5	5	5.5	V	_
$V_{bat\ float}$	Charge Voltage	4.15	4.2	4.25	V	VPWR＞4.5V
I_{bat}	Charge Current	20	_	200	mA	Charge current at fast charge mode VBAT=4.0V@VPWR=5.0V
I_{end}	End Of Charge Current	2	_	30	mA	End of charge current
V_{Trikl}	Trickle Charge Voltage	_	3.0	_	V	VPWR＞4.5V

3.4 IO Input/Output Electrical Logical Characteristics

Table 3-4

GPIO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	_	0.3* IOVDD	V	IOVDD = 3.0V
V_{IH}	High-Level Input Voltage	0.7* IOVDD	_	IOVDD+0.3	V	IOVDD = 3.0V
High Voltage Resistant IO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	_	0.3* IOVDD	V	IOVDD = 3.0V
V_{IH}	High-Level Input Voltage	0.7* IOVDD	_	+5V	V	IOVDD = 3.0V
GPIO & High Voltage Resistant IO output characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{OL}	Low-Level Output Voltage	_	_	0.1* IOVDD	V	IOVDD = 3.0V
V_{OH}	High-Level Output Voltage	0.9* IOVDD	_	_	V	IOVDD = 3.0V

3.5 Internal Resistor Characteristics

Table 3-5

Port	Drive(mA)		Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA1,PA2 PB1,PB2,PB6 PC4,PC5	HD,HD0==0,0	2.4	10K	10K	1、PB1 default pull up 2、USBDM & USBDP default pull Down 3、internal pull-up / pull-down resistance | accuracy ±20%
	HD,HD0==0,1	8			
	HD,HD0==1,0	26			
	HD,HD0==1,1	46			
PP0(VPWR)	8 (High Voltage Resistant)		10K	10K	
USBDP	4		1.5K	15K	
USBDM			180K	15K	

3.6 Audio DAC Characteristics

Audio Format: SBC

Table 3-6

Parameter	Min	Typ	Max	Unit	Test Conditions
Frequency Response	20	_	20k	Hz	1KHz/0dB 32 ohm loading With A-Weighted Filter Differential Mode
Output Swing		0.35	1.18	Vrms	
THD+N	_	-68	_	dB	
S/N	_	95	101	dB	
Dynamic Range	_	96	101	dB	1KHz/-60dB 32 ohm loading With A-Weighted Filter Differential Mode
Noise Floor	_	6	_	uVrms	A-Weighted Filter
DAC Output Power	_	4	43	mW	32ohm loading Differential Mode

3.7 Audio ADC Characteristics

Audio Filter: A-Weighted

Table 3-7

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range	_	90	_	dB	Fsample=44.1kHz,Gain=6dB Fin=1KHz 320mVrms
SNR	_	90	_	dB	Fsample=44.1kHz,Gain=6dB Fin=1KHz 320mVrms
THD+N	_	-70	_	dB	
SNR	_	84	_	dB	Fsample=44.1kHz,Gain=16dB Fin=1KHz 90mVrms
THD+N	_	-65	_	dB	

3.8 BT Characteristics

3.8.1 Transmitter

Basic Data Rate Table 3-8

Parameter		Min	Typ	Max	Unit	Test Conditions
RF Transmit Power，DH5			6	8	dBm	25℃， Power Supply VBAT=3.7V 2441MHz 4 Layer Board
RF Power Control Range，DH1			20		dB	
20dB Bandwidth，DH5			920		KHz	
Adjacent Channel Transmit Power，DH1（BQB Test Mode RF_Tx Power=3.6dBm）	+2MHz		-54		dBm	
	-2MHz		-49		dBm	
	+3MHz		-58		dBm	
	-3MHz		-43		dBm	

Enhanced Data Rate Table 3-9

Parameter		Min	Typ	Max	Unit	Test Conditions
Relative Power			-1.5		dB	25℃ Power Supply VBAT=3.7V 2441MHz 2DH5 4 Layer Board
π/4 DQPSK Modulation Accuracy	DEVM RMS		6		%	
	DEVM 99%		10		%	
	DEVM Peak		14		%	
In-band spurious Emissions（BQB Test Mode RF_Tx Power=3.6dBm）	+2MHz		-42		dBm	
	-2MHz		-35		dBm	
	+3MHz		-47		dBm	
	-3MHz		-36		dBm	

3.8.2 Receiver

Basic Data Rate Table 3-10

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-91		dBm	25℃， Power Supply VBAT=3.7V 2441MHz DH1 4 Layer Board
Co-channel Interference Rejection			4		dB	
Adjacent Channel Interference Rejection	+1MHz		-27		dB	
	-1MHz		-26		dB	
	+2MHz		-41		dB	
	-2MHz		-36		dB	
	+3MHz		-42		dB	
	-3MHz		-34		dB	

Enhanced Data Rate **Table 3-11**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity		-94	-92		dBm	25℃, Power Supply VBAT=3.7V 2441MHz 2DH5 4 Layer Board
Co-channel Interference Rejection			10		dB	
Adjacent Channel Interference Rejection	+1MHz		-27		dB	
	-1MHz		-26		dB	
	+2MHz		-31		dB	
	-2MHz		-27		dB	
	+3MHz		-37		dB	
	-3MHz		-27		dB	

3.9 ESD Protection

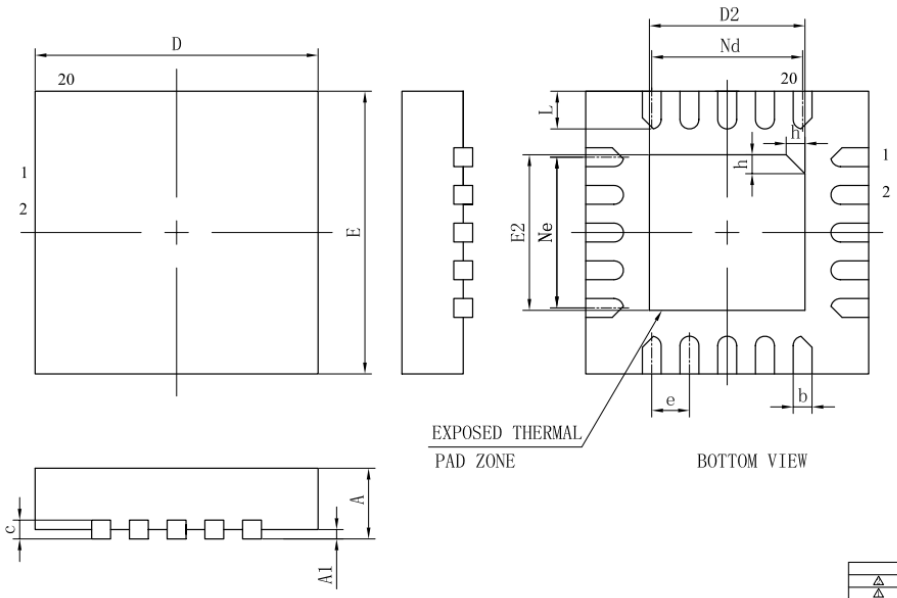
Table 3-12

Parameter	Typ.	Test pin	Reference standard
Human Body Mode	±4KV	All pins	JEDEC EIA/JESD22-A114
Machine Mode	±200V	All pins	JEDEC EIA/JESD22-A115
Charge Device Model	±1KV	All pins	JEDEC EIA/JESD22-C101F
Latch up	±200mA	All GPIO pins	JEDEC STANDARD NO.78E
	1.5xVopmax	All power pins	

Note : 1.5xVopmax = 1.5 times maximum operating voltage.

4 Package Information

4.1 QFN20_3.0x3.0



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30
L/F载体尺寸 (架1)	75*75		

△	更改公司名称	李万霞	2011.7.5
△	更改公司名称	李新锋	2011.3.3
更改标记	更改内容	签 名	日 期

Figure 4-1 AC7023D Package

5 Solder-Reflow Condition

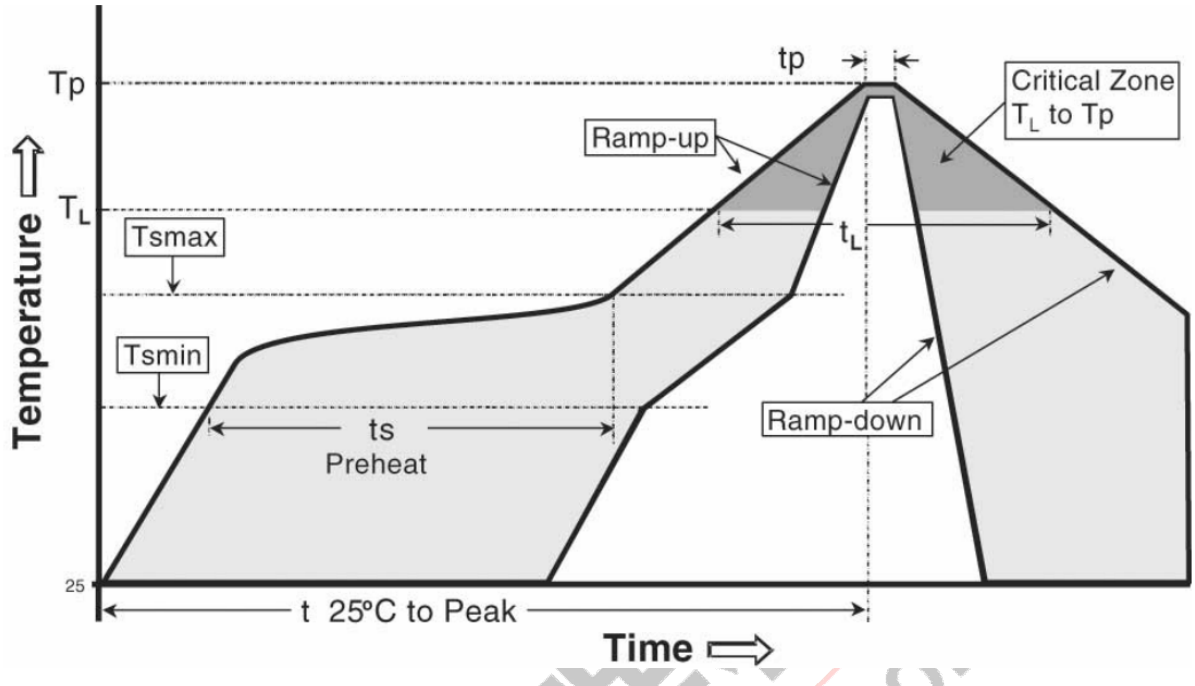


Figure 5-1 Classification Reflow Profile

Classification Profiles **Table 5-1**

Profile Feature		Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/ Soak	Temperature Min (T_{smin})	100℃	150℃
	Temperature Max (T_{smax})	150℃	200℃
	Time (ts) from (T_{smin} to T_{smax})	60-120 seconds	60-180 seconds
Average ramp-up rate (T_{smax} to T_p)		3℃/second max	3℃/second max
Liquidous temperature (T_L) Time (t_L) maintained above T_L		183℃ 60-150 seconds	217℃ 60-150 seconds
Peak package body temperature (T_p)		See Table 5-2	See Table 5-3
Time within 5℃ of actual Peak Temperature (tp)[2]		10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)		6℃/second max	6℃/second max
Time 25℃ to peak temperature		6 minutes max	8 minutes max

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Note 2: Time within 5℃ of actual peak temperature (tp) specified for the reflow profiles is a "supplier" minimum and "user" maximum.

SnPb - Classification Temperature **Table 5-2**

Package Thickness	Volume mm^3 < 350	Volume mm^3 ⩾ 350
<2.5 mm	240 +0/-5℃	225 +0/-5℃
⩾2.5 mm	225 +0/-5℃	225 +0/-5℃

Pb-free - Classification Temperature **Table 5-3**

Package Thickness	Volume mm^3 < 350	Volume mm^3 350 - 2000	Volume mm^3 > 2000
< 1.6mm	260℃	260℃	260℃
1.6 mm - 2.5mm	260℃	250℃	245℃
> 2.5mm	250℃	245℃	245℃

*Tolerance:The device manufancturer/supplier shall assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C.For example 260°C+0°C)at the rated MSL level.

6 Revision History

Date	Revision	Description
2022.09.06	V1.0	Initial Release
2022.12.20	V1.1	Update resource description
2023.01.09	V1.2	Update Characteristics table format