

General Description

The LTA604x family true single-supply voltage feedback operational amplifiers feature high speed performance with 100 MHz of small signal bandwidth and 107 V/ μ s slew rate. The products are specified for +3 V, +5 V, and \pm 5 V supplies, input common mode voltage range extends to 0.2 V below V_{S-} and 1 V from V_{S+} , and output voltage range extends to within 500 mV of either supply rail, allowing wide dynamic range especially desirable in low voltage applications. The LTA604xC also offer excellent signal quality of low distortion (-53 dBc with a 2 V_{PP} , 5 MHz output signal) and fast settling time (66 ns to 0.1%), which make them ideal as buffers to single-supply ADCs.

Operating on supplies from +2.5 V to +12.6 V and dual supplies up to \pm 6.3 V, the LTA604x are ideal for a wide range of applications, from battery-operated systems with large bandwidth requirements to high speed systems where component density requires lower power dissipation. The single version LTA6041 device is available in micro-size SOT23-5L and SOIC-8L packages. The dual LTA6042 device is offered in MSOP-8L and SOIC-8L packages. The quad LTA6044 device is offered in SOIC-14L and TSSOP-14L packages.

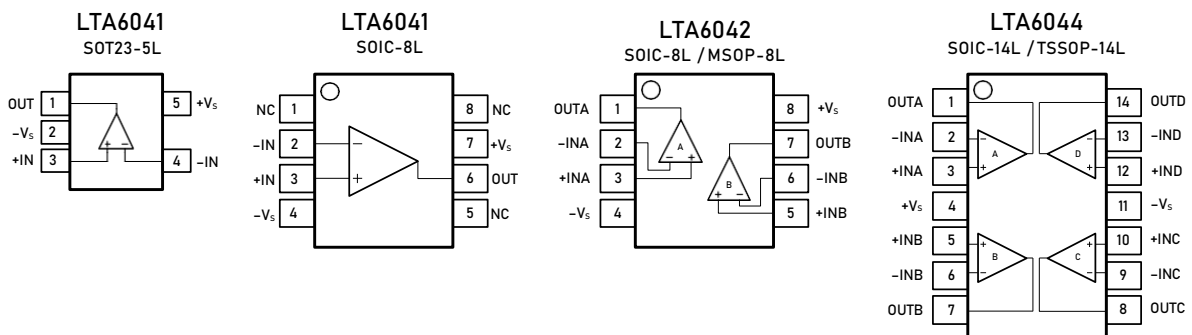
Features and Benefits

- High Speed and Fast Settling on \pm 5 V
 - 105 MHz, -3 dB bandwidth ($G = +1$)
 - 107 V/ μ s slew rate
 - 66 ns settling time to 0.1%
- Fully specified at +3 V, +5 V, and \pm 5 V Supplies
- Low Input Bias Current 4 pA
- Input Common Mode Voltage 0.2 V Beyond V_{S-} , 1 V from V_{S+}
- Output Voltage Swing 500 mV from Rails
- Output Short Circuit Current 150 mA
- Linear Output Current \pm 70 mA
- Operating Temperature Range -40°C to +125°C (except SOT23-5L)

Applications

- High speed, battery-operated systems
- High component density systems
- Portable test instruments
- A/D buffers
- Active filters
- High speed, set-and-demand amplifiers

Pin Configuration (Top View)



Pin Description

Symbol	Description
-IN	Inverting input of the amplifier. The voltage range is from $V_{S-} - 0.2V$ to $V_{S+} - 1V$.
+IN	Non-inverting input of the amplifier. This pin has the same voltage range as -IN.
+V _S	Positive power supply. The voltage is from 2.5V to 12.6V. Split supplies are possible as long as the voltage between V_{S+} and V_{S-} is from 2.5V to 12.6V.
-V _S	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V_{S+} and V_{S-} is from 2.5V to 12.6V.
OUT	Amplifier output.
NC	No connection

Ordering Information ⁽¹⁾

Type Number	Package Name	Package Quantity	Eco Class ⁽²⁾	Marking Code ⁽³⁾
LTA6041XT5/R6	SOT23-5L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	W41
LTA6041XS8/R8	SOIC-8L	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	W6041
LTA6042XS8/R8	SOIC-8L	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	W6042
LTA6042XV8/R6	MSOP-8L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	W6042
LTA6044XS14/R5	SOIC-14L	Tape and Reel, 2 500	Green (RoHS & no Sb/Br)	W6044
LTA6044XT14/R6	TSSOP-14L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	W6044

- (1) Please contact to your Linearin representative for the latest availability information and product content details.
- (2) Eco Class - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & Halogen Free).
- (3) There may be multiple device markings, a varied marking character of "x", or additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

Limiting Value – In accordance with the Absolute Maximum Rating System (IEC 60134).

Parameter	Absolute Maximum Rating
Supply Voltage, V_{S+} to V_{S-}	13.5 V
Signal Input Terminals: Voltage, Current	$-V_{S-} - 0.5 V$ to $+V_{S+} + 0.5 V$, ± 10 mA
Output Short-Circuit	Continuous
Storage Temperature Range, T_{stg}	-65 to $+150$ °C
Junction Temperature, T_j	150 °C
Lead Temperature Range (Soldering 10 sec)	260 °C

ESD Rating

Parameter	Item	Value	Unit
Electrostatic Discharge Voltage	Human body model (HBM), per MIL-STD-883J / Method 3015.9 ⁽¹⁾	$\pm 4\ 000$	V
	Charged device model (CDM), per ESDA/JEDEC JS-002-2014 ⁽²⁾	$\pm 2\ 000$	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible if necessary precautions are taken.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible if necessary precautions are taken.

Electrical Characteristics

$V_S = 3\text{ V}$, $T_A = +25\text{ }^\circ\text{C}$, $V_{CM} = V_O = V_S/2$, and $R_L = 2\text{ k}\Omega$ to $V_S/2$, unless otherwise noted.
Boldface limits apply over the specified temperature range, $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DYNAMIC PERFORMANCE						
BW _{-3dB}	-3 dB Small Signal Bandwidth	$G = +1, V_O = 0.2V_{PP}$		95		MHz
		$G = +2, -1, V_O = 0.2V_{PP}$		38		
BW _{0.1dB}	Bandwidth for 0.1 dB Flatness	$G = +2, V_O = 0.2V_{PP}, R_L = 150\Omega$ to $V_S/2$, $R_F = 402\Omega$		8.5		MHz
SR	Slew rate	$G = -1, V_O = 2\text{ V}$ step		98		V/ μ s
BW _{FP}	Full Power Response	$G = +1, V_O = 1V_{PP}$		11		MHz
t _s	Settling time to 0.1%	$G = -1, V_O = 2\text{ V}$ step		66		ns
NOISE/DISTORTION PERFORMANCE						
THD	Total harmonic distortion	$f_C = 5\text{ MHz}, V_O = 2V_{PP}, G = +2$		-36		dBc
e _n	Input voltage noise density	$f = 100\text{ kHz}$		27		nV/ $\sqrt{\text{Hz}}$
i _n	Input current noise density	$f = 10\text{ kHz}$		3		pA/ $\sqrt{\text{Hz}}$
DG	Differential Gain Error (NTSC)	$G = +2, R_L = 150\Omega$ to $V_S/2$		0.17		%
		$R_L = 1\text{ k}\Omega$ to $V_S/2$		0.03		
DP	Differential Phase Error (NTSC)	$G = +2, R_L = 150\Omega$ to $V_S/2$		0.05		deg.
		$R_L = 1\text{ k}\Omega$ to $V_S/2$		0.03		
DC PERFORMANCE						
V _{OS}	Input offset voltage			± 3	± 15	mV
V _{OS TC}	Offset voltage drift	$T_A = -40$ to $+125\text{ }^\circ\text{C}$		± 5		$\mu\text{V}/^\circ\text{C}$
I _B	Input bias current			4		pA
I _{OS}	Input offset current			2		pA
A _{VOL}	Open-loop voltage gain	$R_L = 2\text{ k}\Omega$ to $V_S/2, V_O = 0.5\text{ V}$ to 2.5 V		95		dB
		$R_L = 150\Omega$ to $V_S/2, V_O = 0.5\text{ V}$ to 2.5 V		82		
INPUT CHARACTERISTICS						
R _{IN}	Input Resistance	Common mode		1		G Ω
C _{IN}	Input capacitance	Common mode		2		pF
V _{CM}	Common-mode voltage range	CMRR $\geq 50\text{ dB}$	-0.2		2	V
CMRR	Common-mode rejection ratio	$V_{CM} = 0\text{ V}$ to 1.5 V		85		dB
OUTPUT						
V _{OH}	High output voltage swing	$R_L = 2\text{ k}\Omega$ to $V_S/2$		2.97		V
		$R_L = 150\Omega$ to $V_S/2$		2.85		
V _{OL}	Low output voltage swing	$R_L = 2\text{ k}\Omega$ to $V_S/2$		30		mV
		$R_L = 150\Omega$ to $V_S/2$		230		
I _{OUT}	Output Current	$V_{OUT} = 0.5\text{ V}$ from either supply		± 60		mA
I _{SC}	Short-circuit current			± 110		mA
C _{LOAD}	Capacitive load drive	$G = +2$		40		pF

Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLY						
V_S	Operating supply range		2.5		12.6	V
I_Q	Quiescent current /Amplifier			4.1		mA
PSRR	Power supply rejection ratio	$V_S = 3.0$ to 3.5 V		70		dB
$V_S = 5$ V, $T_A = +25$ °C, $V_{CM} = V_O = V_S/2$, and $R_L = 2$ k Ω to $V_S/2$, unless otherwise noted. Boldface limits apply over the specified temperature range, $T_A = -40$ °C to $+125$ °C.						
DYNAMIC PERFORMANCE						
BW_{-3dB}	-3 dB Small Signal Bandwidth	$G = +1, V_O = 0.2V_{PP}$		100		MHz
		$G = +2, -1, V_O = 0.2V_{PP}$		38		
$BW_{0.1dB}$	Bandwidth for 0.1 dB Flatness	$G = +2, V_O = 0.2V_{PP}, R_L = 150\Omega$ to $V_S/2$, $R_F = 402\Omega$		8		MHz
SR	Slew rate	$G = -1, V_O = 2V$ step		102		V/ μ s
BW_{FP}	Full Power Response	$G = +1, V_O = 2V_{PP}$		14		MHz
t_s	Settling time to 0.1%	$G = -1, V_O = 2V$ step		66		ns
NOISE/DISTORTION PERFORMANCE						
THD	Total harmonic distortion	$f_C = 5$ MHz, $V_O = 2V_{PP}, G = +2$		-49		dBc
e_n	Input voltage noise density	$f = 100$ kHz		27		nV/ \sqrt Hz
I_n	Input current noise density	$f = 10$ kHz		3		pA/ \sqrt Hz
DG	Differential Gain Error (NTSC)	$G = +2, R_L = 150\Omega$ to $V_S/2$		0.16		%
		$R_L = 1$ k Ω to $V_S/2$		0.05		
DP	Differential Phase Error (NTSC)	$G = +2, R_L = 150\Omega$ to $V_S/2$		0.05		deg.
		$R_L = 1$ k Ω to $V_S/2$		0.01		
DC PERFORMANCE						
V_{OS}	Input offset voltage			± 2	± 15	mV
$V_{OS\ TC}$	Offset voltage drift	$T_A = -40$ to $+125$ °C		± 5		μ V/ $^{\circ}$ C
I_B	Input bias current			4		pA
I_{OS}	Input offset current			2		pA
A_{VOL}	Open-loop voltage gain	$R_L = 2$ k Ω to $V_S/2, V_O = 0.5$ V to 2.5 V		98		dB
		$R_L = 150\Omega$ to $V_S/2, V_O = 0.5$ V to 2.5 V		82		
INPUT CHARACTERISTICS						
R_{IN}	Input Resistance	Common mode		1		G Ω
C_{IN}	Input capacitance	Common mode		2		pF
V_{CM}	Common-mode voltage range	CMRR ≥ 50 dB		-0.2	4	V
CMRR	Common-mode rejection ratio	$V_{CM} = 0$ V to 1.5 V		95		dB
OUTPUT						
V_{OH}	High output voltage swing	$R_L = 2$ k Ω to $V_S/2$		4.9		V
		$R_L = 150\Omega$ to $V_S/2$		4.8		

Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Low output voltage swing	$R_L = 2k\Omega$ to $V_S/2$		60		mV
		$R_L = 150\Omega$ to $V_S/2$		370		
I_{OUT}	Output Current	$V_{OUT} = 0.5V$ from either supply		± 65		
I_{SC}	Short-circuit current			± 130		mA
C_{LOAD}	Capacitive load drive	$G = +2$		40		pF
POWER SUPPLY						
V_S	Operating supply range		2.5		12.6	V
I_Q	Quiescent current /Amplifier			4.2		mA
PSRR	Power supply rejection ratio	$V_S = 4.0$ to $6V$		78		dB

$V_S = 10V$, $T_A = +25^\circ C$, $V_{CM} = V_O = V_S/2$, and $R_L = 2k\Omega$ to $V_S/2$, unless otherwise noted.
Boldface limits apply over the specified temperature range, $T_A = -40^\circ C$ to $+125^\circ C$.

DYNAMIC PERFORMANCE

BW_{-3dB}	-3 dB Small Signal Bandwidth	$G = +1$, $V_O = 0.2V_{PP}$		105		MHz
		$G = +2$, -1 , $V_O = 0.2V_{PP}$		43		
$BW_{0.1dB}$	Bandwidth for 0.1 dB Flatness	$G = +2$, $V_O = 0.2V_{PP}$, $R_L = 150\Omega$ to $V_S/2$, $R_F = 402\Omega$		6		MHz
SR	Slew rate	$G = -1$, $V_O = 2V$ step		107		V/ μs
BW_{FP}	Full Power Response	$G = +1$, $V_O = 2V_{PP}$		16		MHz
t_S	Settling time to 0.1%	$G = -1$, $V_O = 2V$ step		66		ns

NOISE/DISTORTION PERFORMANCE

THD	Total harmonic distortion	$f_C = 5MHz$, $V_O = 2V_{PP}$, $G = +2$		-53		dBc
e_n	Input voltage noise density	$f = 100kHz$		27		nV/ \sqrt{Hz}
i_n	Input current noise density	$f = 10kHz$		3		pA/ \sqrt{Hz}
DG	Differential Gain Error (NTSC)	$G = +2$, $R_L = 150\Omega$ to $V_S/2$		0.15		%
		$R_L = 1k\Omega$ to $V_S/2$		0.02		
DP	Differential Phase Error (NTSC)	$G = +2$, $R_L = 150\Omega$ to $V_S/2$		0.05		deg.
		$R_L = 1k\Omega$ to $V_S/2$		0.02		

DC PERFORMANCE

V_{OS}	Input offset voltage			± 2	± 15	mV
$V_{OS TC}$	Offset voltage drift	$T_A = -40$ to $+125^\circ C$		± 5		$\mu V/^\circ C$
I_B	Input bias current			4		pA
I_{OS}	Input offset current			2		pA
A_{VOL}	Open-loop voltage gain	$R_L = 2k\Omega$ to $V_S/2$, $V_O = 0.5V$ to $2.5V$		96		dB
		$R_L = 150\Omega$ to $V_S/2$, $V_O = 0.5V$ to $2.5V$		82		

INPUT CHARACTERISTICS

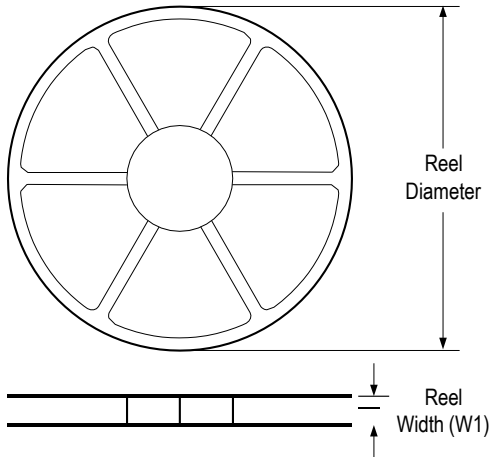
R_{IN}	Input Resistance	Common mode		1		G Ω
C_{IN}	Input capacitance	Common mode		2		pF

Electrical Characteristics

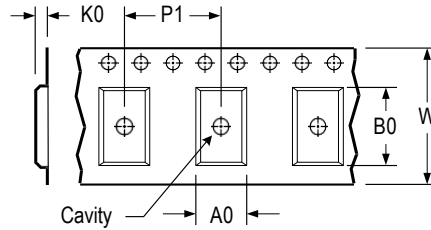
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CM}	Common-mode voltage range	$CMRR \geq 50dB$	-0.2		9	V
CMRR	Common-mode rejection ratio	$V_{CM} = 0V$ to 1.5 V		95		dB
OUTPUT						
V_{OH}	High output voltage swing	$R_L = 2k\Omega$ to $V_S/2$		4.91		V
		$R_L = 150\Omega$ to $V_S/2$		4.52		
V_{OL}	Low output voltage swing	$R_L = 2k\Omega$ to $V_S/2$		-4.9		V
		$R_L = 150\Omega$ to $V_S/2$		-4.5		
I_{OUT}	Output Current	$V_{OUT} = 0.5V$ from either supply		± 70		
I_{SC}	Short-circuit current			± 150		mA
C_{LOAD}	Capacitive load drive	$G = +2$		40		pF
POWER SUPPLY						
V_S	Operating supply range		2.5		12.6	V
I_Q	Quiescent current /Amplifier			4.4		mA
PSRR	Power supply rejection ratio	$V_S = \pm 4.5 V$ to $\pm 5.5 V$		78		dB
THERMAL CHARACTERISTICS						
T_A	Operating temperature range	SOT23-5L	-40		+85	°C
		Other packages	-40		+125	
θ_{JA}	Package Thermal Resistance	SOT23-5L		190		°C/W
		MSOP-8L		201		
		SOIC-8L		125		
		TSSOP-14L		112		
		SOIC-14L		115		

Tape and Reel Information

REEL DIMENSIONS

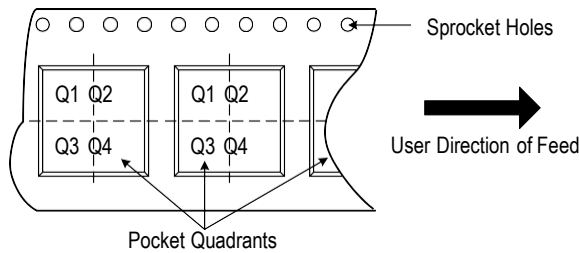


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

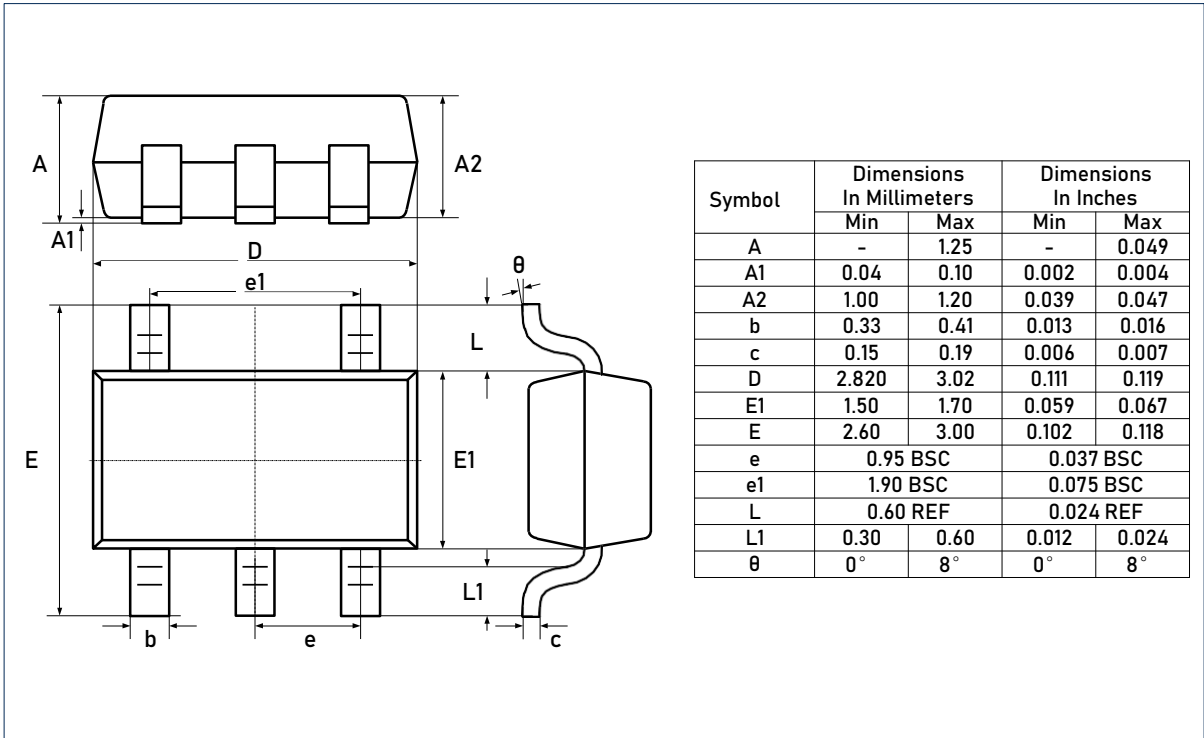


* All dimensions are nominal

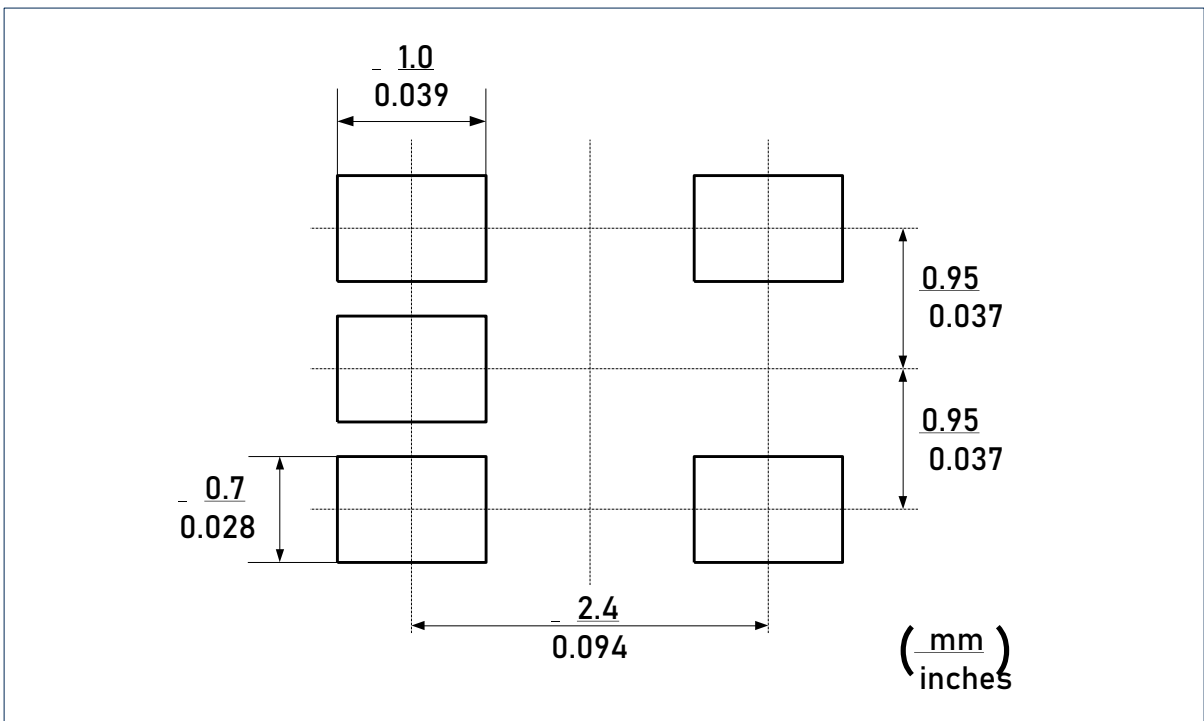
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTA6041XT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3
LTA6041XS8/R8	SOIC	8	4 000	330	12.4	6.6	5.3	2.0	8.0	12.0	Q1
LTA6042XS8/R8	SOIC	8	4 000	330	12.4	6.6	5.3	2.0	8.0	12.0	Q1
LTA6042XV8/R6	MSOP	8	3 000	330	12.4	5.0	3.5	2.0	8.0	12.0	Q1
LTA6044XS14/R5	SOIC	14	2 500	330	18	8.5	1.1	2.0	8.5	1.6	Q1
LTA6044XT14/R6	TSSOP	14	3 000	330	18	8.5	1.1	2.0	8.5	1.6	Q1

Package Outlines

DIMENSIONS, SOT23-5L

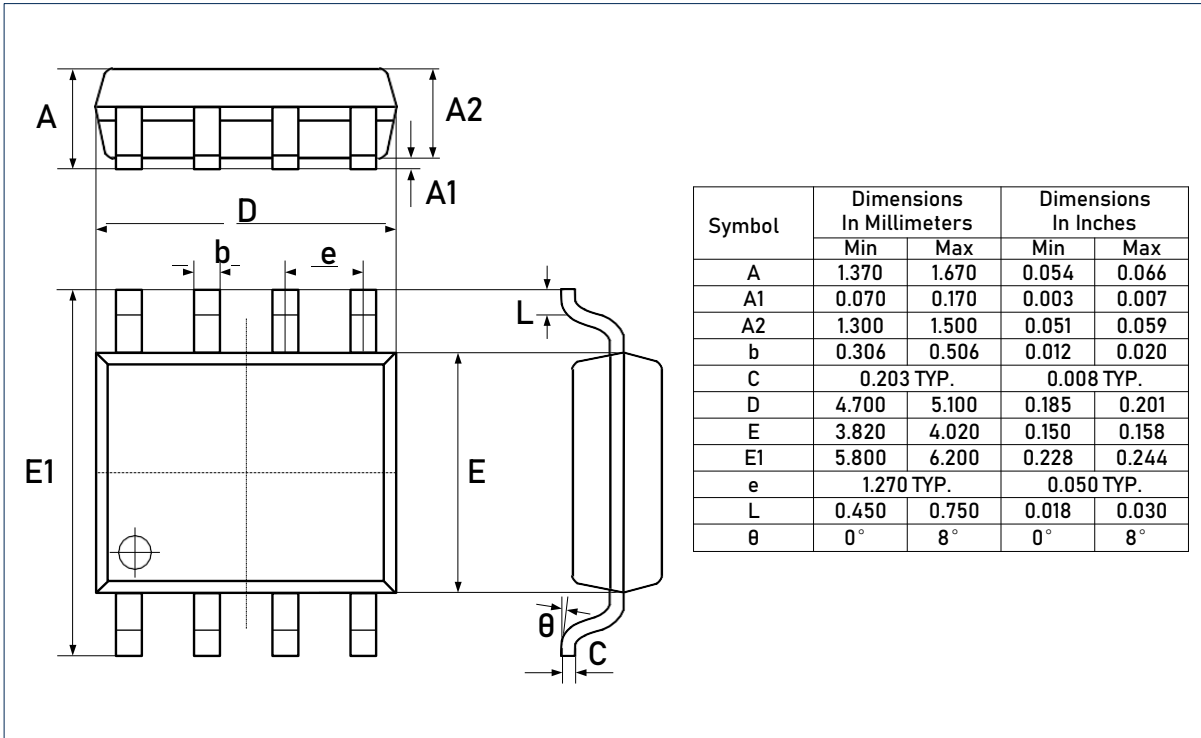


RECOMMENDED SOLDERING FOOTPRINT, SOT23-5L

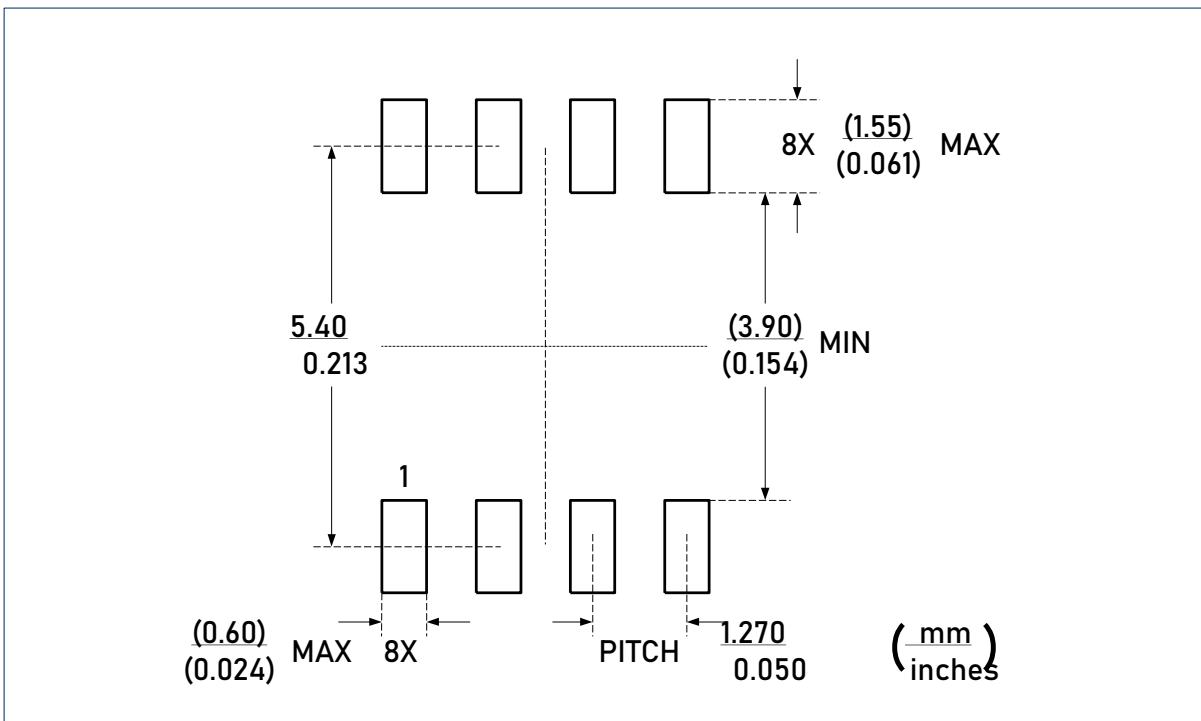


Package Outlines (continued)

DIMENSIONS, SOIC-8L



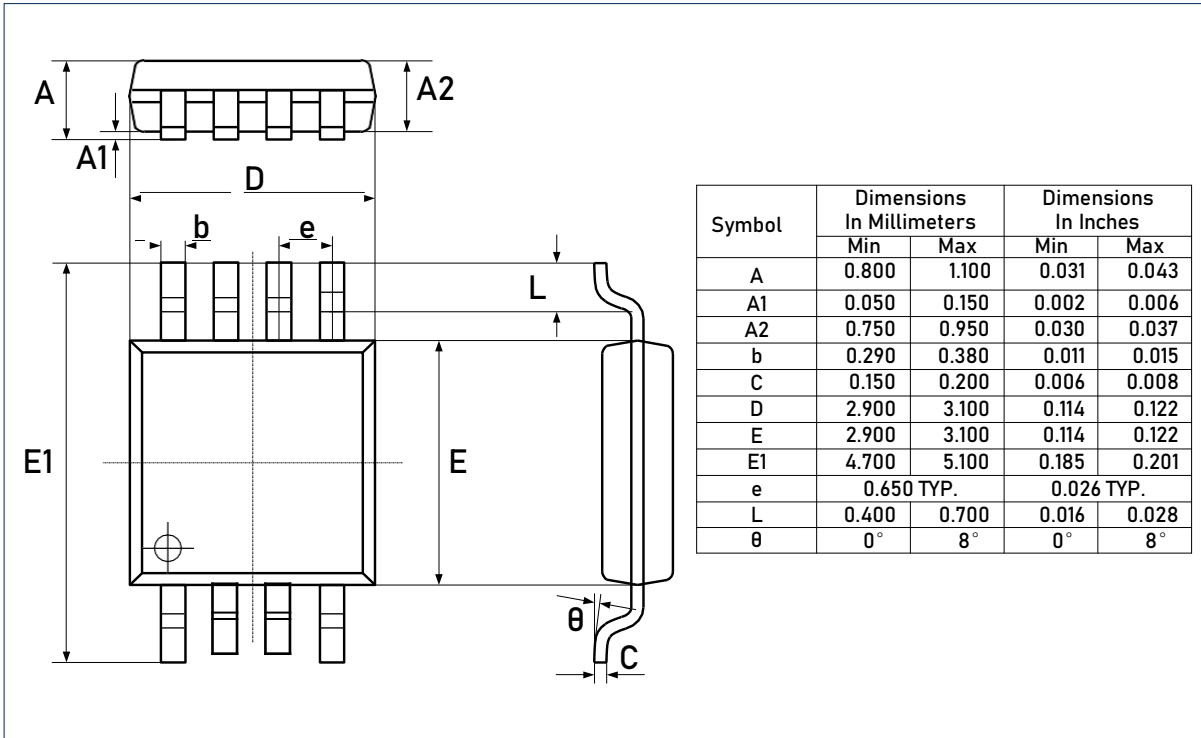
RECOMMENDED SOLDERING FOOTPRINT, SOIC-8L



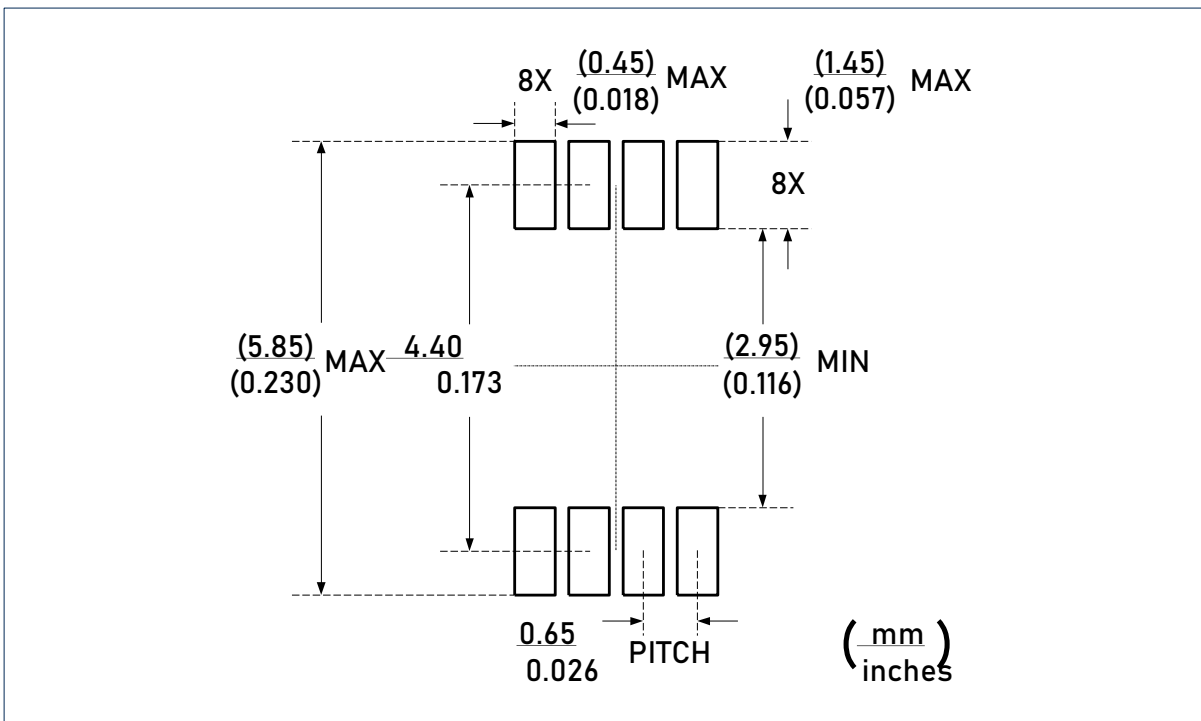
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Package Outlines (continued)

DIMENSIONS, MSOP-8L

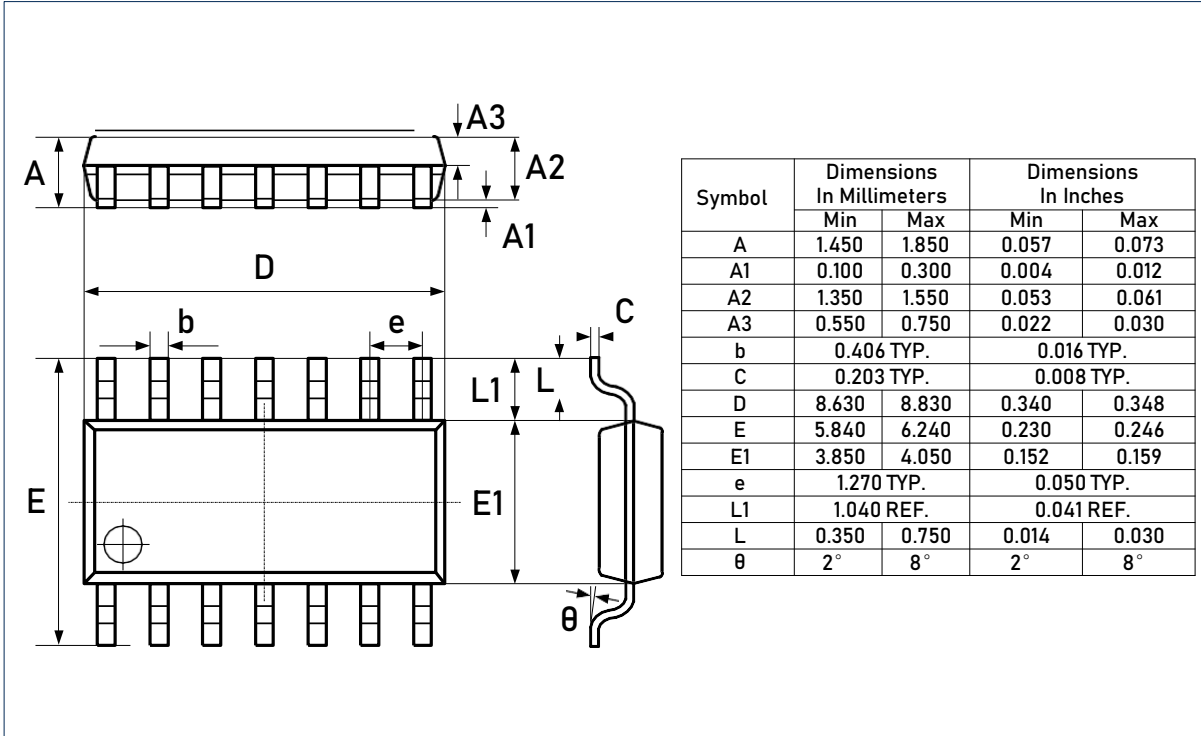


RECOMMENDED SOLDERING FOOTPRINT, MSOP-8L

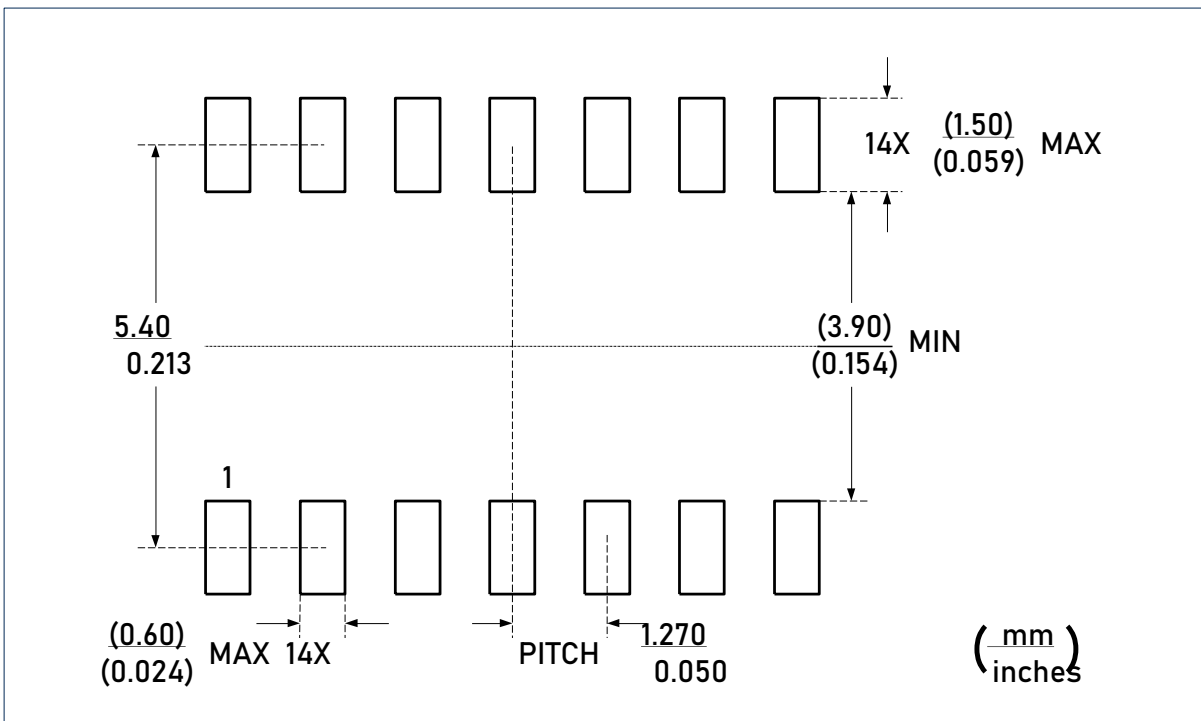


Package Outlines (continued)

DIMENSIONS, SOIC-14L



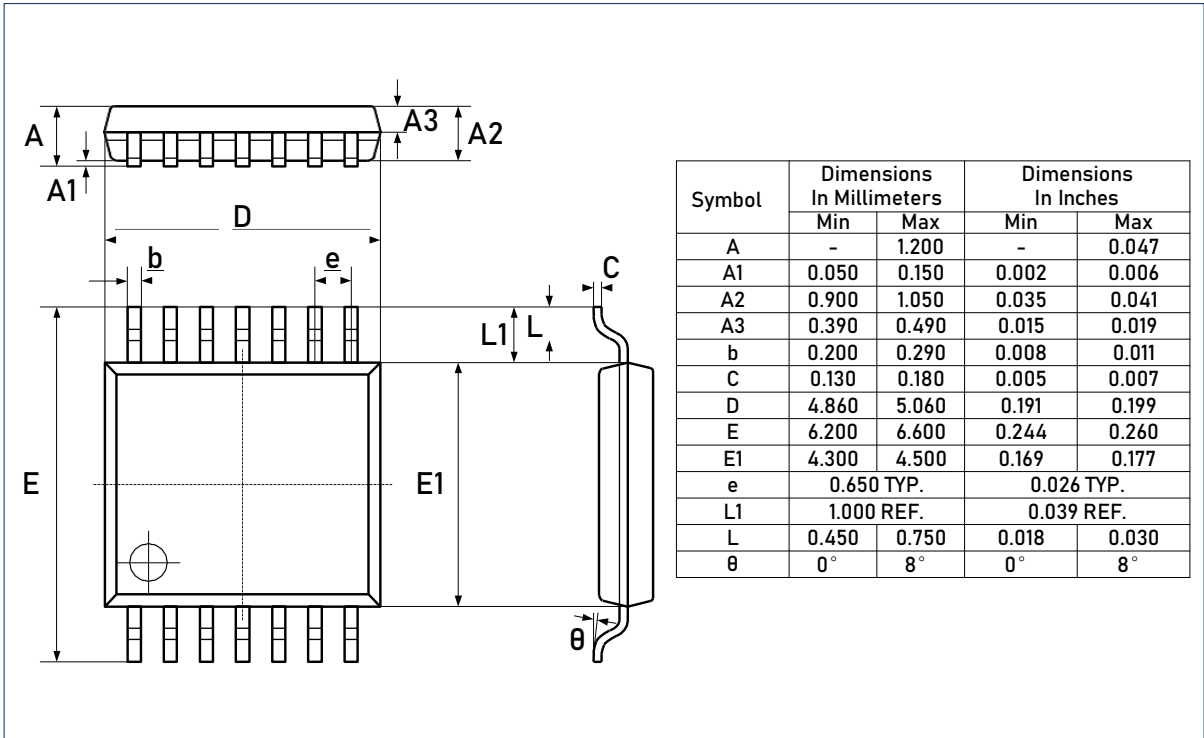
RECOMMENDED SOLDERING FOOTPRINT, SOIC-14L



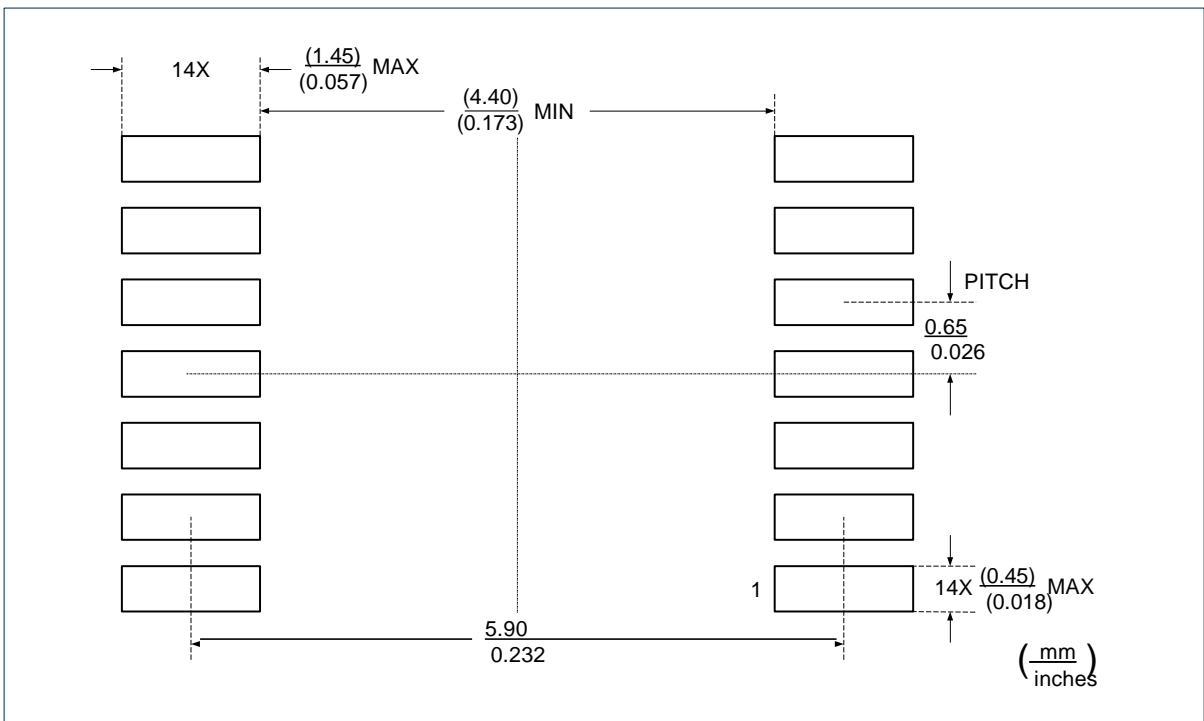
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Package Outlines (continued)

DIMENSIONS, TSSOP-14L



RECOMMENDED SOLDERING FOOTPRINT, TSSOP-14L



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For additional product information, or full datasheet, please contact with the Linearin's Sales Department or Representatives.