# SN74LS193 (LX)
# Presettable Synchronous 4-bit Binary up/down Counter; Asynchronous Reset

# Product Specification

**Specification Revision History:**

| Version | Date | Description |
|---|---|---|
| 2021-06-A1 | 2021-06 | New |
| 2023-04-B1 | 2023-04 | Update the template |
| | | |
| | | |

# Contents

## 1、General Description

The SN74LS193 is a 4-bit synchronous binary up/down counter. Separate up/down clocks, CPU and CPD respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CPU clock is pulsed while CPD is held HIGH, the device will count up. If the CPD clock is pulsed while CPU is held HIGH, the device will count down. Only one clock input can be held HIGH at any time to guarantee predictable behavior. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input ($\overline{PL}$).The terminal count up ($\overline{TCU}$) and terminal count down ($\overline{TCD}$) outputs are normally HIGH. When the circuit has reached the maximum count state of 15, the next HIGH-to-LOW transition of CPU will cause $\overline{TCU}$ to go LOW. $\overline{TCU}$ will stay LOW until CPU goes HIGH again, duplicating the count up clock. Likewise, the $\overline{TCD}$ output will go LOW when the circuit is in the zero state and the CPD goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added. The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D0 to D3) is loaded into the counter and appears on the outputs (Q0 to Q3) regardless of the conditions of the clock inputs when the parallel load ($\overline{PL}$) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs (Q0 to Q3) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of $V_{CC}$.

**Features:**

- Synchronous reversible 4-bit binary counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic
- Specified from -40℃ to +125℃
- Packaging information: DIP16/SOP16/TSSOP16

**Ordering Information:**

**Tube packing specifications:**

| Part number | Packaging form | Marking code | Tube quantity | Boxed tube quantity | Boxed quantity | Notes |
|---|---|---|---|---|---|---|
| SN74LS193N (LX) | DIP16 | SN74LS193N | 25 PCS/tube | 40 tube/box | 1000 PCS/box | Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm |
| SN74LS193D (LX) | SOP16 | LS193 | 50 PCS/tube | 200 tube/box | 10000 PCS/box | Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm |
| SN74LS193PW(LX) | TSSOP16 | LS193 | 96 PCS/tube | 200 tube/box | 19200 PCS/box | Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm |

**Reel packing specifications:**

| Part number | Packaging form | Marking code | Reel quantity | Boxed reel quantity | Notes |
|---|---|---|---|---|---|
| SN74LS193DR(LX) | SOP16 | LS193 | 2500 PCS/reel | 5000 PCS/box | Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm |
| SN74LS193PW(LX) | TSSOP16 | LS193 | 5000 PCS/reel | 10000 PCS/box | Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm |

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

## 2、Block Diagram And Pin Description

### 2.1、Block Diagram

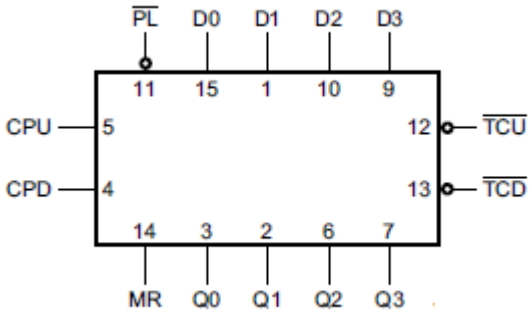



Figure 1. Logic symbol

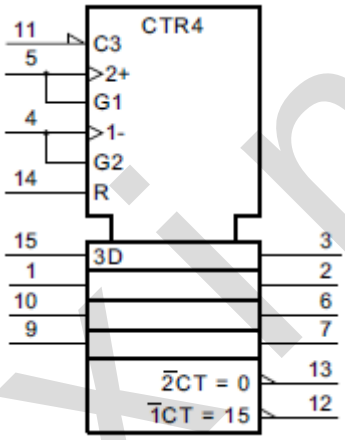



Figure 2. IEC logic symbol

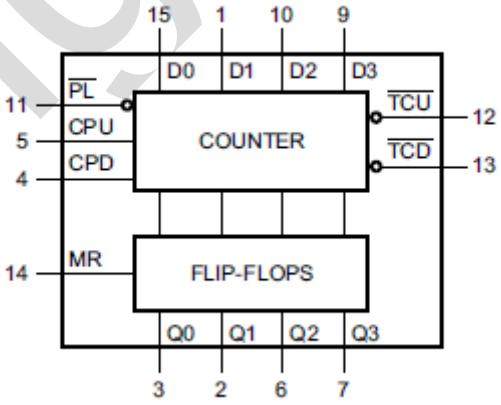



Figure 3. Functional diagram

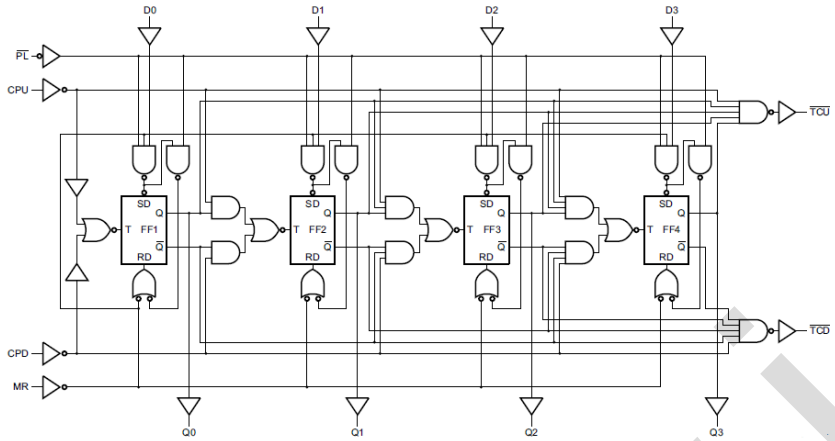
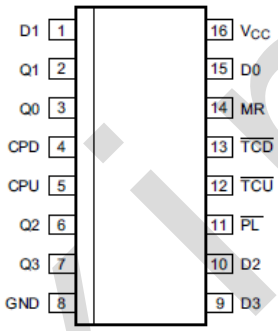



Figure 4. Logic diagram

## 2.2、Pin Configurations




## 2.3、Pin Description

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | D1 | data input 1 |
| 2 | Q1 | flip-flop output 1 |
| 3 | Q0 | flip-flop output 0 |
| 4 | CPD | count down clock input |
| 5 | CPU | count up clock input |
| 6 | Q2 | flip-flop output 2 |
| 7 | Q3 | flip-flop output 3 |
| 8 | GND | ground (0V) |
| 9 | D3 | data input 3 |
| 10 | D2 | data input 2 |
| 11 | $\overline{PL}$ | asynchronous parallel load input (active LOW) |
| 12 | $\overline{TCU}$ | terminal count up (carry) output (active LOW) |
| 13 | $\overline{TCD}$ | terminal count down (borrow) output (active LOW) |
| 14 | MR | asynchronous master reset input (active HIGH) |
| 15 | D0 | data input 0 |
| 16 | $V_{CC}$ | supply voltage |

Note: CPD, CPU is LOW-to-HIGH, edge triggered.

### 2.4、Function Table

| Operating mode | Input | | | | | | | | Output | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MR | $\overline{PL}$ | CPU | CPD | D0 | D1 | D2 | D3 | Q0 | Q1 | Q2 | Q3 | $\overline{TCU}$ | $\overline{TCD}$ |
| Reset (clear) | H | X | X | L | X | X | X | X | L | L | L | L | H | L |
| | H | X | X | H | X | X | X | X | L | L | L | L | H | H |
| Parallel load | L | L | X | L | L | L | L | L | L | L | L | L | H | L |
| | L | L | X | H | L | L | L | L | L | L | L | L | H | H |
| | L | L | L | X | H | H | H | H | H | H | H | H | L | H |
| | L | L | H | X | H | H | H | H | H | H | H | H | H | H |
| Count up | L | H | ↑ | H | X | X | X | X | count up | | | | H | H |
| Count down | L | H | H | ↑ | X | X | X | X | count down | | | | H | H |

Note:

[1] H=HIGH voltage level; L=LOW voltage level; X=don't care; ↑=LOW-to-HIGH transition.

[2] $\overline{TCU}$=CPU at terminal count up (HHHH).

[3] $\overline{TCD}$=CPD at terminal count down (LLLL).

## 3、Electrical Parameter

### 3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

| Parameter | Symbol | Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| supply voltage | $V_{CC}$ | - | | -0.5 | +7.0 | V |
| input clamping current | $I_{IK}$ | $V_I$ < -0.5V or $V_I$ > $V_{CC}$+0.5V | | - | ±20 | mA |
| output clamping current | $I_{OK}$ | $V_O$ < -0.5V or $V_O$ > $V_{CC}$+0.5V | | - | ±20 | mA |
| output current | $I_O$ | $V_O$= -0.5V to ($V_{CC}$+0.5V) | | - | ±25 | mA |
| supply current | $I_{CC}$ | - | | - | 50 | mA |
| ground current | $I_{GND}$ | - | | - | -50 | mA |
| storage temperature | $T_{stg}$ | - | | -65 | +150 | ℃ |
| total power dissipation | $P_{tot}$ | - | | - | 500 | mW |
| Soldering temperature | $T_L$ | 10s | DIP | 245 | | ℃ |
| | | | SOP/TSSOP | 260 | | ℃ |

### 3.2、Recommended Operating Conditions

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| supply voltage | $V_{CC}$ | - | | 2.0 | 5.0 | 6.0 | V |
| input voltage | $V_I$ | - | | 0 | - | $V_{CC}$ | V |
| output voltage | $V_O$ | - | | 0 | - | $V_{CC}$ | V |
| input transition rise and fall rate | $\Delta t/\Delta V$ | - | $V_{CC}$=2.0V | - | - | 625 | ns/V |
| | | | $V_{CC}$=4.5V | - | 1.67 | 139 | ns/V |
| | | | $V_{CC}$=6.0V | - | - | 83 | ns/V |
| ambient temperature | $T_{amb}$ | - | | -40 | - | +125 | ℃ |

### 3.3、Electrical Characteristics

#### 3.3.1、DC Characteristics 1

($T_{amb}$=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| HIGH-level input voltage | $V_{IH}$ | $V_{CC}$=2.0V | | 1.5 | 1.2 | - | V |
| | | $V_{CC}$=4.5V | | 3.15 | 2.4 | - | V |
| | | $V_{CC}$=6.0V | | 4.2 | 3.2 | - | V |
| LOW-level input voltage | $V_{IL}$ | $V_{CC}$=2.0V | | - | 0.8 | 0.5 | V |
| | | $V_{CC}$=4.5V | | - | 2.1 | 1.35 | V |
| | | $V_{CC}$=6.0V | | - | 2.8 | 1.8 | V |
| HIGH-level output voltage | $V_{OH}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_O$=-20uA; $V_{CC}$=2.0V | 1.9 | 2.0 | - | V |
| | | | $I_O$=-20uA; $V_{CC}$=4.5V | 4.4 | 4.5 | - | V |
| | | | $I_O$=-20uA; $V_{CC}$=6.0V | 5.9 | 6.0 | - | V |
| | | | $I_O$=-4mA; $V_{CC}$=4.5V | 3.98 | 4.32 | - | V |
| | | | $I_O$=-5.2mA; $V_{CC}$=6.0V | 5.48 | 5.81 | - | V |
| LOW-level output voltage | $V_{OL}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_O$=20uA; $V_{CC}$=2.0V | - | 0 | 0.1 | V |
| | | | $I_O$=20uA; $V_{CC}$=4.5V | - | 0 | 0.1 | V |
| | | | $I_O$=20uA; $V_{CC}$=6.0V | - | 0 | 0.1 | V |
| | | | $I_O$=4mA; $V_{CC}$=4.5V | - | 0.15 | 0.26 | V |
| | | | $I_O$=5.2mA; $V_{CC}$=6.0V | - | 0.16 | 0.26 | V |
| input leakage current | $I_I$ | $V_I$=$V_{CC}$ or GND; $V_{CC}$=6.0V | | - | - | ±1.0 | uA |
| supply current | $I_{CC}$ | $V_I$=$V_{CC}$ or GND; $I_O$=0A; $V_{CC}$=6.0V | | - | - | 8.0 | uA |
| input capacitance | $C_I$ | - | | - | 3.5 | - | pF |

### 3.3.2、DC Characteristics 2

($T_{amb}$=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| HIGH-level input voltage | $V_{IH}$ | $V_{CC}$=2.0V | | 1.5 | - | - | V |
| | | $V_{CC}$=4.5V | | 3.15 | - | - | V |
| | | $V_{CC}$=6.0V | | 4.2 | - | - | V |
| LOW-level input voltage | $V_{IL}$ | $V_{CC}$=2.0V | | - | - | 0.5 | V |
| | | $V_{CC}$=4.5V | | - | - | 1.35 | V |
| | | $V_{CC}$=6.0V | | - | - | 1.8 | V |
| HIGH-level output voltage | $V_{OH}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_O$=-20uA; $V_{CC}$=2.0V | 1.9 | - | - | V |
| | | | $I_O$=-20uA; $V_{CC}$=4.5V | 4.4 | - | - | V |
| | | | $I_O$=-20uA; $V_{CC}$=6.0V | 5.9 | - | - | V |
| | | | $I_O$=-4mA; $V_{CC}$=4.5V | 3.84 | - | - | V |
| | | | $I_O$=-5.2mA; $V_{CC}$=6.0V | 5.34 | - | - | V |
| LOW-level output voltage | $V_{OL}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_O$=20uA; $V_{CC}$=2.0V | - | - | 0.1 | V |
| | | | $I_O$=20uA; $V_{CC}$=4.5V | - | - | 0.1 | V |
| | | | $I_O$=20uA; $V_{CC}$=6.0V | - | - | 0.1 | V |
| | | | $I_O$=4mA; $V_{CC}$=4.5V | - | - | 0.33 | V |
| | | | $I_O$=5.2mA; $V_{CC}$=6.0V | - | - | 0.33 | V |
| input leakage current | $I_I$ | $V_I$=$V_{CC}$ or GND; $V_{CC}$=6.0V | | - | - | ±1.0 | uA |
| supply current | $I_{CC}$ | $V_I$=$V_{CC}$ or GND; $I_O$=0A; $V_{CC}$=6.0V | | - | - | 80 | uA |

### 3.3.3、DC Characteristics 3

($T_{amb}$=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| HIGH-level input voltage | $V_{IH}$ | $V_{CC}$=2.0V | | 1.5 | - | - | V |
| | | $V_{CC}$=4.5V | | 3.15 | - | - | V |
| | | $V_{CC}$=6.0V | | 4.2 | - | - | V |
| LOW-level input voltage | $V_{IL}$ | $V_{CC}$=2.0V | | - | - | 0.5 | V |
| | | $V_{CC}$=4.5V | | - | - | 1.35 | V |
| | | $V_{CC}$=6.0V | | - | - | 1.8 | V |
| HIGH-level output voltage | $V_{OH}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_O$=-20uA; $V_{CC}$=2.0V | 1.9 | - | - | V |
| | | | $I_O$=-20uA; $V_{CC}$=4.5V | 4.4 | - | - | V |
| | | | $I_O$=-20uA; $V_{CC}$=6.0V | 5.9 | - | - | V |
| | | | $I_O$=-4mA; $V_{CC}$=4.5V | 3.7 | - | - | V |
| | | | $I_O$=-5.2mA; $V_{CC}$=6.0V | 5.2 | - | - | V |
| LOW-level output voltage | $V_{OL}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_O$=20uA; $V_{CC}$=2.0V | - | - | 0.1 | V |
| | | | $I_O$=20uA; $V_{CC}$=4.5V | - | - | 0.1 | V |
| | | | $I_O$=20uA; $V_{CC}$=6.0V | - | - | 0.1 | V |
| | | | $I_O$=4mA; $V_{CC}$=4.5V | - | - | 0.4 | V |
| | | | $I_O$=5.2mA; $V_{CC}$=6.0V | - | - | 0.4 | V |
| input leakage current | $I_I$ | $V_I$=$V_{CC}$ or GND; $V_{CC}$=6.0V | | - | - | ±1.0 | uA |
| supply current | $I_{CC}$ | $V_I$=$V_{CC}$ or GND; $I_O$=0A; $V_{CC}$=6.0V | | - | - | 160 | uA |

### 3.3.4、AC Characteristics 1

($T_{amb}$=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| propagation delay | $t_{pd}$ | CPU, CPD to Qn; see Figure 6 | $V_{CC}$=2.0V | - | 63 | 215 | ns |
| | | | $V_{CC}$=4.5V | - | 23 | 43 | ns |
| | | | $V_{CC}$=6.0V | - | 18 | 37 | ns |
| | | CPU to $\overline{TCU}$; see Figure 7 | $V_{CC}$=2.0V | - | 39 | 125 | ns |
| | | | $V_{CC}$=4.5V | - | 14 | 25 | ns |
| | | | $V_{CC}$=6.0V | - | 11 | 21 | ns |
| | | CPD to $\overline{TCD}$; see Figure 7 | $V_{CC}$=2.0V | - | 39 | 125 | ns |
| | | | $V_{CC}$=4.5V | - | 14 | 25 | ns |
| | | | $V_{CC}$=6.0V | - | 11 | 21 | ns |
| | | $\overline{PL}$ to Qn; see Figure 8 | $V_{CC}$=2.0V | - | 69 | 220 | ns |
| | | | $V_{CC}$=4.5V | - | 25 | 44 | ns |
| | | | $V_{CC}$=6.0V | - | 20 | 37 | ns |
| | | MR to Qn; see Figure 9 | $V_{CC}$=2.0V | - | 58 | 200 | ns |
| | | | $V_{CC}$=4.5V | - | 21 | 40 | ns |
| | | | $V_{CC}$=6.0V | - | 17 | 34 | ns |
| | | Dn to Qn; see Figure 8 | $V_{CC}$=2.0V | - | 69 | 210 | ns |
| | | | $V_{CC}$=4.5V | - | 25 | 42 | ns |
| | | | $V_{CC}$=6.0V | - | 20 | 36 | ns |
| | | $\overline{PL}$ to $\overline{TCU}$, $\overline{PL}$ to $\overline{TCD}$; see Figure 11 | $V_{CC}$=2.0V | - | 80 | 290 | ns |
| | | | $V_{CC}$=4.5V | - | 29 | 58 | ns |
| | | | $V_{CC}$=6.0V | - | 23 | 49 | ns |
| | | MR to $\overline{TCU}$, MR to $\overline{TCD}$; see Figure 11 | $V_{CC}$=2.0V | - | 74 | 285 | ns |
| | | | $V_{CC}$=4.5V | - | 27 | 57 | ns |
| | | | $V_{CC}$=6.0V | - | 22 | 48 | ns |
| | | Dn to $\overline{TCU}$, Dn to $\overline{TCD}$; see Figure 11 | $V_{CC}$=2.0V | - | 80 | 290 | ns |
| | | | $V_{CC}$=4.5V | - | 29 | 58 | ns |
| | | | $V_{CC}$=6.0V | - | 23 | 49 | ns |
| HIGH to LOW output transition time | $t_{THL}$ | see Figure 9 | $V_{CC}$=2.0V | - | 19 | 75 | ns |
| | | | $V_{CC}$=4.5V | - | 7 | 15 | ns |
| | | | $V_{CC}$=6.0V | - | 6 | 13 | ns |
| LOW to HIGH output transition time | $t_{TLH}$ | see Figure 9 | $V_{CC}$=2.0V | - | 19 | 75 | ns |
| | | | $V_{CC}$=4.5V | - | 7 | 15 | ns |
| | | | $V_{CC}$=6.0V | - | 6 | 13 | ns |
| pulse width | $t_W$ | CPU, CPD (HIGH or LOW); | $V_{CC}$=2.0V | 100 | 22 | - | ns |
| | | | $V_{CC}$=4.5V | 20 | 8 | - | ns |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | see Figure 6 | $V_{CC}$=6.0V | 17 | 6 | - | ns |
| | | MR (HIGH); see Figure 9 | $V_{CC}$=2.0V | 100 | 25 | - | ns |
| | | | $V_{CC}$=4.5V | 20 | 9 | - | ns |
| | | | $V_{CC}$=6.0V | 17 | 7 | - | ns |
| | | $\overline{PL}$ (LOW); see Figure 8 | $V_{CC}$=2.0V | 100 | 19 | - | ns |
| | | | $V_{CC}$=4.5V | 20 | 7 | - | ns |
| | | | $V_{CC}$=6.0V | 17 | 6 | - | ns |
| recovery time | $t_{rec}$ | $\overline{PL}$ to CPU, CPD; see Figure 8 | $V_{CC}$=2.0V | 50 | 8 | - | ns |
| | | | $V_{CC}$=4.5V | 10 | 3 | - | ns |
| | | | $V_{CC}$=6.0V | 9 | 2 | - | ns |
| | | MR to CPU, CPD; see Figure 9 | $V_{CC}$=2.0V | 50 | 0 | - | ns |
| | | | $V_{CC}$=4.5V | 10 | 0 | - | ns |
| | | | $V_{CC}$=6.0V | 9 | 0 | - | ns |
| set-up time | $t_{su}$ | Dn to $\overline{PL}$; see Figure 10; note: CPU = CPD = HIGH | $V_{CC}$=2.0V | 80 | 22 | - | ns |
| | | | $V_{CC}$=4.5V | 16 | 8 | - | ns |
| | | | $V_{CC}$=6.0V | 14 | 6 | - | ns |
| hold time | $t_h$ | Dn to $\overline{PL}$; see Figure 10 | $V_{CC}$=2.0V | 0 | -14 | - | ns |
| | | | $V_{CC}$=4.5V | 0 | -5 | - | ns |
| | | | $V_{CC}$=6.0V | 0 | -4 | - | ns |
| | | CPU to CPD, CPD to CPU; see Figure 12 | $V_{CC}$=2.0V | 80 | 22 | - | ns |
| | | | $V_{CC}$=4.5V | 16 | 8 | - | ns |
| | | | $V_{CC}$=6.0V | 8 | 6 | - | ns |
| maximum frequency | $f_{max}$ | CPU, CPD; see Figure 6 | $V_{CC}$=2.0V | 4.0 | 13.5 | - | MHz |
| | | | $V_{CC}$=4.5V | 20 | 41 | - | MHz |
| | | | $V_{CC}$=6.0V | 24 | 49 | - | MHz |
| power dissipation capacitance | $C_{PD}$ | $V_I$=GND to $V_{CC}$; $V_{CC}$=5V; $f_i$=1MHz | | - | 24 | - | pF |

Note:

[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.

[2] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i\times N+\sum(C_L\times V_{CC}^2\times f_o)$ where:

$f_i$=input frequency in MHz;

$f_o$=output frequency in MHz;

$C_L$=output load capacitance in pF;

$V_{CC}$=supply voltage in V;

N=number of inputs switching;

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

### 3.3.5、AC Characteristics 2

($T_{amb}$=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| propagation delay | $t_{pd}$ | CPU, CPD to Qn; see Figure 6 | $V_{CC}$=2.0V | - | - | 270 | ns |
| | | | $V_{CC}$=4.5V | - | - | 54 | ns |
| | | | $V_{CC}$=6.0V | - | - | 46 | ns |
| | | CPU to $\overline{TCU}$; see Figure 7 | $V_{CC}$=2.0V | - | - | 155 | ns |
| | | | $V_{CC}$=4.5V | - | - | 31 | ns |
| | | | $V_{CC}$=6.0V | - | - | 26 | ns |
| | | CPD to $\overline{TCD}$; see Figure 7 | $V_{CC}$=2.0V | - | - | 155 | ns |
| | | | $V_{CC}$=4.5V | - | - | 31 | ns |
| | | | $V_{CC}$=6.0V | - | - | 26 | ns |
| | | $\overline{PL}$ to Qn; see Figure 8 | $V_{CC}$=2.0V | - | - | 275 | ns |
| | | | $V_{CC}$=4.5V | - | - | 55 | ns |
| | | | $V_{CC}$=6.0V | - | - | 47 | ns |
| | | MR to Qn; see Figure 9 | $V_{CC}$=2.0V | - | - | 250 | ns |
| | | | $V_{CC}$=4.5V | - | - | 50 | ns |
| | | | $V_{CC}$=6.0V | - | - | 43 | ns |
| | | Dn to Qn; see Figure 8 | $V_{CC}$=2.0V | - | - | 265 | ns |
| | | | $V_{CC}$=4.5V | - | - | 53 | ns |
| | | | $V_{CC}$=6.0V | - | - | 45 | ns |
| | | $\overline{PL}$ to $\overline{TCU}$, $\overline{PL}$ to $\overline{TCD}$; see Figure 11 | $V_{CC}$=2.0V | - | - | 365 | ns |
| | | | $V_{CC}$=4.5V | - | - | 73 | ns |
| | | | $V_{CC}$=6.0V | - | - | 62 | ns |
| | | MR to $\overline{TCU}$, MR to $\overline{TCD}$; see Figure 11 | $V_{CC}$=2.0V | - | - | 355 | ns |
| | | | $V_{CC}$=4.5V | - | - | 71 | ns |
| | | | $V_{CC}$=6.0V | - | - | 60 | ns |
| | | Dn to $\overline{TCU}$, Dn to $\overline{TCD}$; see Figure 11 | $V_{CC}$=2.0V | - | - | 365 | ns |
| | | | $V_{CC}$=4.5V | - | - | 73 | ns |
| | | | $V_{CC}$=6.0V | - | - | 62 | ns |
| HIGH to LOW output transition time | $t_{THL}$ | see Figure 9 | $V_{CC}$=2.0V | - | - | 95 | ns |
| | | | $V_{CC}$=4.5V | - | - | 19 | ns |
| | | | $V_{CC}$=6.0V | - | - | 16 | ns |
| LOW to HIGH output transition time | $t_{TLH}$ | see Figure 9 | $V_{CC}$=2.0V | - | - | 95 | ns |
| | | | $V_{CC}$=4.5V | - | - | 19 | ns |
| | | | $V_{CC}$=6.0V | - | - | 16 | ns |
| pulse width | $t_W$ | CPU, CPD (HIGH or LOW); see Figure 6 | $V_{CC}$=2.0V | 125 | - | - | ns |
| | | | $V_{CC}$=4.5V | 25 | - | - | ns |
| | | | $V_{CC}$=6.0V | 21 | - | - | ns |
| | | MR (HIGH); see Figure 9 | $V_{CC}$=2.0V | 125 | - | - | ns |
| | | | $V_{CC}$=4.5V | 25 | - | - | ns |
| | | | $V_{CC}$=6.0V | 21 | - | - | ns |
| | | $\overline{PL}$ (LOW); see Figure 8 | $V_{CC}$=2.0V | 125 | - | - | ns |
| | | | $V_{CC}$=4.5V | 25 | - | - | ns |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$=6.0V | 21 | - | - | ns |
| recovery time | $t_{rec}$ | $\overline{PL}$ to CPU, CPD; see Figure 8 | $V_{CC}$=2.0V | 65 | - | - | ns |
| | | | $V_{CC}$=4.5V | 13 | - | - | ns |
| | | | $V_{CC}$=6.0V | 11 | - | - | ns |
| | | MR to CPU, CPD; see Figure 9 | $V_{CC}$=2.0V | 65 | - | - | ns |
| | | | $V_{CC}$=4.5V | 13 | - | - | ns |
| | | | $V_{CC}$=6.0V | 11 | - | - | ns |
| set-up time | $t_{su}$ | Dn to $\overline{PL}$; see Figure 10; note: CPU = CPD = HIGH | $V_{CC}$=2.0V | 100 | - | - | ns |
| | | | $V_{CC}$=4.5V | 20 | - | - | ns |
| | | | $V_{CC}$=6.0V | 17 | - | - | ns |
| hold time | $t_h$ | Dn to $\overline{PL}$; see Figure 10 | $V_{CC}$=2.0V | 0 | - | - | ns |
| | | | $V_{CC}$=4.5V | 0 | - | - | ns |
| | | | $V_{CC}$=6.0V | 0 | - | - | ns |
| | | CPU to CPD, CPD to CPU; see Figure 12 | $V_{CC}$=2.0V | 100 | - | - | ns |
| | | | $V_{CC}$=4.5V | 20 | - | - | ns |
| | | | $V_{CC}$=6.0V | 17 | - | - | ns |
| maximum frequency | $f_{max}$ | CPU, CPD; see Figure 6 | $V_{CC}$=2.0V | 3.2 | - | - | MHz |
| | | | $V_{CC}$=4.5V | 16 | - | - | MHz |
| | | | $V_{CC}$=6.0V | 19 | - | - | MHz |

Note:

[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.

### 3.3.6、AC Characteristics 3

($T_{amb}$=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| propagation delay | $t_{pd}$ | CPU, CPD to Qn; see Figure 6 | $V_{CC}$=2.0V | - | - | 325 | ns |
| | | | $V_{CC}$=4.5V | - | - | 65 | ns |
| | | | $V_{CC}$=6.0V | - | - | 55 | ns |
| | | CPU to $\overline{TCU}$; see Figure 7 | $V_{CC}$=2.0V | - | - | 190 | ns |
| | | | $V_{CC}$=4.5V | - | - | 38 | ns |
| | | | $V_{CC}$=6.0V | - | - | 32 | ns |
| | | CPD to $\overline{TCD}$; see Figure 7 | $V_{CC}$=2.0V | - | - | 190 | ns |
| | | | $V_{CC}$=4.5V | - | - | 38 | ns |
| | | | $V_{CC}$=6.0V | - | - | 32 | ns |
| | | $\overline{PL}$ to Qn; see Figure 8 | $V_{CC}$=2.0V | - | - | 330 | ns |
| | | | $V_{CC}$=4.5V | - | - | 66 | ns |
| | | | $V_{CC}$=6.0V | - | - | 56 | ns |
| | | MR to Qn; see Figure 9 | $V_{CC}$=2.0V | - | - | 300 | ns |
| | | | $V_{CC}$=4.5V | - | - | 60 | ns |
| | | | $V_{CC}$=6.0V | - | - | 51 | ns |
| | | Dn to Qn; see Figure 8 | $V_{CC}$=2.0V | - | - | 315 | ns |
| | | | $V_{CC}$=4.5V | - | - | 63 | ns |
| | | | $V_{CC}$=6.0V | - | - | 54 | ns |
| | | $\overline{PL}$ to $\overline{TCU}$, $\overline{PL}$ to $\overline{TCD}$; see Figure 11 | $V_{CC}$=2.0V | - | - | 435 | ns |
| | | | $V_{CC}$=4.5V | - | - | 87 | ns |
| | | | $V_{CC}$=6.0V | - | - | 74 | ns |
| | | MR to $\overline{TCU}$, MR to $\overline{TCD}$; see Figure 11 | $V_{CC}$=2.0V | - | - | 430 | ns |
| | | | $V_{CC}$=4.5V | - | - | 86 | ns |
| | | | $V_{CC}$=6.0V | - | - | 73 | ns |
| | | Dn to $\overline{TCU}$, Dn to $\overline{TCD}$; see Figure 11 | $V_{CC}$=2.0V | - | - | 435 | ns |
| | | | $V_{CC}$=4.5V | - | - | 87 | ns |
| | | | $V_{CC}$=6.0V | - | - | 74 | ns |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| HIGH to LOW output transition time | $t_{THL}$ | see Figure 9 | $V_{CC}$=2.0V | - | - | 110 | ns |
| | | | $V_{CC}$=4.5V | - | - | 22 | ns |
| | | | $V_{CC}$=6.0V | - | - | 19 | ns |
| LOW to HIGH output transition time | $t_{TLH}$ | see Figure 9 | $V_{CC}$=2.0V | - | - | 110 | ns |
| | | | $V_{CC}$=4.5V | - | - | 22 | ns |
| | | | $V_{CC}$=6.0V | - | - | 19 | ns |
| pulse width | $t_W$ | CPU, CPD (HIGH or LOW); see Figure 6 | $V_{CC}$=2.0V | 150 | - | - | ns |
| | | | $V_{CC}$=4.5V | 30 | - | - | ns |
| | | | $V_{CC}$=6.0V | 26 | - | - | ns |
| | | MR (HIGH); see Figure 9 | $V_{CC}$=2.0V | 150 | - | - | ns |
| | | | $V_{CC}$=4.5V | 30 | - | - | ns |
| | | | $V_{CC}$=6.0V | 26 | - | - | ns |
| | | $\overline{PL}$ (LOW); see Figure 8 | $V_{CC}$=2.0V | 150 | - | - | ns |
| | | | $V_{CC}$=4.5V | 30 | - | - | ns |
| | | | $V_{CC}$=6.0V | 26 | - | - | ns |
| recovery time | $t_{rec}$ | $\overline{PL}$ to CPU, CPD; see Figure 8 | $V_{CC}$=2.0V | 75 | - | - | ns |
| | | | $V_{CC}$=4.5V | 15 | - | - | ns |
| | | | $V_{CC}$=6.0V | 13 | - | - | ns |
| | | MR to CPU, CPD; see Figure 9 | $V_{CC}$=2.0V | 75 | - | - | ns |
| | | | $V_{CC}$=4.5V | 15 | - | - | ns |
| | | | $V_{CC}$=6.0V | 13 | - | - | ns |
| set-up time | $t_{su}$ | Dn to $\overline{PL}$; see Figure 10; note: CPU = CPD = HIGH | $V_{CC}$=2.0V | 120 | - | - | ns |
| | | | $V_{CC}$=4.5V | 24 | - | - | ns |
| | | | $V_{CC}$=6.0V | 20 | - | - | ns |
| hold time | $t_h$ | Dn to $\overline{PL}$; see Figure 10 | $V_{CC}$=2.0V | 0 | - | - | ns |
| | | | $V_{CC}$=4.5V | 0 | - | - | ns |
| | | | $V_{CC}$=6.0V | 0 | - | - | ns |
| | | CPU to CPD, CPD to CPU; see Figure 12 | $V_{CC}$=2.0V | 120 | - | - | ns |
| | | | $V_{CC}$=4.5V | 24 | - | - | ns |
| | | | $V_{CC}$=6.0V | 20 | - | - | ns |
| maximum frequency | $f_{max}$ | CPU, CPD; see Figure 6 | $V_{CC}$=2.0V | 2.6 | - | - | MHz |
| | | | $V_{CC}$=4.5V | 13 | - | - | MHz |
| | | | $V_{CC}$=6.0V | 15 | - | - | MHz |

Note:

[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.

# 4、Testing Circuit

## 4.1、AC Testing Circuit

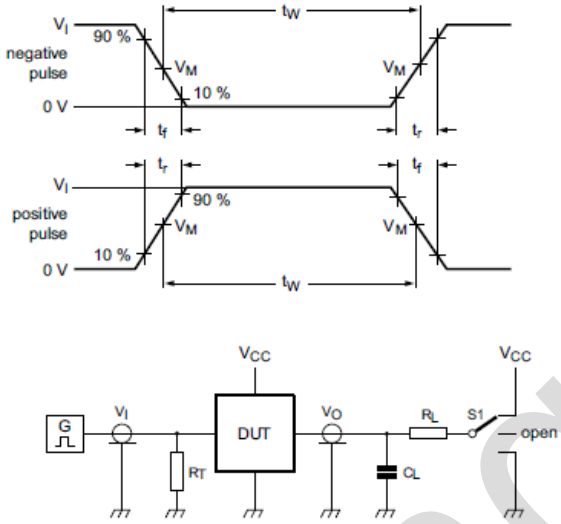



Figure 5. Test circuit for measuring switching times

Definitions for test circuit:

$R_L$=Load resistance.

$C_L$=Load capacitance including jig and probe capacitance.

$R_T$=Termination resistance should be equal to the output impedance $Z_o$ of the pulse generator.

S1=Test selection switch.

## 4.2、AC Testing Waveforms

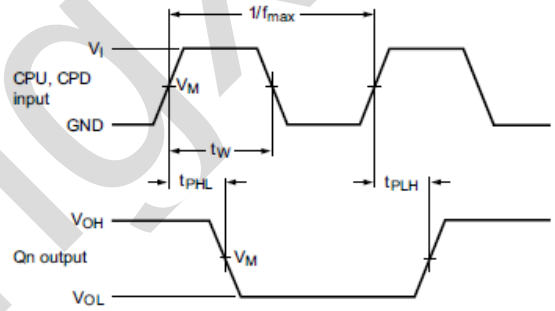



Figure 6. The clock (CPU, CPD) to output (Qn) propagation delays, the clock pulse width, and the maximum clock pulse frequency

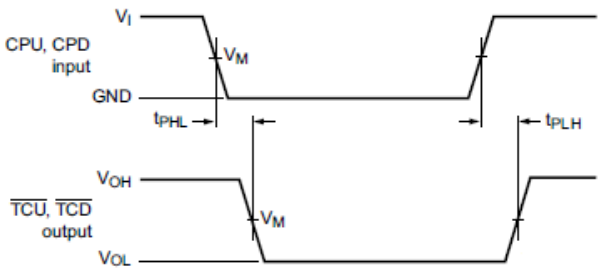



Figure 7. The clock (CPU, CPD) to terminal count output ($\overline{TCU}$, $\overline{TCD}$) propagation delays

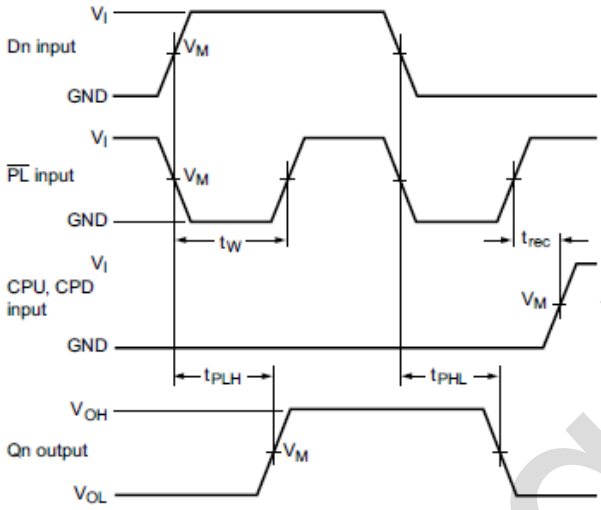



Figure 8. The parallel load input ($\overline{PL}$) and data (Dn) to Qn output propagation delays and $\overline{PL}$ removal time to clock input (CPU, CPD)

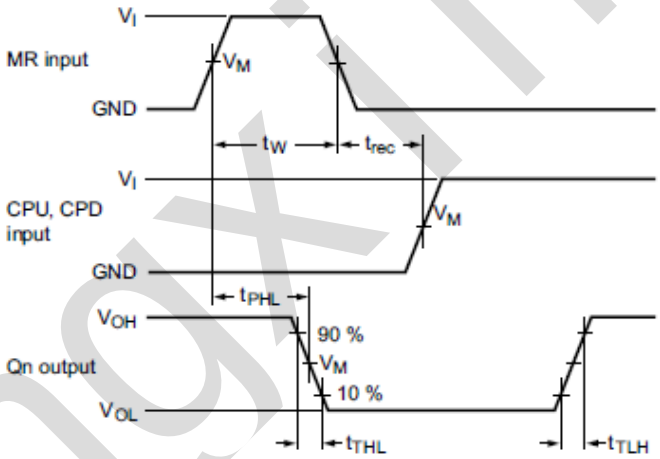



Figure 9. The master reset input (MR) pulse width, MR to Qn propagation delays, MR to CPU, CPD removal time and output transition times

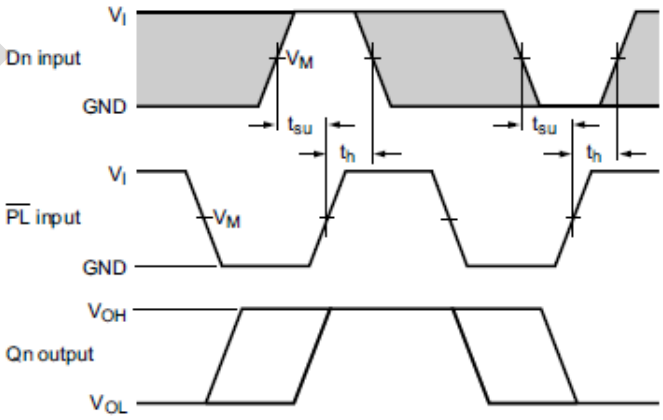



Figure 10. The data input (Dn) to parallel load input ($\overline{PL}$) set-up and hold times

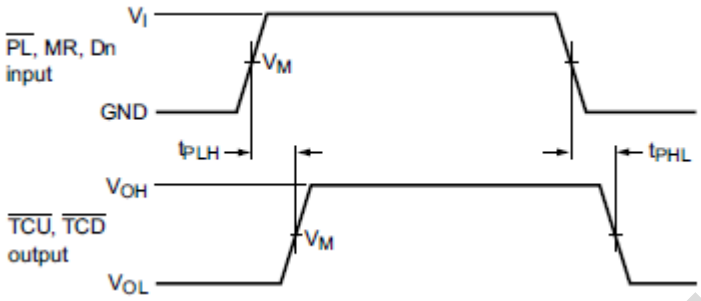



Figure 11. The data input (Dn), parallel load input ($\overline{PL}$) and the master reset input (MR) to the terminal count outputs ($\overline{TCU}$, $\overline{TCD}$) propagation delays

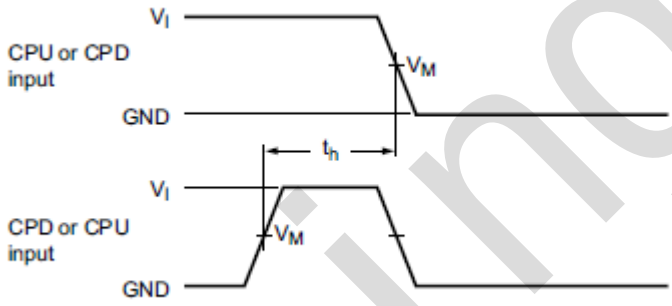



Figure 12. The CPU to CPD or CPD to CPU hold times

### 4.3、Measurement Points

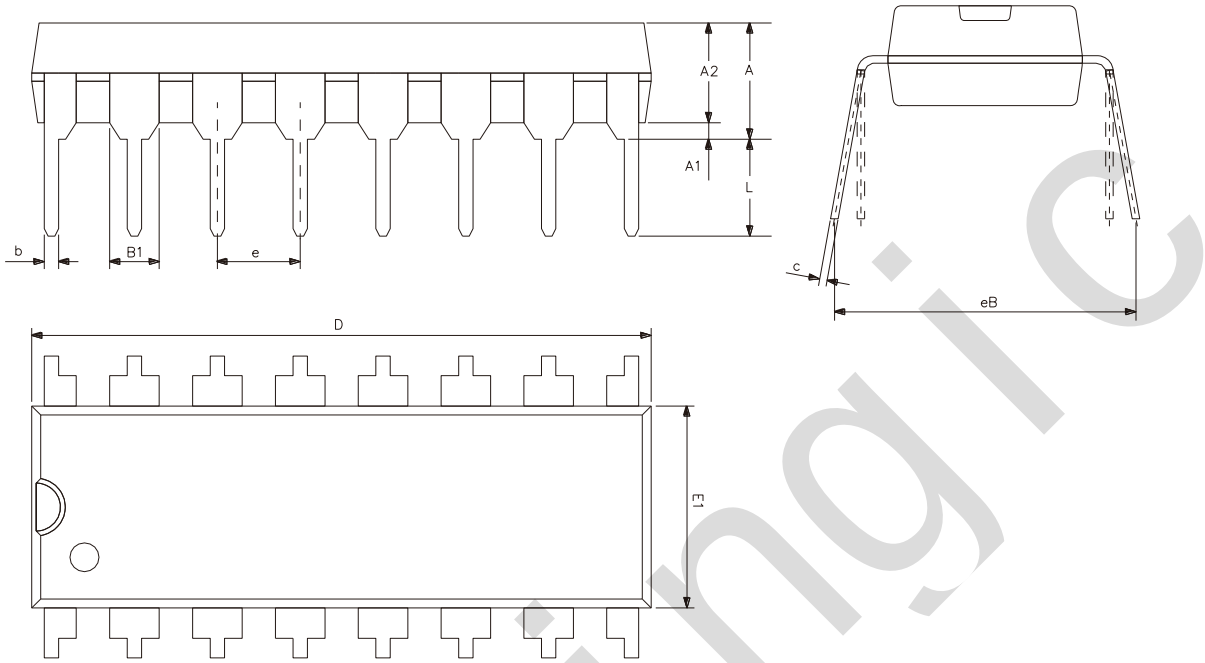
| Input | | Output |
|---|---|---|
| $V_I$ | $V_M$ | $V_M$ |
| GND to $V_{CC}$ | 0.5×$V_{CC}$ | 0.5×$V_{CC}$ |

### 4.4、Test Data

| Input | | Load | | S1 position |
|---|---|---|---|---|
| $V_I$ | $t_r$ , $t_f$ | $C_L$ | $R_L$ | $t_{PHL}$, $t_{PLH}$ |
| $V_{CC}$ | 6ns | 15pF, 50pF | 1kΩ | open |

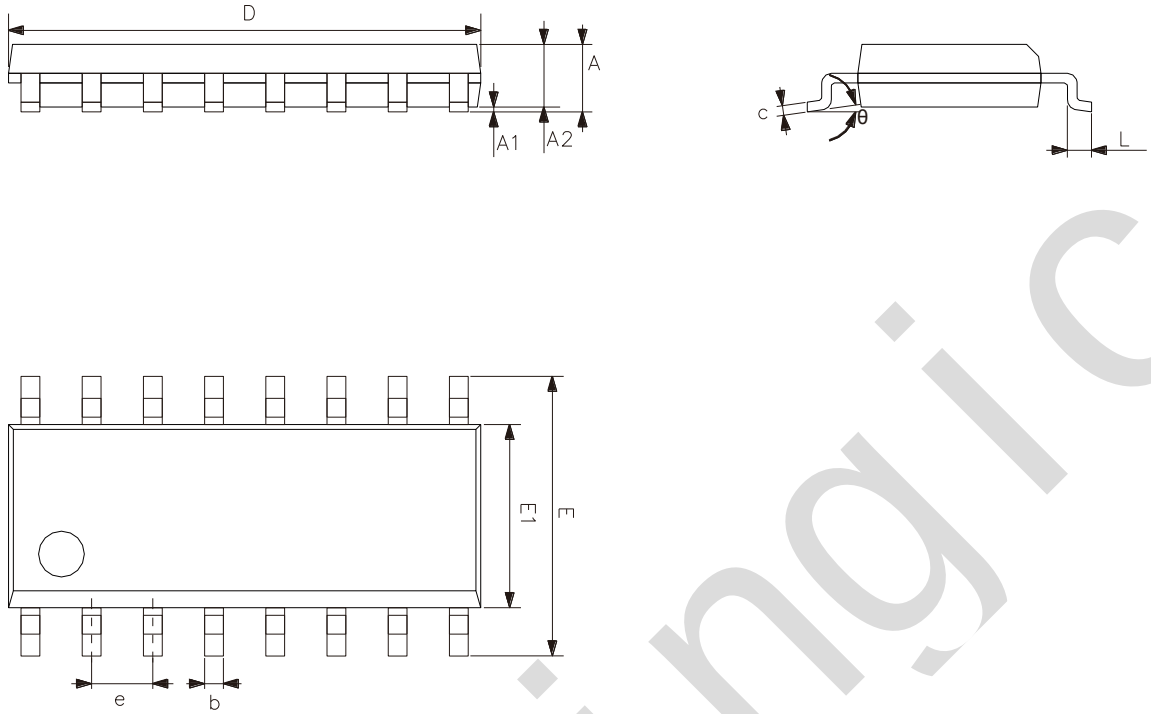
## 5、Package Information

### 5.1、DIP16



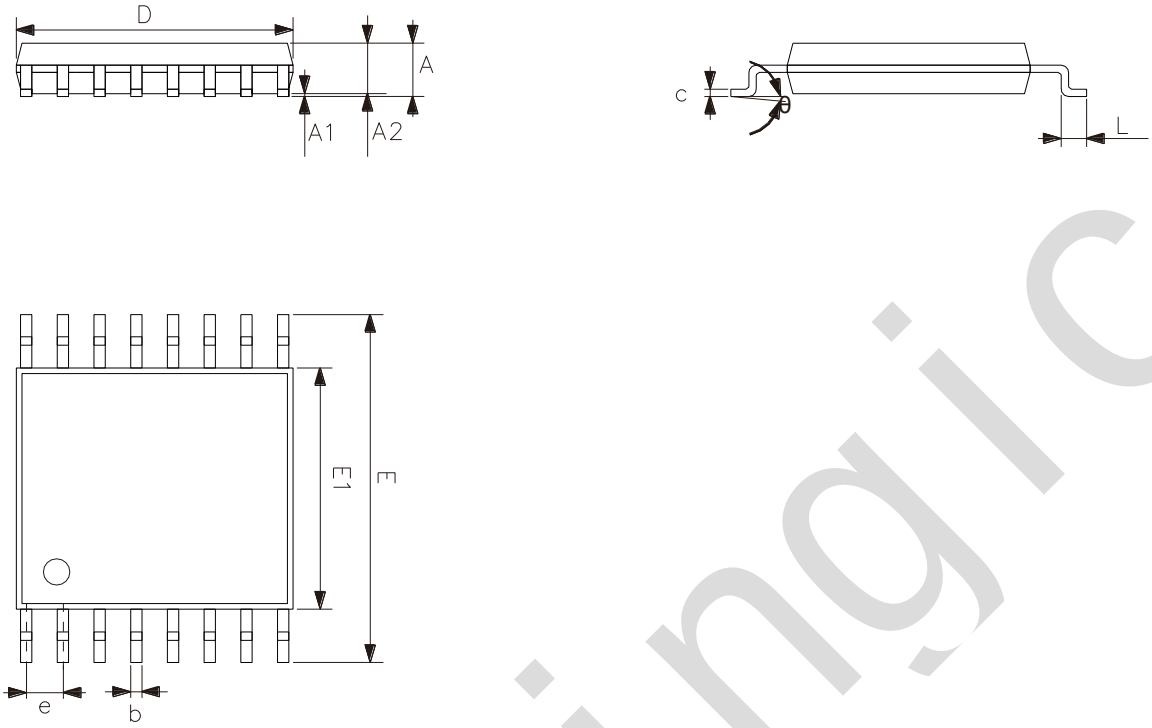

| Symbol | Dimensions (mm) | |
|---|---|---|
| | Min. | Max. |
| A2 | 3.20 | 3.60 |
| A1 | 0.51 | - |
| A | 3.60 | 5.33 |
| L | 3.00 | 3.60 |
| b | 0.36 | 0.56 |
| B1 | 1.52 | |
| D | 18.80 | 19.94 |
| E1 | 6.20 | 6.60 |
| e | 2.54 | |
| c | 0.20 | 0.36 |
| eB | 7.62 | 9.30 |

**5.2、SOP16**




| Symbol | Dimensions (mm) | |
|---|---|---|
| | Min. | Max. |
| A | 1.35 | 1.80 |
| A1 | 0.10 | 0.25 |
| A2 | 1.25 | 1.55 |
| b | 0.33 | 0.51 |
| c | 0.19 | 0.25 |
| D | 9.50 | 10.10 |
| E | 5.80 | 6.30 |
| E1 | 3.70 | 4.10 |
| e | 1.27 | |
| L | 0.35 | 0.89 |
| θ | 0° | 8° |

**5.3、TSSOP16**




| Symbol | Dimensions (mm) | |
|---|---|---|
| | Min. | Max. |
| A | - | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 4.90 | 5.10 |
| E1 | 4.30 | 4.50 |
| E | 6.20 | 6.60 |
| e | 0.65 | |
| L | 0.45 | 0.75 |
| θ | 0° | 8° |

# 6、Statements And Notes

## 6.1、The name and content of Hazardous substances or Elements in the product

| Part name | Hazardous substances or Elements | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Lead and lead compounds | Mercury and mercury compounds | Cadmium and cadmium compounds | Hexavalent chromium compounds | Polybrominated biphenyls | Polybrominated biphenyl ethers | Dibutyl phthalate | Butylbenzyl phthalate | Di-2-ethylhexyl phthalate | Diisobutyl phthalate |
| Lead frame | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| Plastic resin | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| Chip | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| The lead | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| Plastic sheet installed | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| explanation | ○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard.<br>×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements. | | | | | | | | | |

## 6.2、Notes

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