

## General Description

The LTA391/LTA2903/LTA2901 are single-, dual-, quad- channel comparators that feature 250  $\mu$  A quiescent current, a wide range of supply voltages from 2.0V to 36V with rail-to-rail inputs helps to implement in a wide variety of applications where require critical response time, power-sensitive, high-voltage. The output of the LTA391/LTA2903/LTA2901 could be connected to other open-collector outputs to achieve wired-AND relationship. All input and output pins can tolerate a continuous short-circuit fault condition to either rail.

The LTA391 (Single) is available in SOT23-5L package. The LTA2903 (Dual) is offered in TSSOP-8L, SOIC-8L, DFN 3\*3-8L and MSOP-8L packages, The LTA2901 (Quad) is offered in SOIC-14L, TSSOP-14L and DFN 3\*3-16L packages. All devices are rated over  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  extended industrial temperature range.

## Features and Benefits

- 2.0V to 36V Single supply or  $\pm 1.0\text{V}$  to  $\pm 18\text{V}$  Dual supply
- Low quiescent current: 250  $\mu$  A
- Common-mode input voltage range includes Ground
- Differential input voltage range equal to power supply
- $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  Operation temperature
- available in packages: SOT23-5L, SOIC-8L, TSSOP-8L, MSOP-8L, DFN-8L, SOIC-14L, TSSOP-14L, DFN-16L
- Output Compatible with TTL, MOS, CMOS logic levels

## Applications

- Industrial Application
- Solar Inverter
- White Goods
- Battery Management System
- Medical Equipment

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## Revision History

### **Version FN1623-49.2 (Jan,2024)**

- Remove "LTA331" in this version datasheet.Rename "LTA391U" for replacement.
- Add "LTA391R" in this version.
- Change supply voltage from minimum 2.5V to 2.0V.
- Update "Electrical Characteristics"
- Update "Typical Characteristics" Figure 4 and Figure 5.

### **Version FN1623-49.1 (Jan,2024)**

- Add ECO Class to "Order information"
- Add Specified Voltage to "Electrical Characteristics ---LTA2903"

### **Version FN1623-49.0 (Dec,2023)**

- Initial version.

### Ordering Information<sup>(1)</sup>

Part Number	Package Type	Quantity	ECO Class <sup>(2)</sup>	Mark Code <sup>(3)</sup>
LTA391JXT5/R6*	SOT23-5L	3 000	Green (RoHS & no Sb/Br)	G91
LTA391UXT5/R6*	SOT23-5L	3 000	Green (RoHS & no Sb/Br)	G31
LTA391RXT5/R6*	SOT23-5L	3 000	Green (RoHS & no Sb/Br)	G9R
LTA2903XS8/R8	SOIC-8L	4 000	Green (RoHS & no Sb/Br)	G2903
LTA2903XV8/R6	MSOP-8L	3 000	Green (RoHS & no Sb/Br)	G2903
LTA2903XT8/R6	TSSOP-8L	3 000	Green (RoHS & no Sb/Br)	G2903
LTA2903XF8/R6*	DFN3*3-8L	3 000	Green (RoHS & no Sb/Br)	G2903
LTA2901XS14/R5*	SOIC-14L	2 500	Green (RoHS & no Sb/Br)	G2901
LTA2901XT14/R6*	TSSOP-14L	3 000	Green (RoHS & no Sb/Br)	G2901
LTA2901XF16/R6*	DFN3x3-16L	3 000	Green (RoHS & no Sb/Br)	G2901

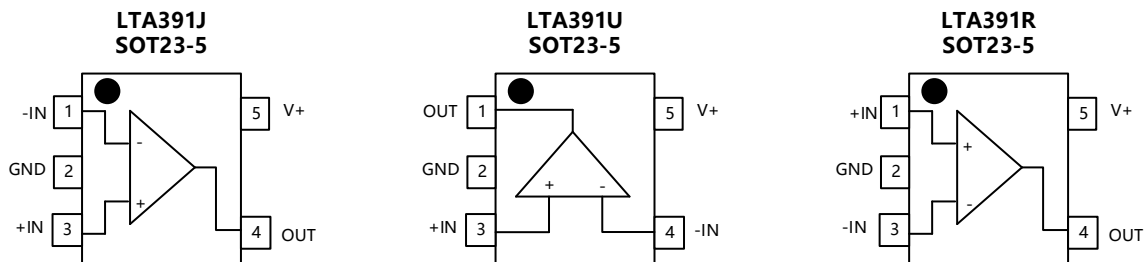
\* Preview Status (Not for MP stage, pls contact with us if you have request)

(1) Please contact to your Linearin representative for the latest availability information and product content details.

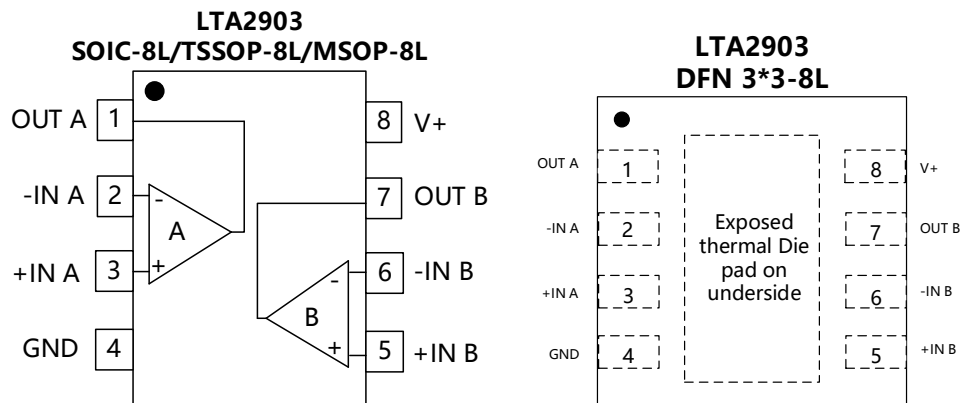
(2) Eco Class - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & Halogen Free).

(3) There may be multiple device markings, a varied marking character of "x", or additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

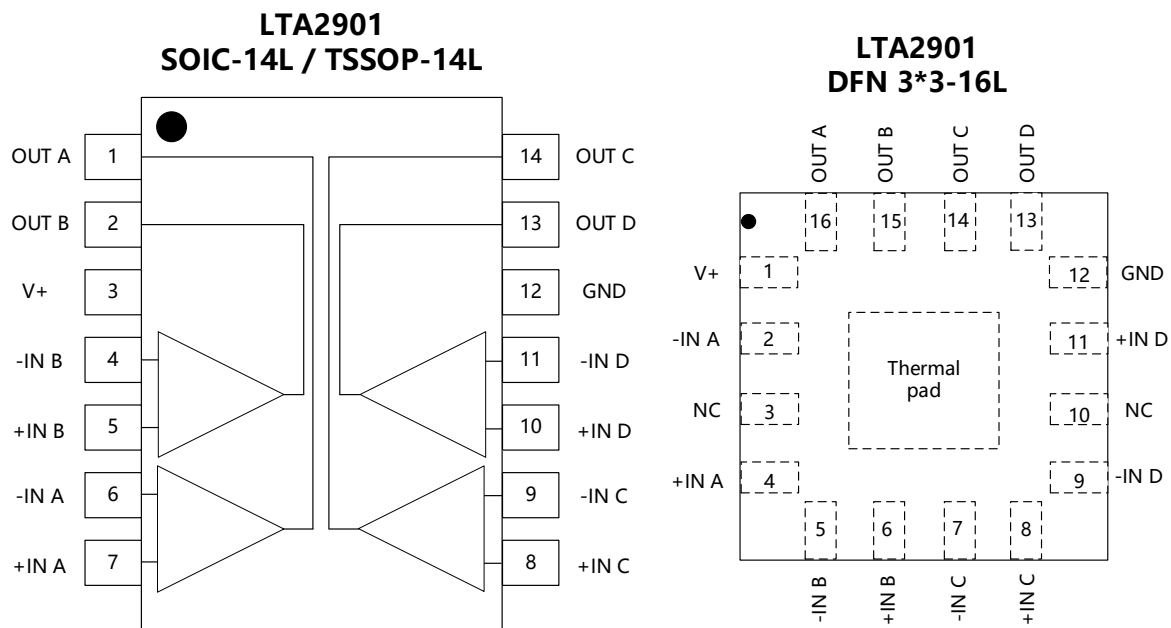
### Pin Configuration (Top View)



Symbol	LTA391J	LTA391U	LTA391R	Description
	SOT23-5L			
-IN	1	4	3	Inverting input
+IN	3	3	1	Non-inverting input
OUT	4	1	4	Output
GND	2	2	2	Ground
V+	5	5	5	Positive power supply



Symbol	LTA2903		Description
	SOIC-8L/MSOP8/TSSOP-8/DFN-8L		
-IN A	2		Inverting input, channel A
+IN A	3		Non-inverting input, channel A
-IN B	6		Inverting input, channel B
+IN B	5		Non-inverting input, channel B
OUT A	1		Output, channel A
OUT B	7		Output, channel B
GND	4		Ground
V+	8		Positive power supply



Symbol	LTA2901		Description
	SOIC-14L / TSSOP-14L	DFN 3*3-16L	
-IN A	6	2	Inverting input, channel A
+IN A	7	4	Non-inverting input, channel A
OUT A	1	16	Output, channel A
GND	12	12	Ground
-IN B	4	5	Inverting input, channel B
+IN B	5	6	Non-inverting input, channel B
OUT B	2	15	Output, channel B
V+	3	1	Positive power supply
-IN C	9	7	Inverting input, channel C
+IN C	8	8	Non-inverting input, channel C
OUT C	14	14	Output, channel C
NC	-	3, 10	No internal connection
-IN D	11	9	Inverting input, channel D
+IN D	10	11	Non-inverting input, channel D
OUT D	13	13	Output, channel D

### Limiting Value– In accordance with the Absolute Maximum Rating System (IEC 60134)

Parameter	Absolute Maximum Rating
Supply Voltage, $V_{S+}$ to $V_{S-}$	36 V
Differential input voltage	$\pm 36$ V
Input voltage range (either input)	-0.3 to 38 V
Input current	-50 mA
Output voltage	36 V
Output current	20 mA
Storage Temperature Range, $T_{sta}$	-65 °C to +150 °C
Junction Temperature, $T_j$	150 °C
Lead Temperature Range (Soldering 10 sec)	260 °C

### ESD Ratings

Parameter	Level	UNIT
Human body model (HBM), per ESDA/JEDEC JS-001-2017 <sup>(1)</sup>	$\pm 1500$	V
Charged device model (CDM), per ESDA/JEDEC JS-002-2018 <sup>(2)</sup>	$\pm 750$	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible if necessary precautions are taken.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible if necessary precautions are taken.

### Thermal Information

Thermal Metric		Package	Unit
$\theta_{JA}$	Thermal Resistance	SOT23-5L	190
		SOIC-8L	125
		TSSOP-8L	160
		MSOP-8L	201
		DFN 3*3-8L	94
		SOIC-14L	115
		TSSOP-14L	112
		DFN 3*3-16L	65

## Electrical Characteristics -- LTA2903

At  $T_A = 25^\circ\text{C}$  and  $V_S = 5\text{ V}$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<i>OFFSET VOLTAGE</i>						
Input offset voltage	$V_{OS}$	$V_{IC} = V_{ICR} \text{ min, } V_O = 1.4\text{ V, } V_{CC} = 5\text{ V to } V_{CC} \text{ MAX, } T_A = 25^\circ\text{C}$		1		mV
		$V_{IC} = V_{ICR} \text{ min, } V_O = 1.4\text{ V, } V_{CC} = 5\text{ V to } V_{CC} \text{ MAX, } T_A = -40 \text{ to } +125^\circ\text{C}$		2		
<i>INPUT BIAS CURRENT</i>						
Input bias current	$I_B$	$I_{IN(+)} - I_{IN(-)}$ with Output in Linear range $V_{CM} = 0\text{ V}^{(1)}$		22		nA
Input offset current	$I_{OS}$	$I_{IN(+)} - I_{IN(-)}$ $V_{CM} = 0\text{ V}$		1		nA
<i>INPUT VOLTAGE</i>						
Common-mode voltage range	$V_{CM}$	$V_{CC} = 30\text{ V}^{(2)}$	-0.3		$V_{CC} - 1.4$	V
<i>OPEN-LOOP GAIN</i>						
Large-signal differential-voltage amplification	$A_{VD}$	$V_{CC} = 15\text{ V, } V_O = 1.4\text{ V to } 11.4\text{ V, } R_L \geq 15\text{ k}\Omega \text{ to } V_{CC}, T_A = 25^\circ\text{C}$		25	100	V/mV
<i>OUTPUT</i>						
Low output voltage swing	$V_{OL}$	$V_{ID} = -1\text{ V, } I_{OL} = 4\text{ mA}$		152	370	mV
High-level output current	$I_{OH}$	$V_{ID} = 1\text{ V, } V_{OH} = 5\text{ V}$		0.1		nA
Low-level output current	$I_{OL}$	$V_{ID} = -1\text{ V, } V_{OL} = 1.5\text{ V}$	6	16		mA
<i>POWER SUPPLY</i>						
Specified Voltage	$V_S$		2.0		36	V
Supply current(one comparator)	$I_{CC}$	$V_O = 2.5\text{ V, No load } V_{CC} = 5\text{ V}$		0.23	0.5	mA
		$V_O = 2.5\text{ V, No load, } V_{CC} = \text{MAX}$		0.28	0.63	

At  $T_A = 25^\circ\text{C}$  and  $V_S = 5\text{ V}$ , unless otherwise noted.

Parameter	Symbol	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay time	$T_{pd}$	$V_{RL} = 5\text{ V, } R_L = 5.1\text{ k}\Omega$		1.4		$\mu\text{s}$
		$V_{IN} = \text{TTL Logic Swing, } V_{REF} = 1.4\text{ V}$		330		ns

(1) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

(2) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is  $V_{CC} - 1.5\text{ V}$  at  $25^\circ\text{C}$ , but either or both inputs can go to 36 V without damage, independent of the magnitude of  $V_{CC}$ .

## Typical Characteristics -- LTA2903

At  $T_A = +25\text{ }^\circ\text{C}$ ,  $V_{CM} = V_S/2$ , and  $R_L = 10\text{ k}\Omega$  connected to  $V_S/2$ , unless otherwise noted.

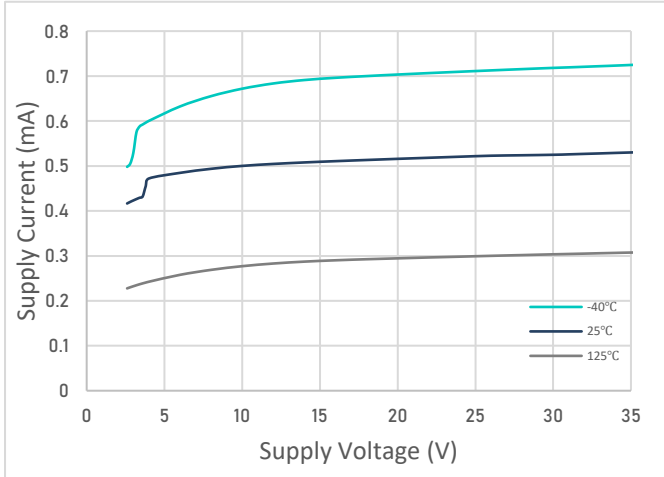


Figure 1. Supply Current vs Supply Voltage

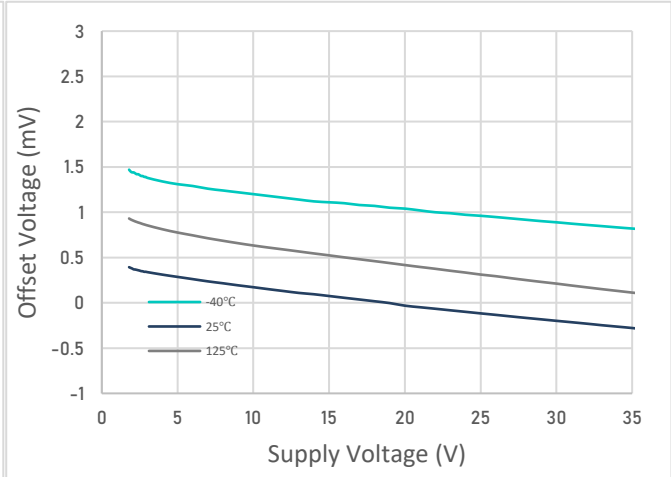


Figure 2. Offset voltage vs Supply Voltage

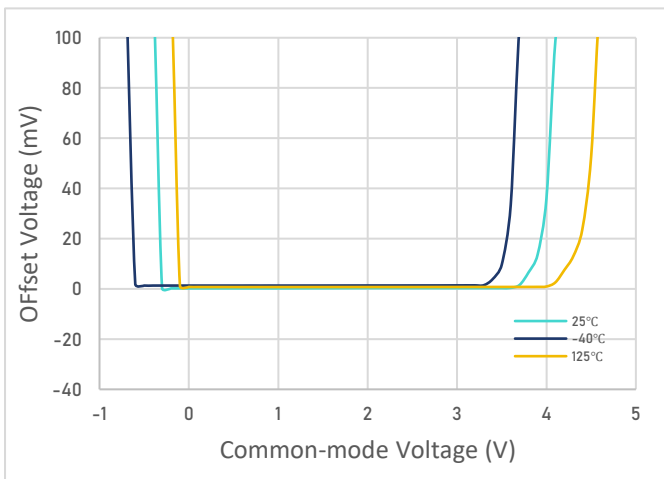


Figure 3. Offset voltage vs Common-mode Voltage

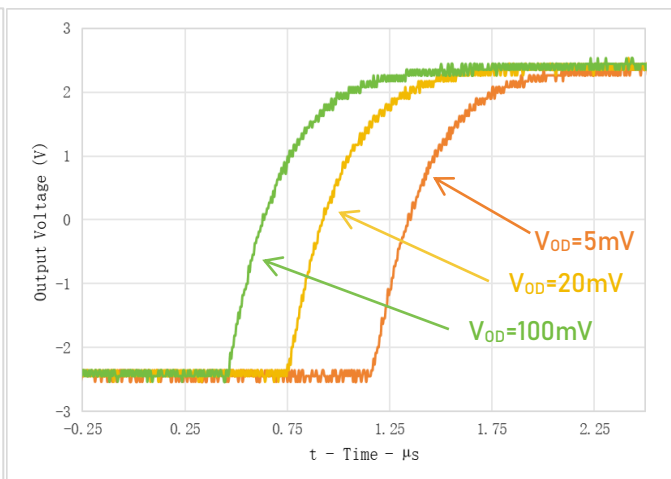


Figure 4. Propagation Delay Falling Edge

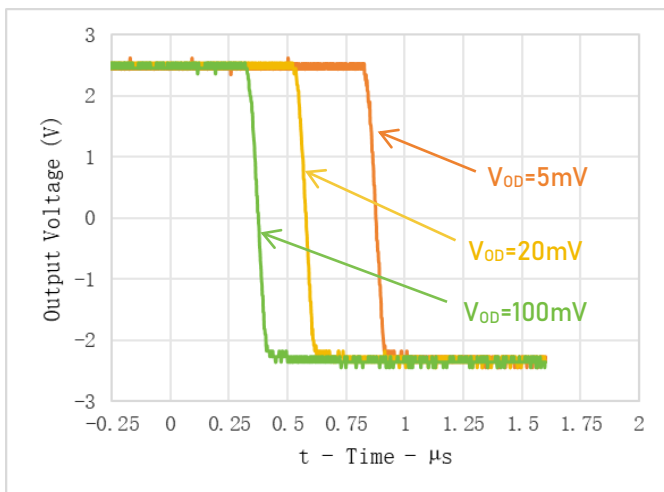


Figure 5. Propagation Delay Rising Edge



## Detailed Description

### Operating Voltage

The LTA391 / LTA2903 / LTA2901 family of 36V General-purpose low power comparators is fully specified and ensured for operation from 2.0 to 36V and offers an excellent speed-to-power combination with propagation delay of 1 $\mu$ s and a quiescent supply current of 250  $\mu$ A. The open-drain output allows the user to configure the output logic low voltage ( $V_{OL}$ ) and allows the comparator to be used in AND functionality.

In addition, and many specifications apply over the industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , parameters that vary significantly with operating voltages or temperature are illustrated in the Typical Characteristics graphs.

### Maximizing performance through proper layout

To achieve the maximum performance of the extremely high input impedance and low offset voltage of the LTA391 / LTA2903 / LTA2901 devices, care is needed in laying out the circuit board. The PCB surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the comparator inputs further reduces leakage currents. Figure 6 shows proper guard ring configuration and the top view of a surface-mount layout. The guard ring does not need to be a specific width, but it should form a continuous loop around both input. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PCB using Teflon standoff insulators.

Other potential sources of offset error are thermo-electric voltages on the circuit board. This voltage, also called Seebeck voltage, occurs at the junction of two dissimilar metals and is proportional to the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-component lead. If the temperature of the PCB at one end of the component is different from the temperature at the other end, the resulting Seebeck voltages are not equal, resulting in a thermal voltage error.

This thermocouple error can be reduced by using dummy components to match the thermoelectric error source. Placing the dummy component as close as possible to its partner ensures both Seebeck voltages are equal, thus canceling the thermocouple error. Maintaining a constant ambient temperature on the circuit board further reduces this error. The use of a ground plane helps distribute heat throughout the board and reduces EMI noise pickup.

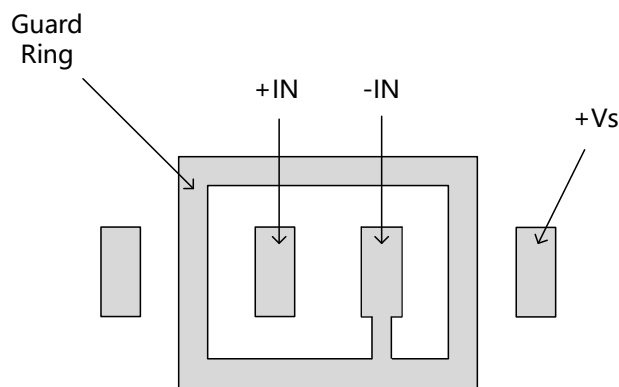


Figure 6: Use a guard ring around sensitive pins

## Input and Output coupling

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

## Typical Application Circuits

### Window Comparator

Window Comparators are commonly used to detect undervoltage (UV) and overvoltage (OV) conditions. Figure 7 shows a simple window comparator circuit.

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 12 V
- Alert (logic low output) when an input signal is greater than 24 V
- Alert signal is active low
- Operate from a 36 V power supply

Configure the circuit as shown in Figure 7. Connect  $V_{S+}$  to a 36 V power supply and  $V_{S-}$  to ground. Make R1, R2 and R3 each 10Mohm resistors. These three resistors are used to create the positive and negative thresholds for the window comparator ( $V_{TH+}$  and  $V_{TH-}$ ). With each resistor being equal,  $V_{TH+}$  is 24 V and  $V_{TH-}$  is 12 V. Large resistor values such as 10Mohm are used to minimize power consumption. The sensor output voltage is applied to the inverting and non-inverting inputs of the 2-channel LTA2903's. The respective comparator outputs will be low when the sensor is less than 12V or greater than 24 V.  $V_{OUT}$  will be high when the sensor is in the range of 12 V to 24 V. See the application curve in Figure 8.

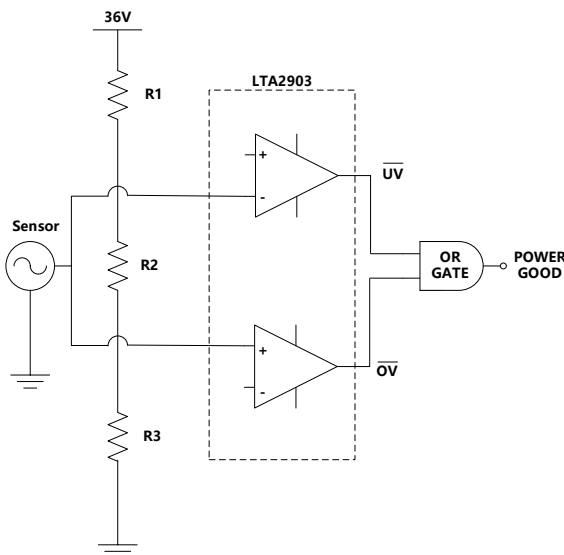


Figure 7: Window Comparator

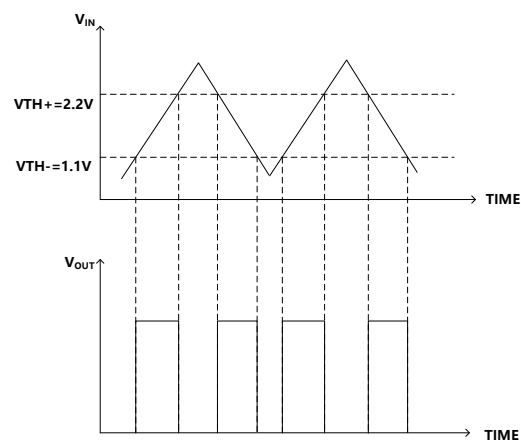
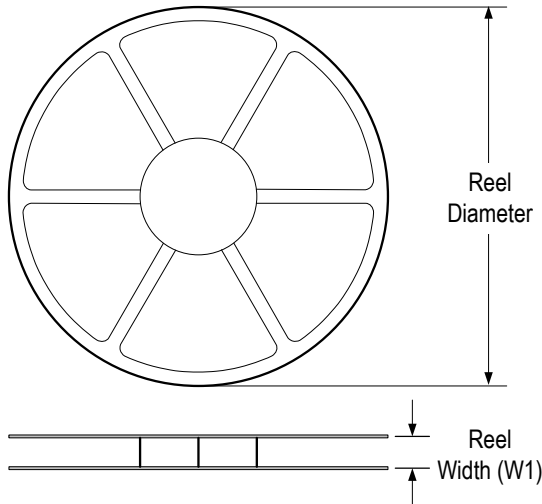


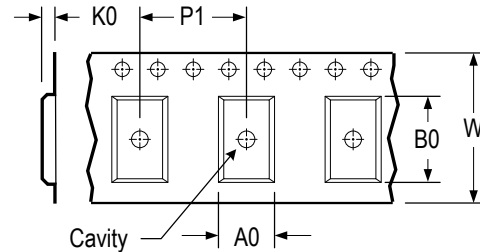
Figure 8: Window Comparator Results

## Tape and Reel Information

### REEL DIMENSIONS

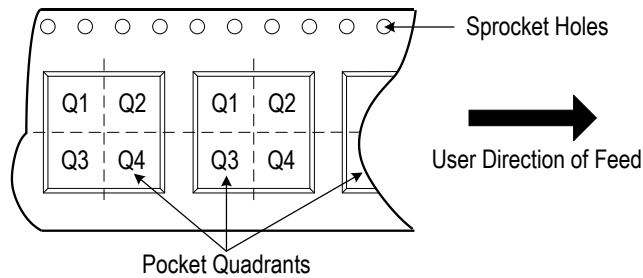


### TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

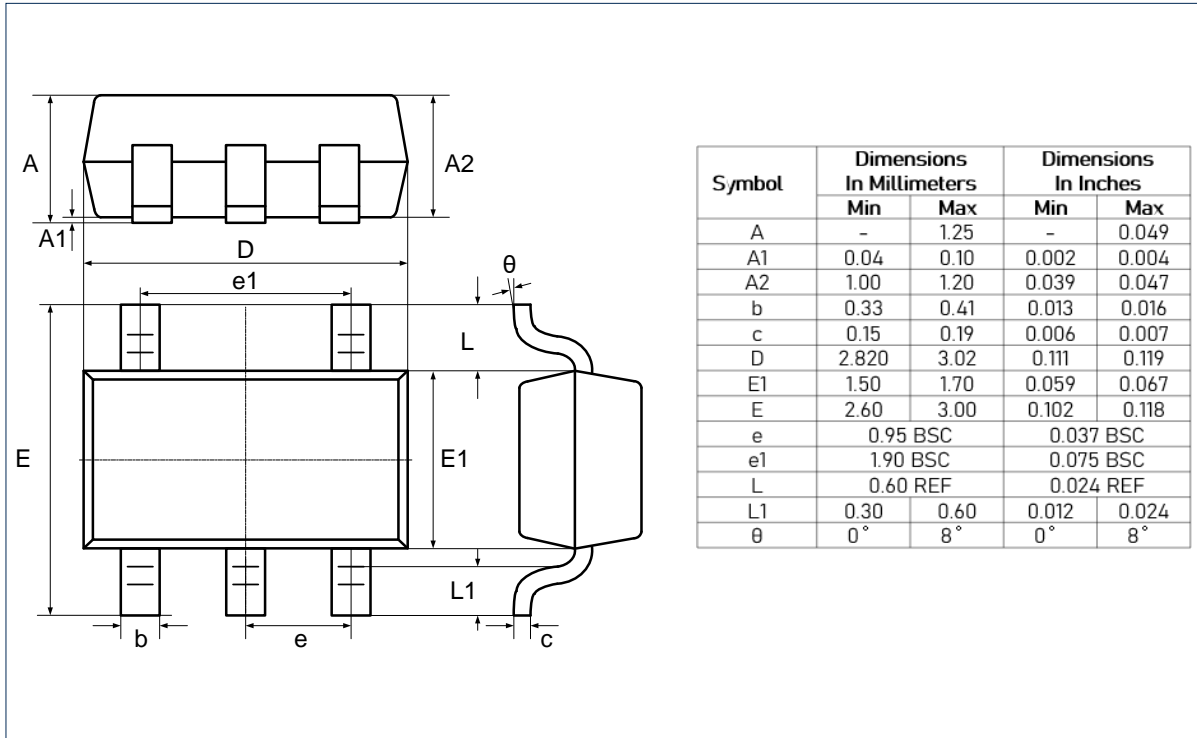


\* All dimensions are nominal

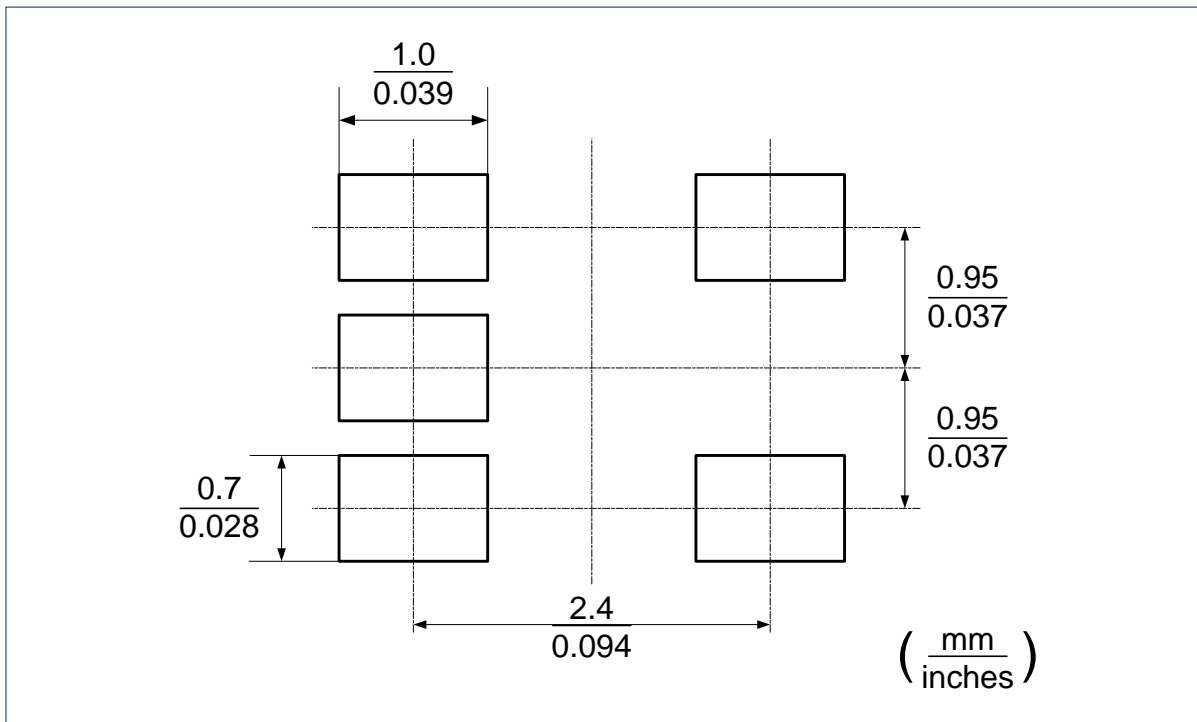
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTA391JXT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3
LTA391UXT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3
LTA391RXT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3
LTA2903XS8/R8	SOIC	8	4 000	330	12.4	6.6	5.3	2.0	8.0	12.0	Q1
LTA2903XV8/R6	MSOP	8	3 000	330	12.4	5.0	3.5	2.0	8.0	12.0	Q1
LTA2903XT8/R6	TSSOP	8	3 000	330	16	8.5	7	2.0	8	1.2	Q1
LTA2903XF8/R6	DFN	8	3 000	330	16	8.5	7	2.0	8	1.2	Q1
LTA2901XS14/R5	SOIC	14	2 500	330	18	8.5	1.1	2.0	8.5	1.6	Q1
LTA2901XT14/R6	TSSOP	14	3 000	330	18	8.5	1.1	2.0	8.5	1.6	Q1
LTA2901XF16/R6	DFN	16	3 000	330	18	8.5	1.1	2.0	8.5	1.6	Q1

Package Outlines

DIMENSIONS, SOT23-5L

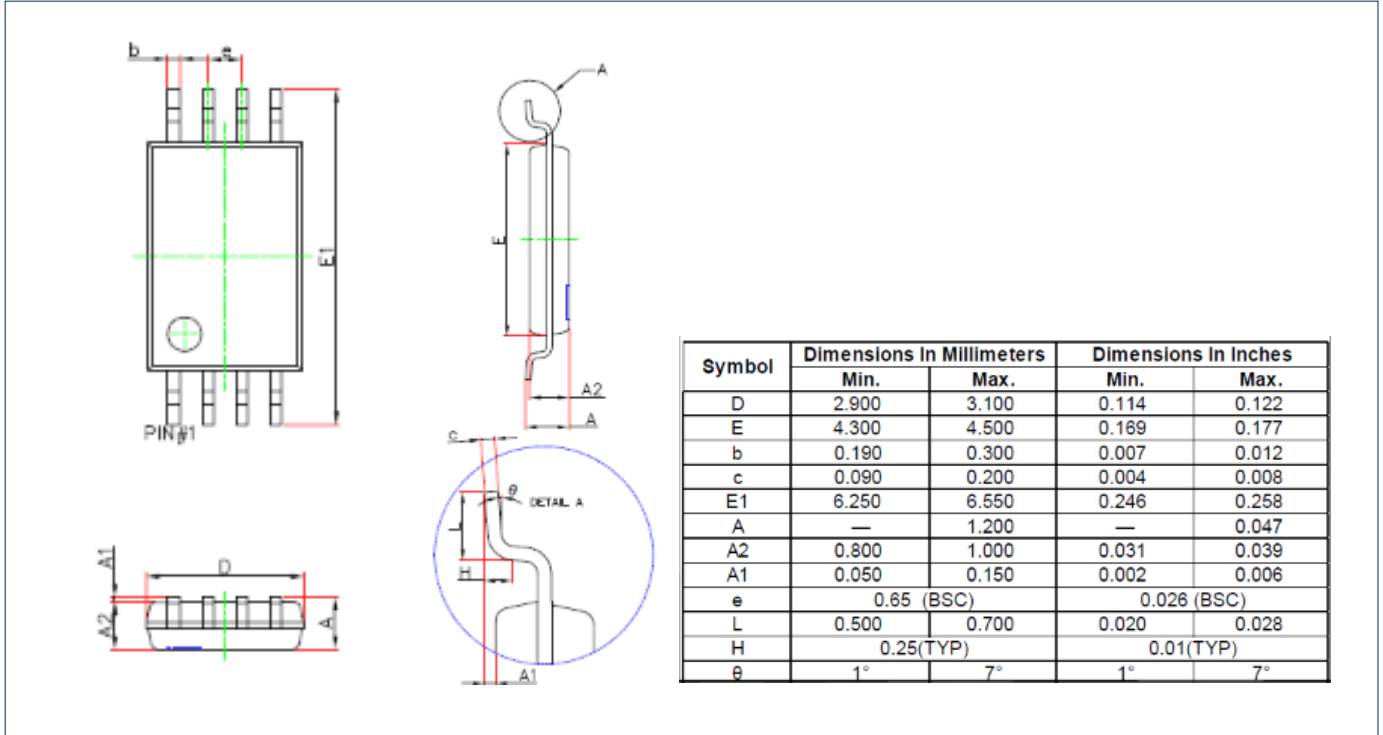


RECOMMENDED SOLDERING FOOTPRINT, SOT23-5L

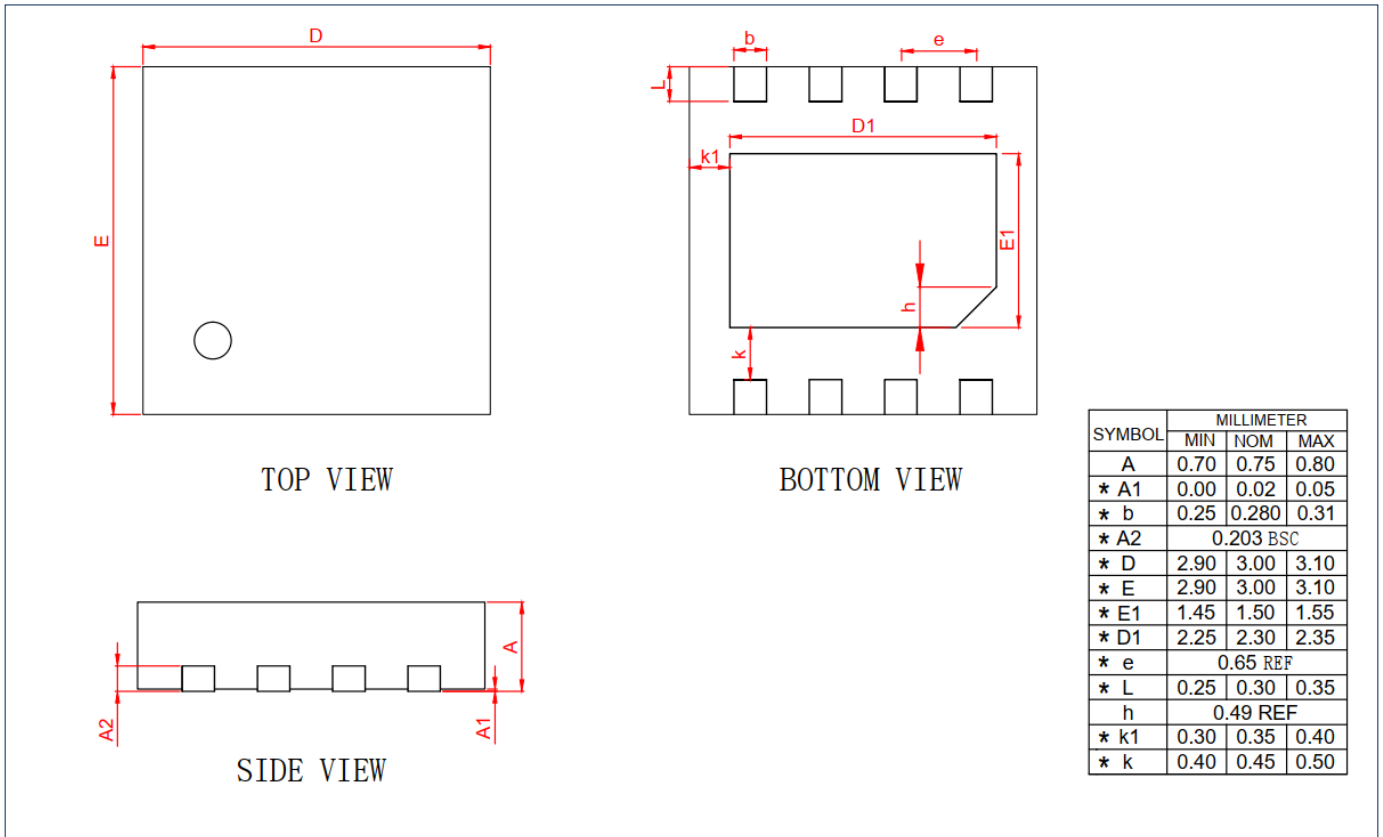


Package Outlines (Continued)

DIMENSIONS, TSSOP-8L

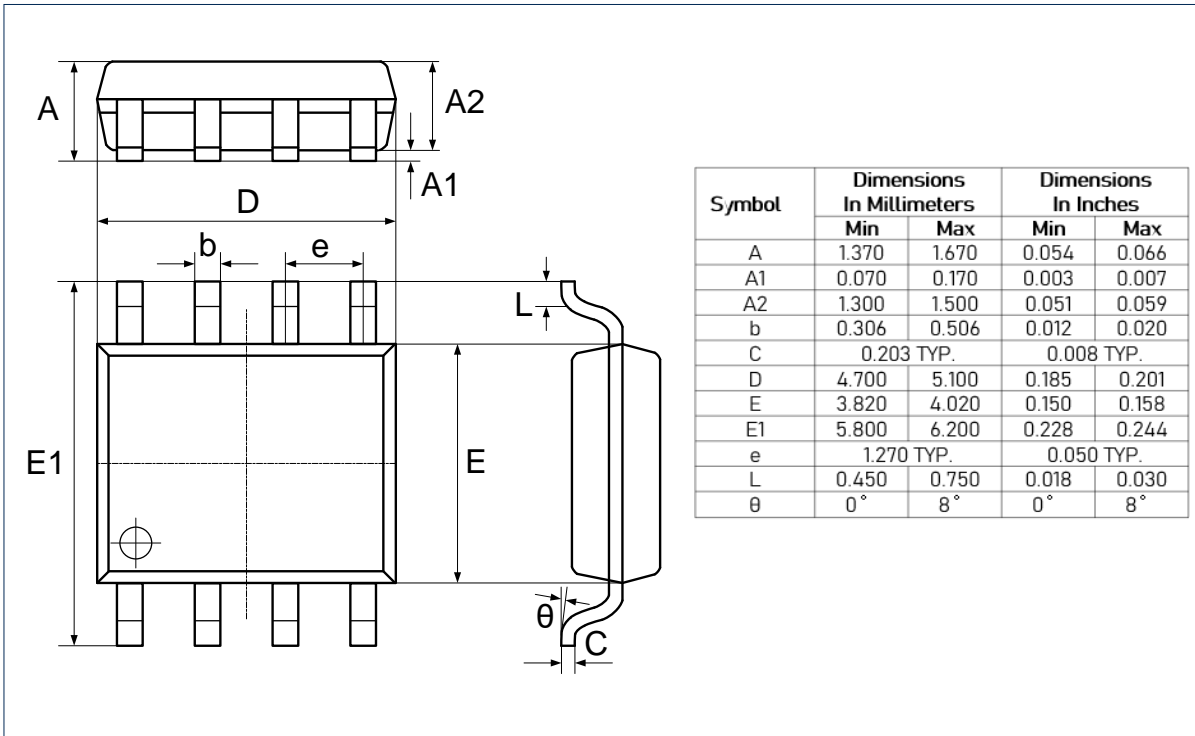


DIMENSIONS, DFN 3\*3-8L

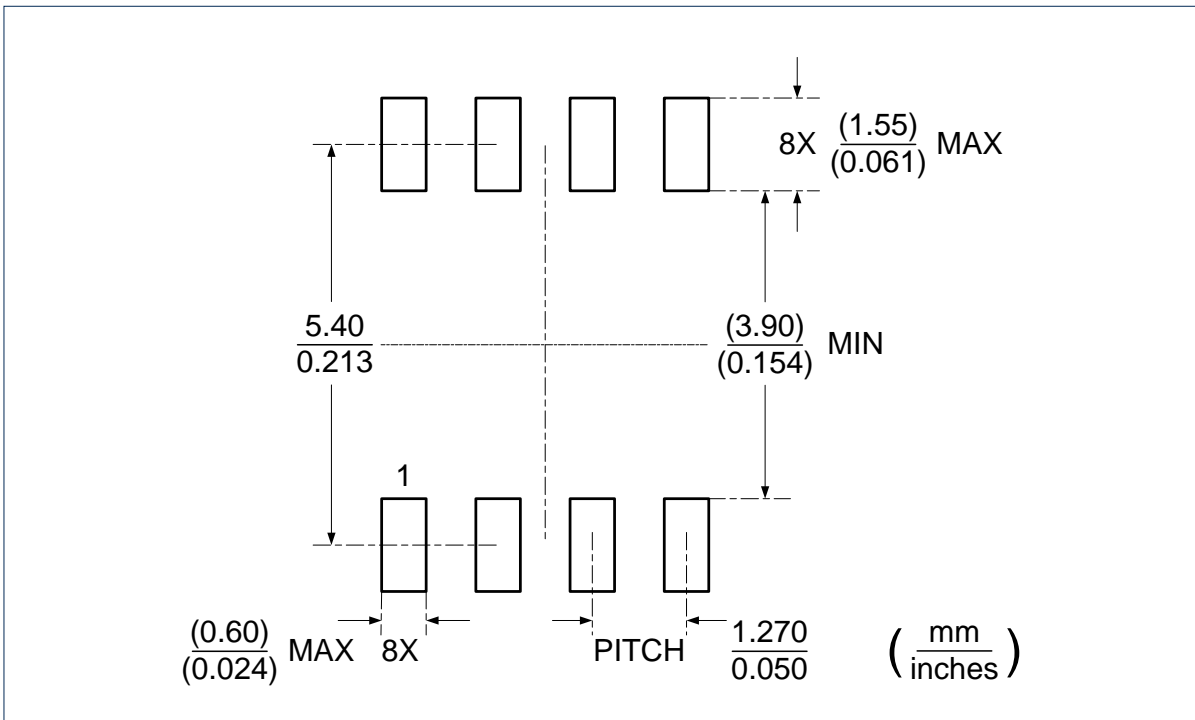


Package Outlines (Continued)

DIMENSIONS, SOIC-8L

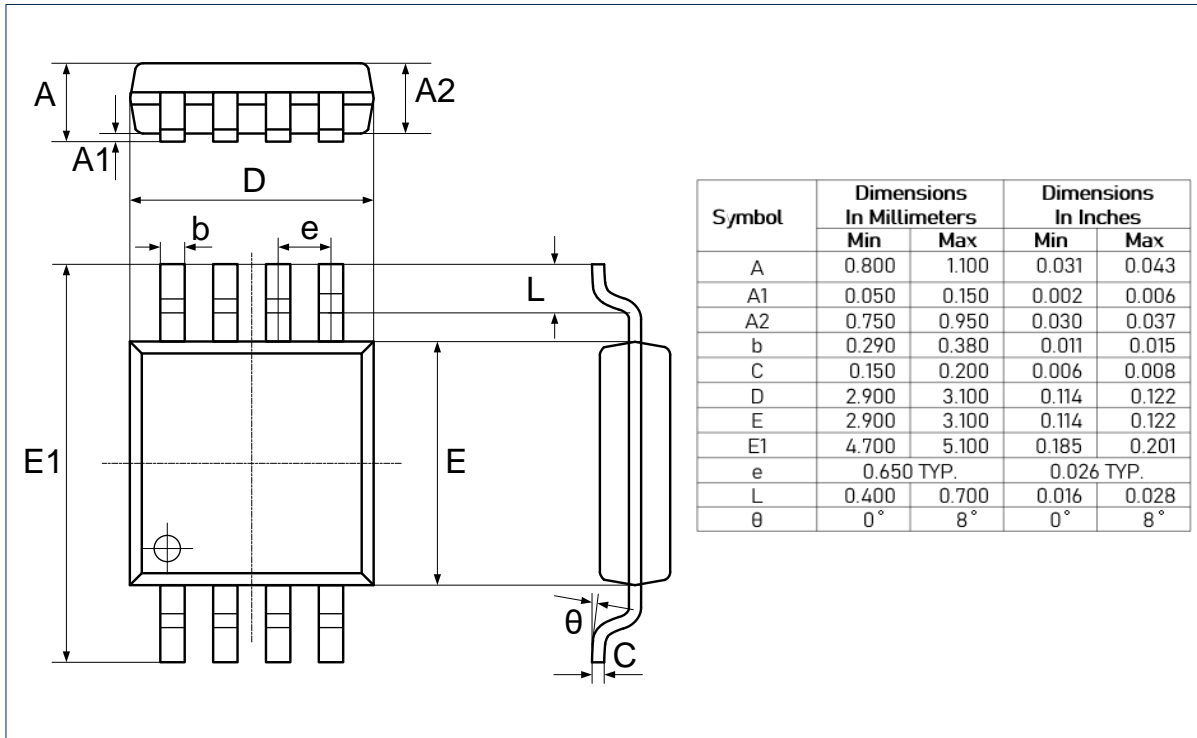


RECOMMENDED SOLDERING FOOTPRINT, SOIC-8L

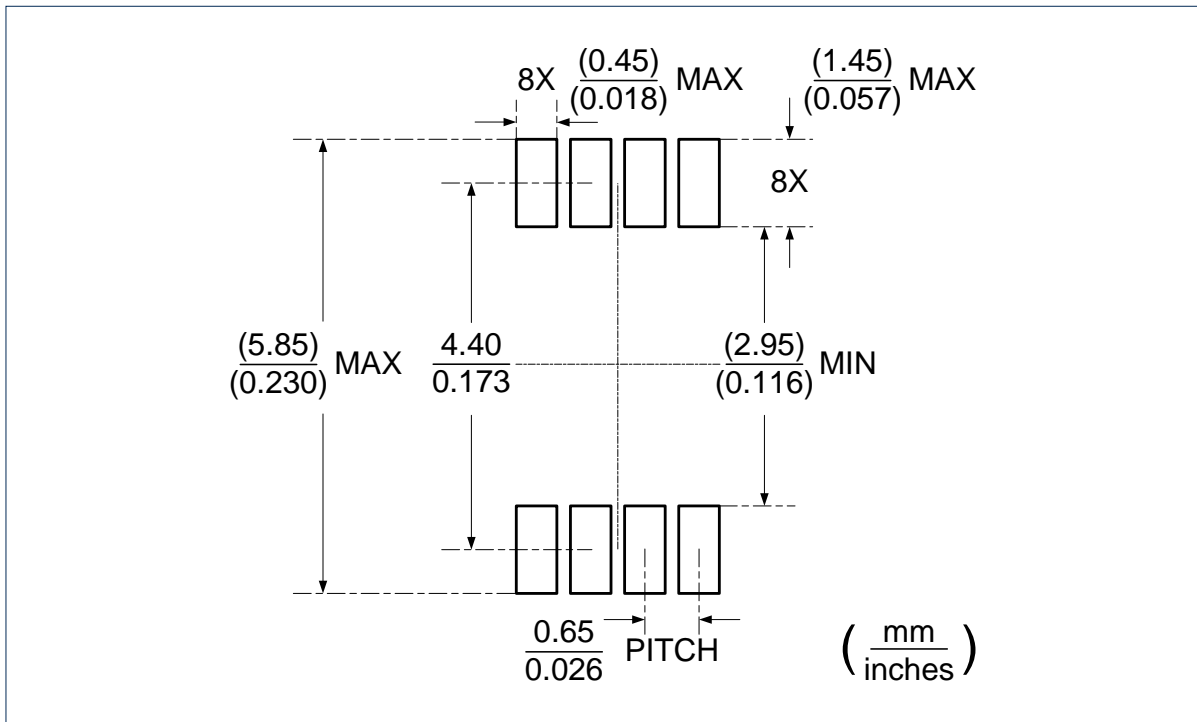


Package Outlines (Continued)

DIMENSIONS, MSOP-8L

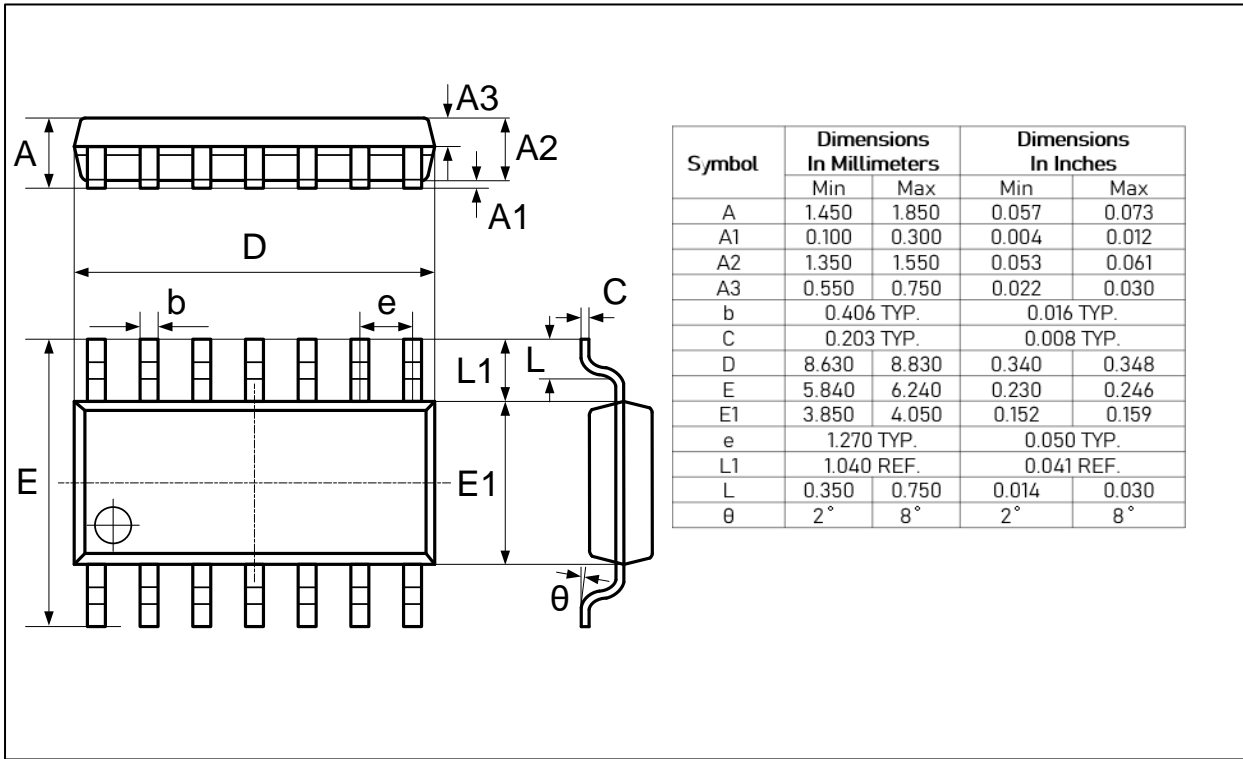


RECOMMENDED SOLDERING FOOTPRINT, MSOP-8L

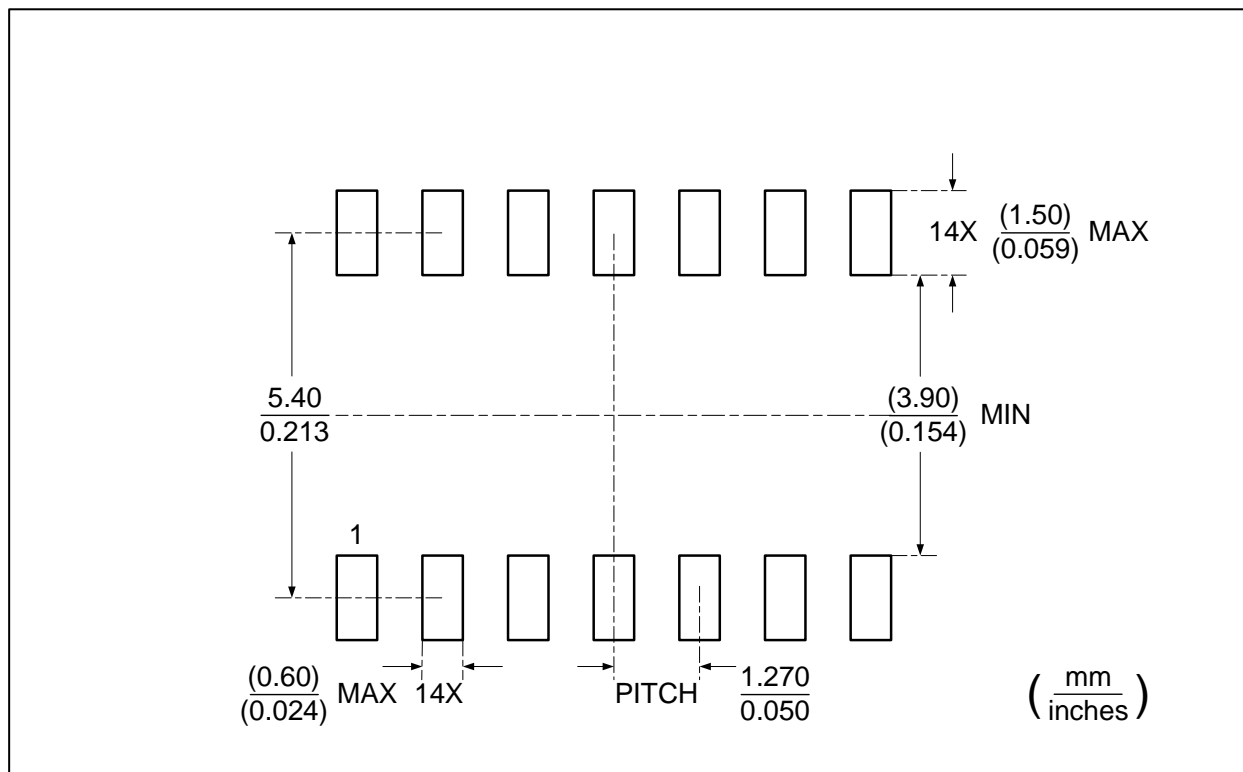


Package Outlines (Continued)

DIMENSIONS, SOIC-14L



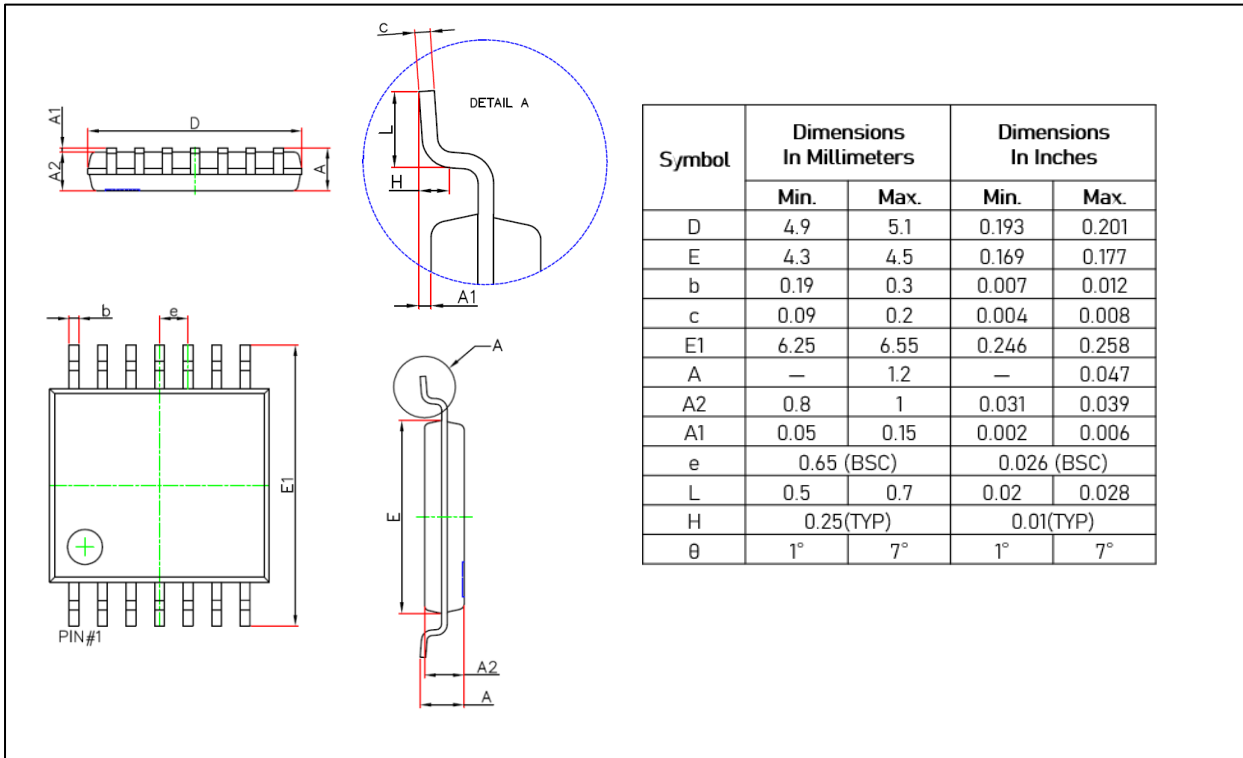
RECOMMENDED SOLDERING FOOTPRINT, SOIC-14L



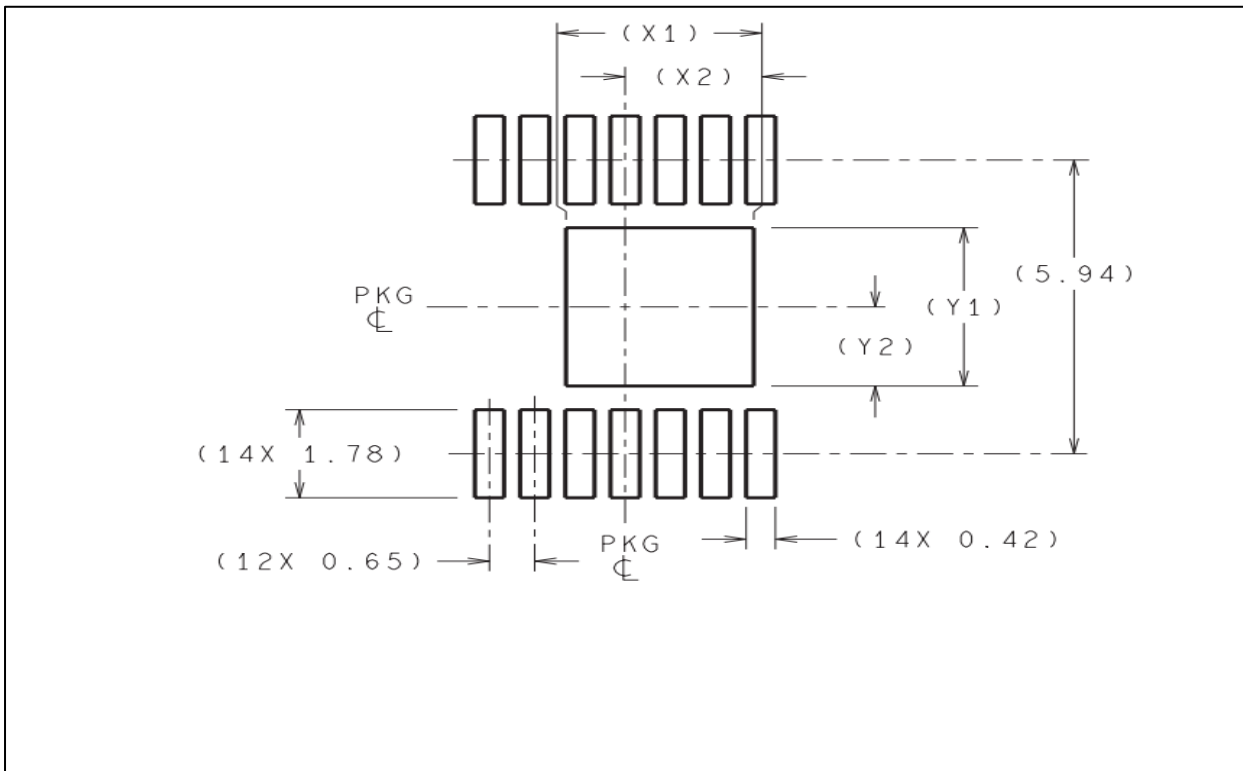


Package Outlines (Continued)

DIMENSIONS, TSSOP-14L

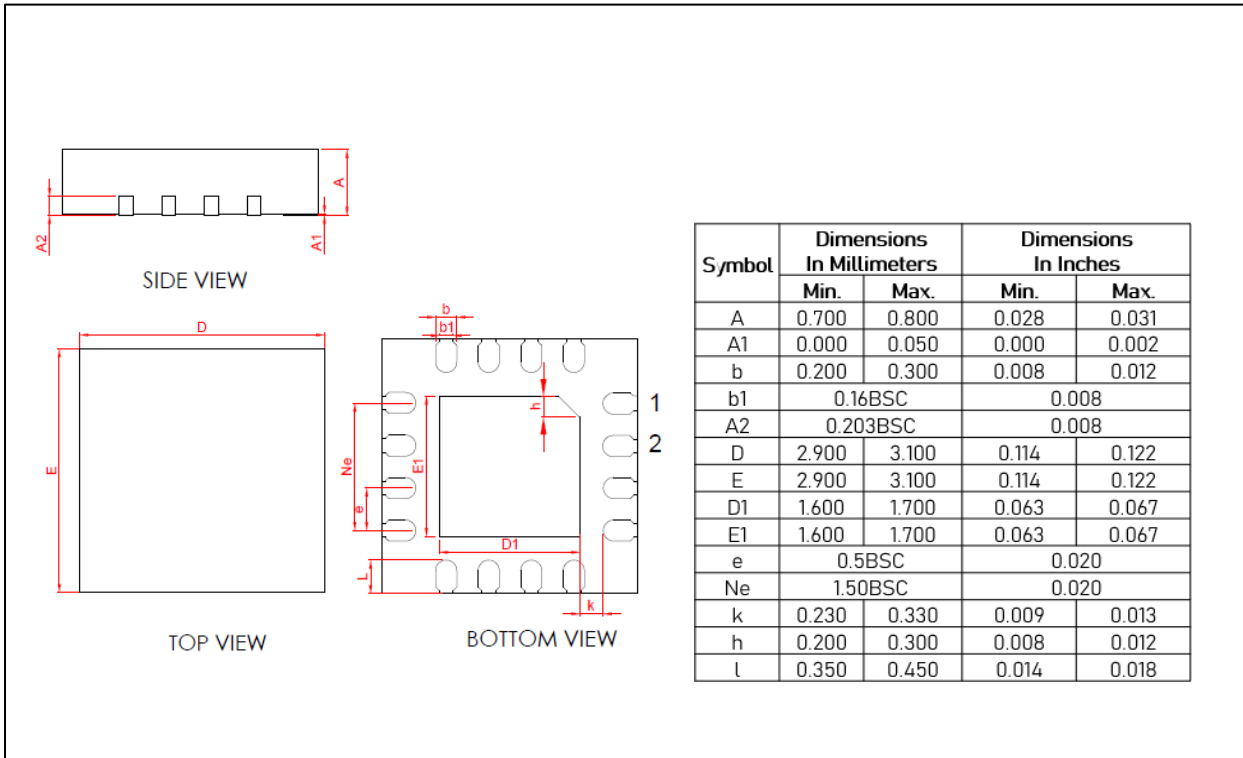


RECOMMENDED SOLDERING FOOTPRINT, TSSOP-14L

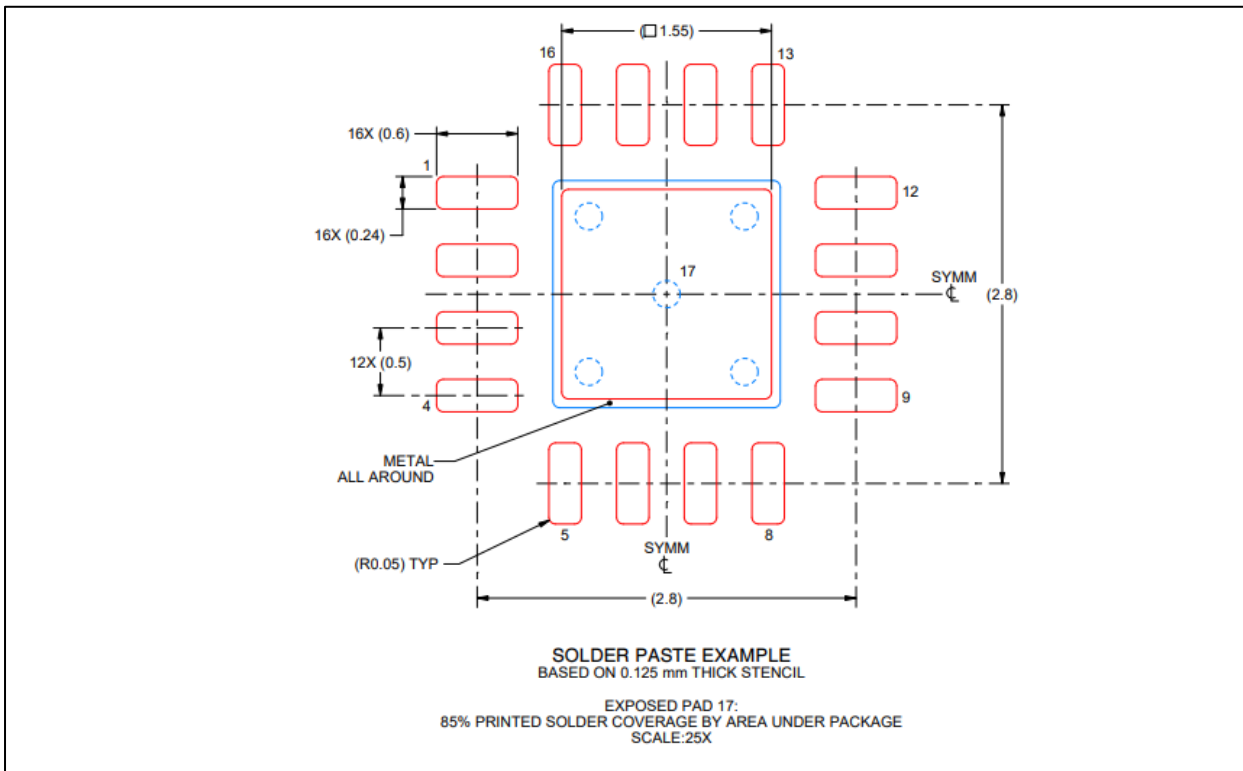


Package Outlines (Continued)

DIMENSIONS, DFN 3\*3-16L



RECOMMENDED SOLDERING FOOTPRINT, DFN 3\*3-16L



## Important Notice

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