

N-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

Surface-mounted package
Super Trench
 $T_j \text{ max } 175^\circ$
Advanced trench cell design
MSL1

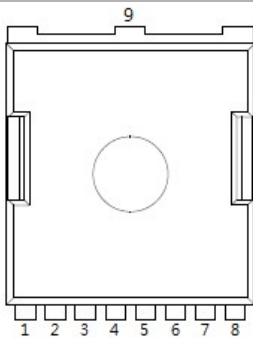
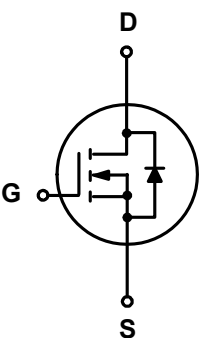
1.2 Applications

Power Tool appliances
BMS appliances
High power inverter system

1.3 Quick reference

$BV \geq 150 \text{ V}$
 $P_{\text{tot}} \leq 500 \text{ W}$
 $I_D \leq 220 \text{ A}$
 $R_{\text{DS(ON)}} \leq 5.0 \text{ m}\Omega @ V_{\text{GS}} = 10 \text{ V}$
 $R_{\text{DS(ON)}} \leq 6.0 \text{ m}\Omega @ V_{\text{GS}} = 6 \text{ V}$

2. Pin Description

Pin	Description	Simplified Outline	Symbol
1	Gate(G)	 Top View TOLL	
2,3,4,5,6,7,8	Source(S)		
9	Drain(D)		

3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	Drain-Source Voltage	T _C = 25 °C	150	-	V
V _{GS}	Gate-Source Voltage	T _C = 25 °C	-	±25	V
I _D *	Drain Current (DC)	T _C = 25 °C, V _{GS} = 10 V	-	220	A
		T _C = 100 °C, V _{GS} = 10 V	-	120	A
I _{DM} *	Drain Current (Pulsed)	T _C = 25 °C, V _{GS} = 10 V	-	680	A
P _{tot}	Drain power dissipation	T _C = 25 °C	-	500	W
T _{stg}	Storage Temperature		-55	175	°C
T _J	Junction Temperature		-	175	°C
I _S	Continuous-Source Current	T _C = 25 °C	-	220	A
I _{AS}	Single Pulsed Avalanche Current	V _{DD} =100V , L=0.05mH	-	160	A
E _{AS}	Single Pulsed Avalanche Energy	V _{DD} =100V , L=1.0mH	-	1250	mJ
R _{θJA} **	Thermal Resistance- Junction to Ambient		-	32.8	°C/W
R _{θJC} **			-	0.4	

Notes :

* Pulse width ≤ 300 μs, duty cycle ≤ 2 %

** Surface Mounted on minimum footprint pad area.

*** Limited by bonding wire

4. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
AOTL66518	TOLL-8L			2000	

5. Electrical Characteristics ($T_A=25^\circ$ Unless Otherwise Noted)

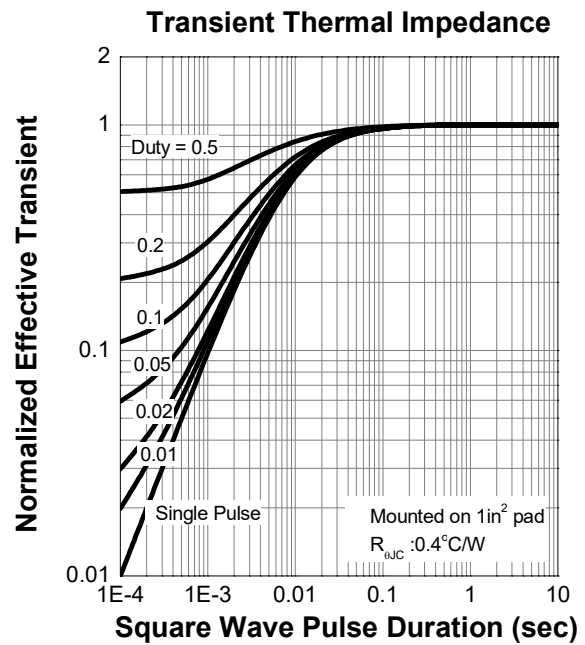
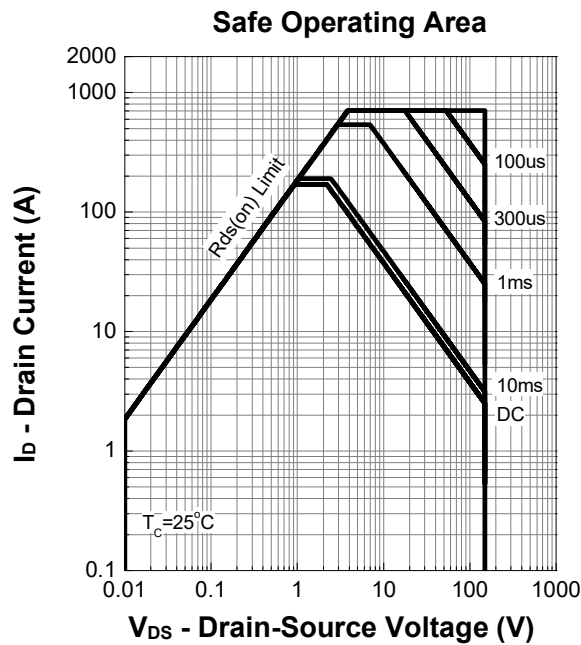
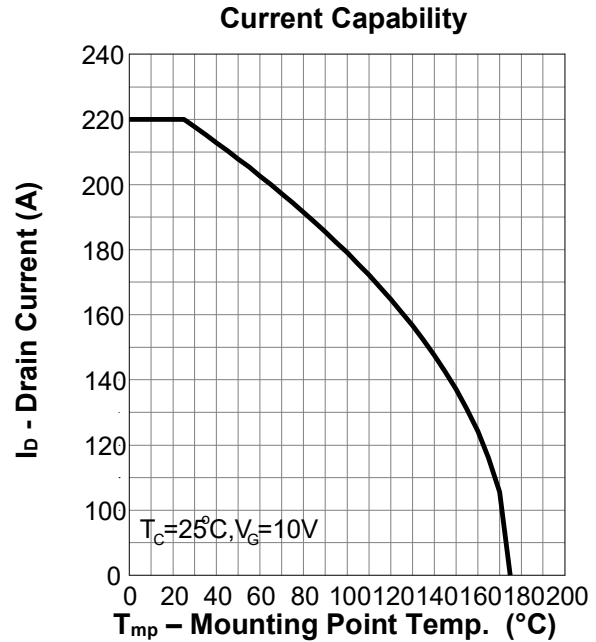
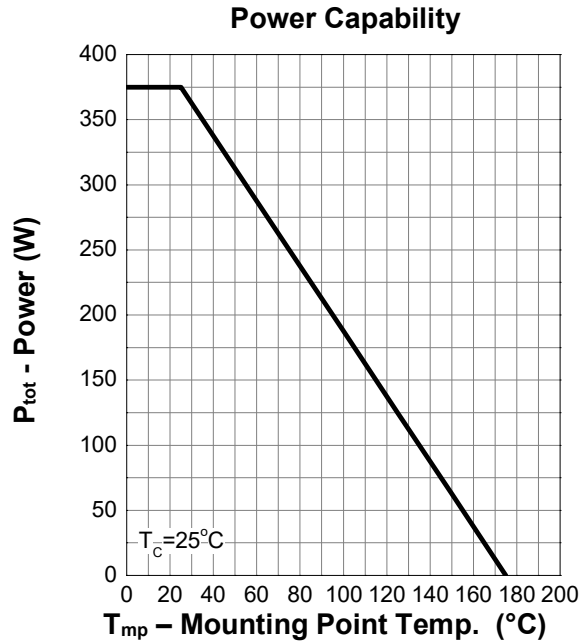
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _{DS} = 250 μA	150	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = 250 μA	2	-	4	V
I _{DSS}	Drain Leakage Current	V _{DS} = 120 V, V _{GS} = 0 V	-	-	1	μA
I _{GSS}	Gate Leakage Current	V _{GS} = 0 V, V _{GS} = ± 25 V	-	-	±100	nA
R _{DS(ON)} ^a	On-State Resistance	V _{GS} = 10 V, I _{DS} = 50 A	-	4.5	5.0	m Ω
		V _{GS} = 6 V, I _{DS} = 25 A	-	5.0	6.0	
Diode Characteristics						
V _{SD} ^a	Diode Forward Voltage	I _{SD} = 50 A, V _{GS} = 0 V	-	-	1.3	V
t _{rr}	Reverse Recovery Time	I _{DS} = 50 A, V _{GS} = 0 V di _{SD} /dt = 100 A/μs	-	115	-	nS
Q _{rr}	Reverse Recovery Charge		-	480	-	nC
Dynamic Characteristics ^b						
C _{iss}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 75 V Frequency = 1 MHz	-	9320	-	pF
C _{oss}	Output Capacitance		-	570	-	
C _{rss}	Reverse Transfer Capacitance		-	60	-	
t _{d(on)}	Turn-on Delay Time	V _{DS} = 75 V, V _{GEN} = 10 V, R _G = 3.9 Ω, R _L = 1.5 Ω, I _{DS} = 50 A	-	24	-	nS
t _r	Turn-on Rise Time		-	70	-	
t _{d(off)}	Turn-off Delay Time		-	112	-	
t _f	Turn-off Fall Time		-	75	-	
Gate Charge Characteristics ^b						
Q _g	Total Gate Charge	V _{DS} = 75 V, V _{GS} = 10 V, I _{DS} = 50 A	-	158	-	nC
Q _{gs}	Gate-Source Charge		-	48	-	
Q _{gd}	Gate-Drain Charge		-	39	-	

Notes :

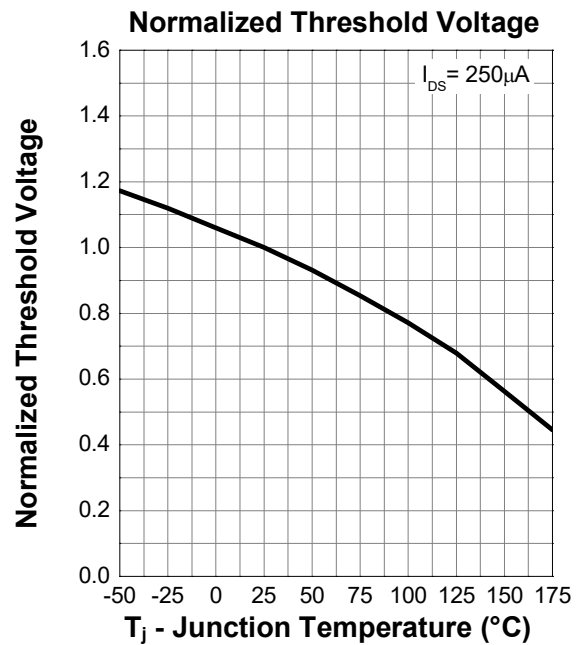
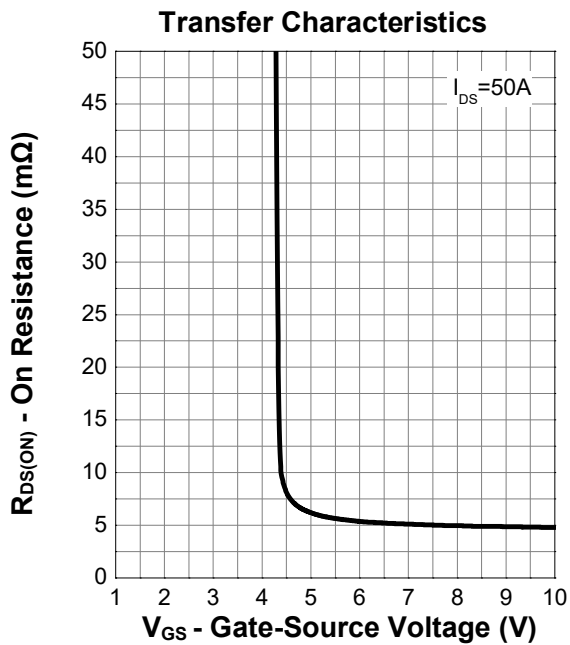
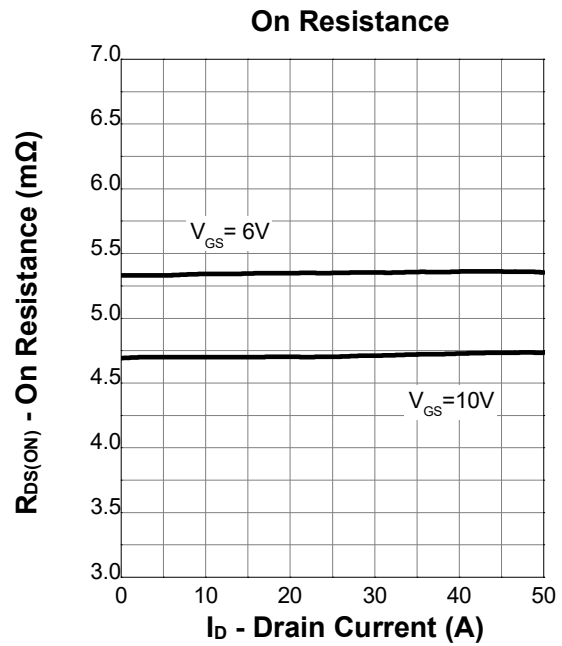
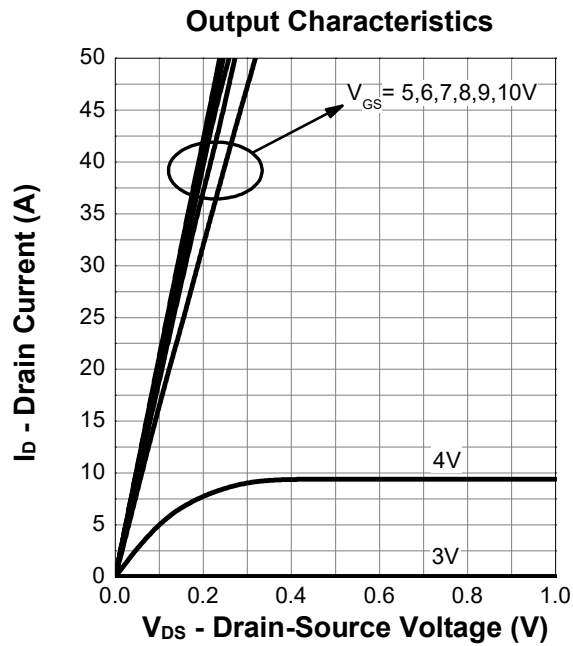
a : Pulse test ; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

b : Guaranteed by design, not subject to production testing

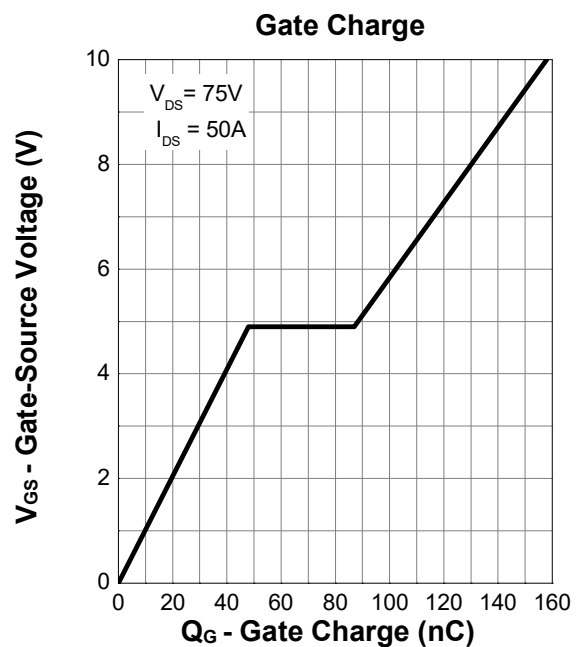
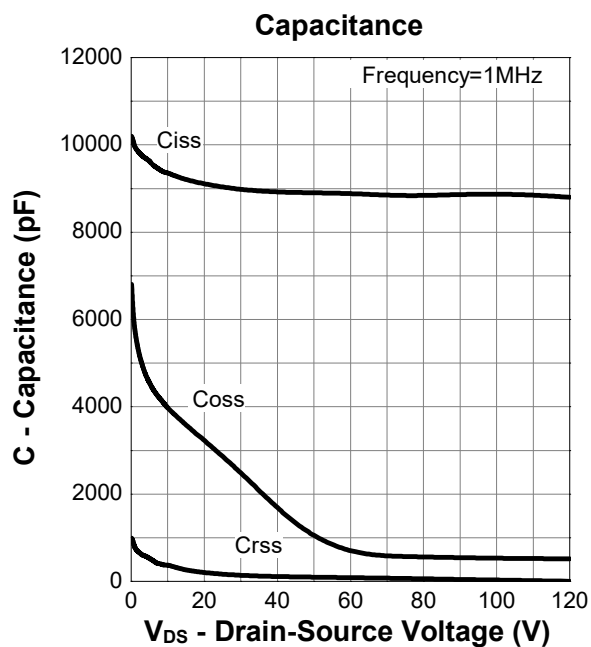
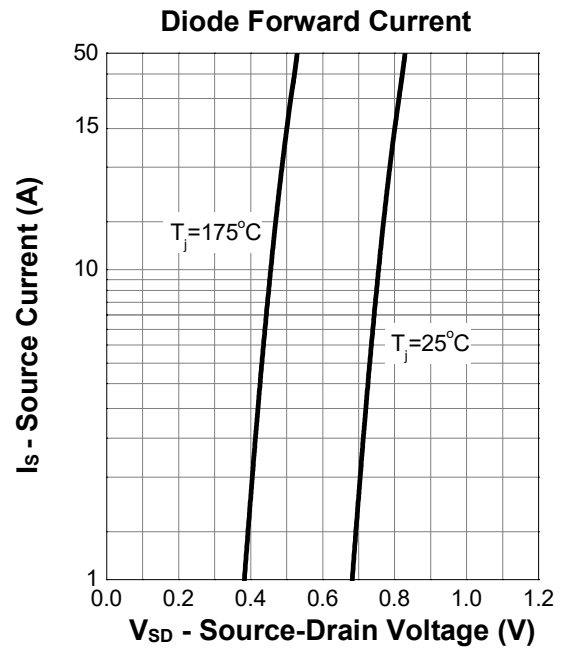
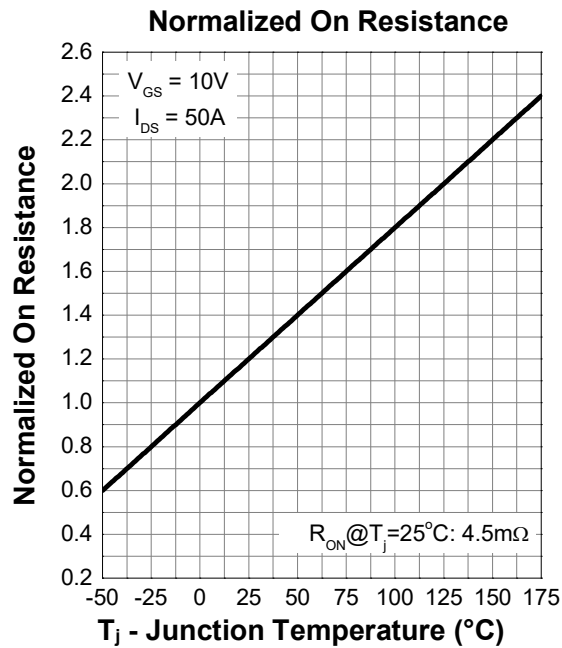
6. Typical Characteristics



7. Typical Characteristics (cont.)

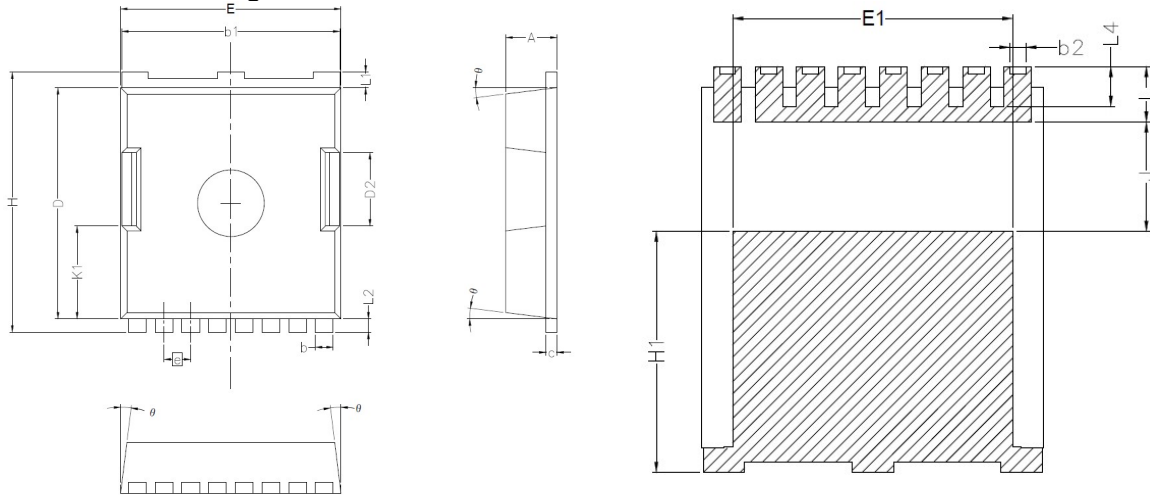


8. Typical Characteristics (cont.)



9. Package Dimensions

TOLL-8L Package



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.42	0.50
c	0.40	0.60
D	10.28	10.58
D2	3.10	3.50
E	9.70	10.10
E1	7.90	8.30
e	1.20BSC	
H	11.48	11.88
H1	6.75	7.15
N	8	
J	3.00	3.30
K1	3.98	4.38
L	1.40	1.80
L1	0.60	0.80
L2	0.50	0.70
L4	1.00	1.30
θ	4°	10°