SN74HC/HCT194 (LX)
4-bit Bidirectional Universal Shift Register

Product Specification

Specification Revision History：

Version	Date	Description
2023-05-A1	2023-05	New

Contents

1、General Description

The SN74HC/HCT194 is a 4-bit bidirectional universal shift register.

Features:

- Supply voltage range:
  SN74HC194: 2V to 6V
  SN74HCT194: 4.5V to 5.5V
- Input levels:
  SN74HC194: CMOS level
  SN74HCT194: TTLlevel
- Temperature range:-40℃ to +125℃
- Packaging information: DIP16/SOP16/TSSOP16

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
SN74HC194N (LX)	DIP16	SN74HC194N	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
SN74HCT194N (LX)	DIP16	74HCT194	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
SN74HC194D (LX)	SOP16	SN74HC194	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
SN74HCT194D (LX)	SOP16	HCT194	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
SN74HC194P (LX)	TSSOP16	74HC194	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm
SN74HCT194P (LX)	TSSOP16	74HCT194	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
SN74HC194DR (LX)	SOP16	SN74HC194	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
SN74HCT194DR (LX)	SOP16	74HCT194	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
SN74HC194PW (LX)	TSSOP16	74HC194	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm
SN74HCT194PW (LX)	TSSOP16	74HCT194	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

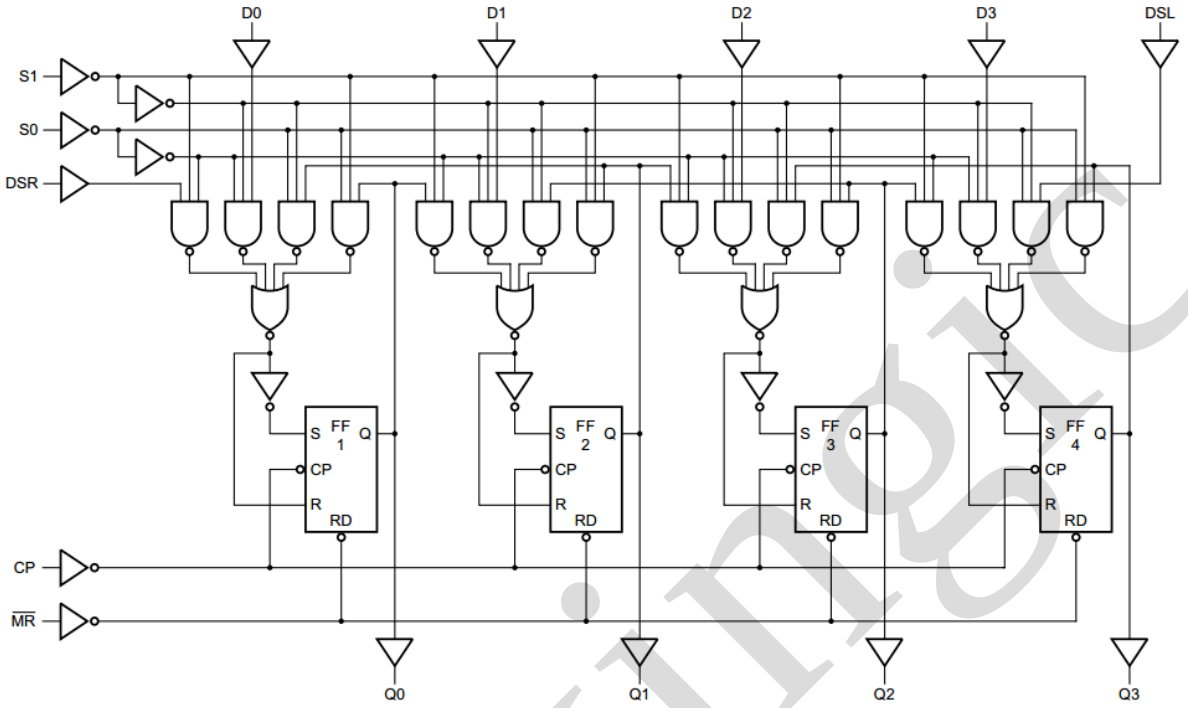


Figure 1. Logic symbol

2.2、Pin Configurations

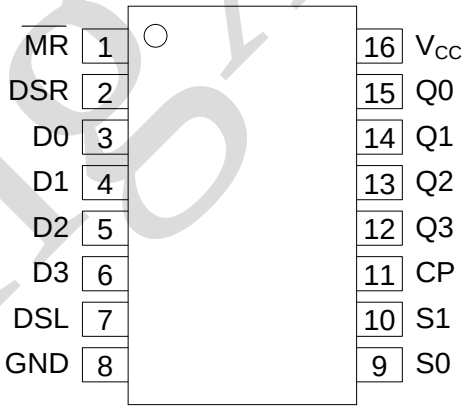


Figure 2. Pin configurations

2.3、Pin Description

Pin No.	Pin Name	Description
1	$\overline{MR}$	Asynchronous master reset input(active low)
2	DSR	serious data input(shift right)
3	D0	parallel data input
4	D1	parallel data input
5	D2	parallel data input
6	D3	parallel data input
7	DSL	Serial data input(shift left)
8	GND	ground (0V)
9	S0	mode control input
10	S1	mode control input
11	CP	Clock input(LOW-to-HIGH edge-triggered)
12	Q3	Parallel output
13	Q2	Parallel output
14	Q1	Parallel output
15	Q0	Parallel output
16	V_{CC}	supply voltage

2.4、Function Table

Operation mode	inputs							Outputs			
	CP	$\overline{MR}$	S1	S0	DSR	DSL	Dn	Q0	Q1	Q2	Q3
reset(clear)	X	L	X	X	X	X	X	L	L	L	L
Hold(do nothing)	X	H	l	l	X	X	X	Q0	Q1	Q2	Q3
Shift left	↑	H	h	l	X	l	X	Q1	Q2	Q3	L
	↑	H	h	l	X	h	X	Q1	Q2	Q3	H
Shift right	↑	H	l	h	l	X	X	L	Q0	Q1	Q2
	↑	H	l	h	h	X	X	H	Q0	Q1	Q2
Parallel load	↑	H	h	h	X	X	Dn	D0	D1	D2	D3

Note:

H=HIGH voltage level; L=LOW voltage level.

h=HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition.

l=LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition.

X=don't care.

↑=LOW to HIGH CP transition.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7	V
supply current	I_{CC}	-		-	50	mA
ground current	I_{GND}	-		-50	-	mA
input clamping current	I_{IK}	V_I<-0.5V or V_I>V_{CC}+0.5V		-	±20	mA
output clamping current	I_{OK}	V_O<-0.5V or V_O>V_{CC}+0.5V		-	±20	mA
output current	I_O	-0.5V<V_O<V_{CC}+0.5V		-	±25	mA
storage temperature	T_{stg}	-		-65	+150	℃
soldering temperature	T_L	10s	DIP	245		℃
			SOP/TSSOP	260		

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SN74HC194						
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
ambient temperature	T_{amb}	-	-40	-	+125	℃
SN74HCT194						
supply voltage	V_{CC}	-	4.5	5.0	5.5	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
ambient temperature	T_{amb}	-	-40	-	+125	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	V_{CC}	Conditions	Min.	Typ.	Max.	Unit
SN74HC194							
HIGH-level input voltage	V_{IH}	2.0V	-	1.5	1.2	-	V
		4.5V	-	3.15	2.4	-	V
		6.0V	-	4.2	3.2	-	V
LOW-level input voltage	V_{IL}	2.0V	-	-	0.8	0.5	V
		4.5V	-	-	2.1	1.35	V
		6.0V	-	-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	2.0V	I_O=-20uA	1.9	2.0	-	V
		4.5V	I_O=-20uA	4.4	4.5	-	V
		6.0V	I_O=-20uA	5.9	6.0	-	V
		4.5V	I_O=-4.0mA	3.84	4.32	-	V
		6.0V	I_O=-5.2mA	5.34	5.81	-	V
LOW-level	V_{OL}	2.0V	I_O=20uA	-	0	0.1	V

output voltage		4.5V	I_O=20uA	-	0	0.1	V
		6.0V	I_O=20uA	-	0	0.1	V
		4.5V	I_O=4.0mA	-	0.15	0.33	V
		6.0V	I_O=5.2mA	-	0.16	0.33	V
input leakage current	I_I	6.0V	V_I=V_{CC} or GND	-	-	±1	uA
supply current	I_{CC}	6.0V	V_I=V_{CC} or GND; I_O=0A	-	-	80	uA
SN74HCT194							
HIGH-level input voltage	V_{IH}	4.5V to 5.5V	-	2.0	1.6	-	V
LOW-level input voltage	V_{IL}	4.5V to 5.5V	-	-	1.2	0.8	V
HIGH-level output voltage	V_{OH}	4.5V	I_O=-20uA	4.4	4.5	-	V
			I_O=-4.0mA	3.84	4.32	-	V
LOW-level output voltage	V_{OL}	4.5V	I_O=20uA	-	0	0.1	V
			I_O=4.0mA	-	0.15	0.33	V
input leakage current	I_I	5.5V	V_I=V_{CC} or GND	-	-	±1	uA
supply current	I_{CC}	6.0V	V_I=V_{CC} or GND; I_O=0A	-	-	80	uA
additional supply current	ΔI_{CC}	4.5V to 5.5V	One input at V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; I_O=0A	-	-	135	uA

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	**Symbol**	**V_{CC}**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
SN74HC194							
HIGH-level input voltage	V_{IH}	2.0V	-	1.5	-	-	V
		4.5V	-	3.15	-	-	V
		6.0V	-	4.2	-	-	V
LOW-level input voltage	V_{IL}	2.0V	-	-	-	0.5	V
		4.5V	-	-	-	1.35	V
		6.0V	-	-	-	1.8	V
HIGH-level output voltage	V_{OH}	2.0V	I_O=-20uA	1.9	-	-	V
		4.5V	I_O=-20uA	4.4	-	-	V
		6.0V	I_O=-20uA	5.9	-	-	V
		4.5V	I_O=-4.0mA	3.7	-	-	V
		6.0V	I_O=-5.2mA	5.2	-	-	V
LOW-level output voltage	V_{OL}	2.0V	I_O=20uA	-	-	0.1	V
		4.5V	I_O=20uA	-	-	0.1	V
		6.0V	I_O=20uA	-	-	0.1	V
		4.5V	I_O=4.0mA	-	-	0.4	V
		6.0V	I_O=5.2mA	-	-	0.4	V
input leakage current	I_I	6.0V	V_I=V_{CC} or GND	-	-	±1	uA
supply current	I_{CC}	6.0V	V_I=V_{CC} or GND; I_O=0A	-	-	160	uA
SN74HCT194							

HIGH-level input voltage	V_{IH}	4.5V to 5.5V	-	2.0	-	-	V
LOW-level input voltage	V_{IL}	4.5V to 5.5V	-	-	-	0.8	V
HIGH-level output voltage	V_{OH}	4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-4.0mA	3.7	-	-	V
LOW-level output voltage	V_{OL}	4.5V	I_O=20uA	-	-	0.1	V
			I_O=4.0mA	-	-	0.4	V
input leakage current	I_I	5.5V	V_I=V_{CC} or GND	-	-	±1	uA
supply current	I_{CC}	6.0V	V_I=V_{CC} or GND; I_O=0A	-	-	160	uA
additional supply current	ΔI_{CC}	4.5V to 5.5V	One input at V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; I_O=0A	-	-	147	uA

3.3.3、AC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	V_{CC}	Conditions		Min.	Typ.	Max.	Unit
SN74HC194								
CP to Qn propagation delay	t_{PLH}, t_{PHL}	2.0V	C_L=50pF	see Figure 4	-	47	155	ns
		4.5V	C_L=50pF		-	17	36	ns
		6.0V	C_L=50pF		-	14	31	ns
$\overline{MR}$ to Qn propagation delay	t_{PHL}	2.0V	C_L=50pF	see Figure 5	-	39	175	ns
		4.5V	C_L=50pF		-	14	35	ns
		6.0V	C_L=50pF		-	11	30	ns
transition time	t_{THL}, t_{TLH}	2.0V	C_L=50pF	see Figure 5	100	17	-	ns
		4.5V	C_L=50pF		20	6	-	ns
		6.0V	C_L=50pF		17	5	-	ns
clock pulse width	t_W	2.0V	C_L=50pF	see Figure 4	100	17	-	ns
		4.5V	C_L=50pF		20	6	-	ns
		6.0V	C_L=50pF		17	5	-	ns
master reset pulse	t_W	2.0V	C_L=50pF	see Figure 5	100	17	-	ns
		4.5V	C_L=50pF		20	6	-	ns
		6.0V	C_L=50pF		17	5	-	ns
$\overline{MR}$ to CP removal time	trem	2.0V	C_L=50pF	see Figure 5	60	17	-	ns
		4.5V	C_L=50pF		12	6	-	ns
		6.0V	C_L=50pF		10	5	-	ns
Dn to CP set-up time	tsu	2.0V	C_L=50pF	see Figure 6	90	17	-	ns
		4.5V	C_L=50pF		18	6	-	ns
		6.0V	C_L=50pF		15	5	-	ns
S0, S1 to CP set-up time		2.0V	C_L=50pF	see Figure 7	100	22	-	ns
		4.5V	C_L=50pF		20	8	-	ns
		6.0V	C_L=50pF		17	6	-	ns
DSR, DSL to CP set-up time		2.0V	C_L=50pF	see Figure 6	90	19	-	ns
		4.5V	C_L=50pF		18	7	-	ns
		6.0V	C_L=50pF		15	6	-	ns

Dn to CP hold time	th	2.0V	C_L=50pF	see Figure 6	0	-14	-	ns
		4.5V	C_L=50pF		0	-5	-	ns
		6.0V	C_L=50pF		0	-4	-	ns
S0, S1 to CP hold time		2.0V	C_L=50pF	see Figure 7	0	-11	-	ns
		4.5V	C_L=50pF		0	-4	-	ns
		6.0V	C_L=50pF		0	-3	-	ns
DSR, DSL to CP hold time		2.0V	C_L=50pF	see Figure 6	0	-17	-	ns
		4.5V	C_L=50pF		0	-6	-	ns
		6.0V	C_L=50pF		0	-5	-	ns
maximum clock pulse frequency	fmax	2.0V	C_L=50pF	see Figure 4	4.8	31	-	MHz
		4.5V	C_L=50pF		24	93	-	MHz
		6.0V	C_L=50pF		28	111	-	MHz
SN74HCT194								
CP to Qn propagation delay	t_{PLH}, t_{PHL}	4.5V	C_L=50pF	see Figure 4	-	18	40	ns
$\overline{MR}$ to Qn propagation delay	t_{PHL}	4.5V	C_L=50pF	see Figure 5	-	18	40	ns
transition time	t_{THL}, t_{TLH}	4.5V	C_L=50pF	see Figure 5	-	7	19	ns
clock pulse width	t_W	4.5V	C_L=50pF	see Figure 4	20	7	-	ns
master reset pulse	t_W	4.5V	C_L=50pF	see Figure 5	20	7	-	ns
$\overline{MR}$ to CP removal time	trem	4.5V	C_L=50pF	see Figure 5	15	6	-	ns
Dn to CP set-up time	tsu	4.5V	C_L=50pF	see Figure 6	18	7	-	ns
S0, S1 to CP set-up time		4.5V	C_L=50pF	see Figure 7	25	10	-	ns
DSR, DSL to CP set-up time		4.5V	C_L=50pF	see Figure 6	18	-	-	ns
Dn to CP hold time	th	4.5V	C_L=50pF	see Figure 6	0	-7	-	ns
S0, S1 to CP hold time		4.5V	C_L=50pF	see Figure 7	0	-5	-	ns
DSR, DSL to CP hold time		4.5V	C_L=50pF	see Figure 6	0	-7	-	ns
maximum clock pulse frequency	fmax	4.5V	C_L=50pF	see Figure 4	24	70	-	MHz

3.3.4、AC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	V_{CC}	Conditions		Min.	Typ.	Max.	Unit
SN74HC194								
CP to Qn propagation delay	t_{PLH}, t_{PHL}	2.0V	C_L=50pF	see Figure 4	-	-	220	ns
		4.5V	C_L=50pF		-	-	44	ns
		6.0V	C_L=50pF		-	-	38	ns
$\overline{MR}$ to Qn propagation delay	t_{PHL}	2.0V	C_L=50pF	see Figure 5	-	-	210	ns
		4.5V	C_L=50pF		-	-	42	ns
		6.0V	C_L=50pF		-	-	36	ns
transition time	t_{THL}, t_{TLH}	2.0V	C_L=50pF	see Figure 5	-	-	110	ns
		4.5V	C_L=50pF		-	-	22	ns
		6.0V	C_L=50pF		-	-	19	ns
clock pulse width	t_W	2.0V	C_L=50pF	see Figure 4	120	-	-	ns
		4.5V	C_L=50pF		24	-	-	ns
		6.0V	C_L=50pF		20	-	-	ns
master reset pulse	t_W	2.0V	C_L=50pF	see Figure 5	120	-	-	ns
		4.5V	C_L=50pF		24	-	-	ns
		6.0V	C_L=50pF		20	-	-	ns
$\overline{MR}$ to CP removal time	trem	2.0V	C_L=50pF	see Figure 5	90	-	-	ns
		4.5V	C_L=50pF		18	-	-	ns
		6.0V	C_L=50pF		15	-	-	ns
Dn to CP set-up time	tsu	2.0V	C_L=50pF	see Figure 6	105	-	-	ns
		4.5V	C_L=50pF		21	-	-	ns
		6.0V	C_L=50pF		18	-	-	ns
S0, S1 to CP set-up time		2.0V	C_L=50pF	see Figure 7	120	-	-	ns
		4.5V	C_L=50pF		24	-	-	ns
		6.0V	C_L=50pF		20	-	-	ns
DSR, DSL to CP set-up time		2.0V	C_L=50pF	see Figure 6	105	-	-	ns
		4.5V	C_L=50pF		21	-	-	ns
		6.0V	C_L=50pF		18	-	-	ns
Dn to CP hold time	th	2.0V	C_L=50pF	see Figure 6	0	-	-	ns
		4.5V	C_L=50pF		0	-	-	ns
		6.0V	C_L=50pF		0	-	-	ns
S0, S1 to CP hold time		2.0V	C_L=50pF	see Figure 7	0	-	-	ns
		4.5V	C_L=50pF		0	-	-	ns
		6.0V	C_L=50pF		0	-	-	ns
DSR, DSL to CP hold time		2.0V	C_L=50pF	see Figure 6	0	-	-	ns
		4.5V	C_L=50pF		0	-	-	ns
		6.0V	C_L=50pF		0	-	-	ns
maximum clock pulse frequency	fmax	2.0V	C_L=50pF	see Figure 4	4.0	-	-	MHz
		4.5V	C_L=50pF		20	-	-	MHz
		6.0V	C_L=50pF		24	-	-	MHz
SN74HCT194								
CP to Qn	t_{PLH}, t_{PHL}	4.5V	C_L=50pF	see Figure 4	-	-	48	ns

propagation delay								
$\overline{MR}$ to Qn propagation delay	t_{PHL}	4.5V	C_L=50pF	see Figure 5	-	-	48	ns
transition time	t_{THL}, t_{TLH}	4.5V	C_L=50pF	see Figure 5	-	-	22	ns
clock pulse width	t_W	4.5V	C_L=50pF	see Figure 4	24	-	-	ns
master reset pulse	t_W	4.5V	C_L=50pF	see Figure 5	24	-	-	ns
$\overline{MR}$ to CP removal time	trem	4.5V	C_L=50pF	see Figure 5	18	-	-	ns
Dn to CP set-up time	tsu	4.5V	C_L=50pF	see Figure 6	21	-	-	ns
S0, S1 to CP set-up time		4.5V	C_L=50pF	see Figure 7	30	-	-	ns
DSR, DSL to CP set-up time		4.5V	C_L=50pF	see Figure 6	21	-	-	ns
Dn to CP hold time	th	4.5V	C_L=50pF	see Figure 6	0	-	-	ns
S0, S1 to CP hold time		4.5V	C_L=50pF	see Figure 7	0	-	-	ns
DSR, DSL to CP hold time		4.5V	C_L=50pF	see Figure 6	0	-	-	ns
maximum clock pulse frequency	fmax	4.5V	C_L=50pF	see Figure 4	20	-	-	MHz

4、Testing Circuit

4.1、AC Testing Circuit

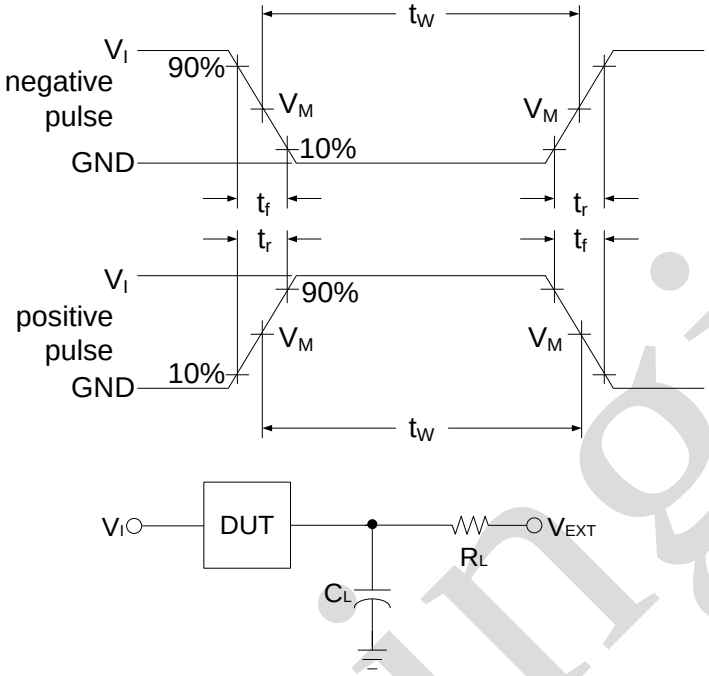


Figure 3. Test circuit for measuring switching times

C_L includes probe and jig capacitance.

4.2、Test Data

Type	Input		Load		V_{EXT}		
	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}/t_{PHL}	t_{PLZ}/t_{PZL}	t_{PHZ}/t_{PZH}
SN74HC194	V_{CC}	6.0ns	50pF	1KΩ	Open	V_{CC}	GND
SN74HCT194	3.0V	6.0ns	50pF	1KΩ	Open	V_{CC}	GND

4.3、AC Testing Waveforms

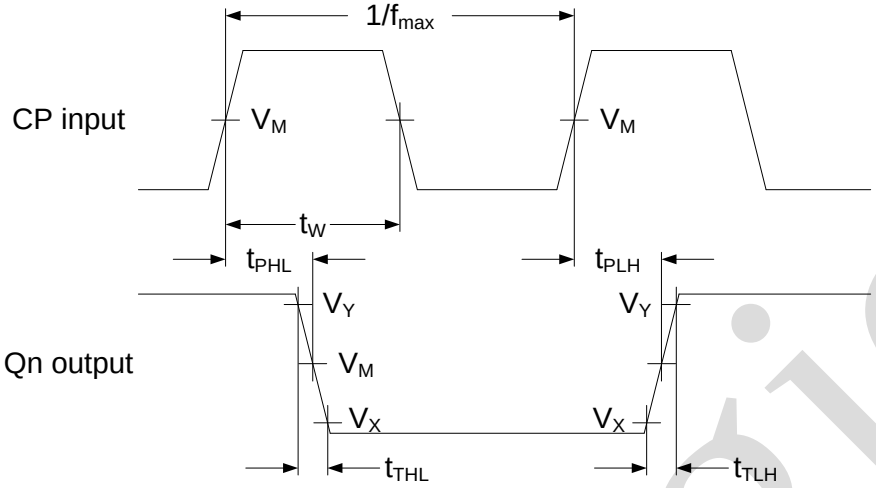


Figure 4. Waveforms showing the clock (CP) to output (Qn) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency

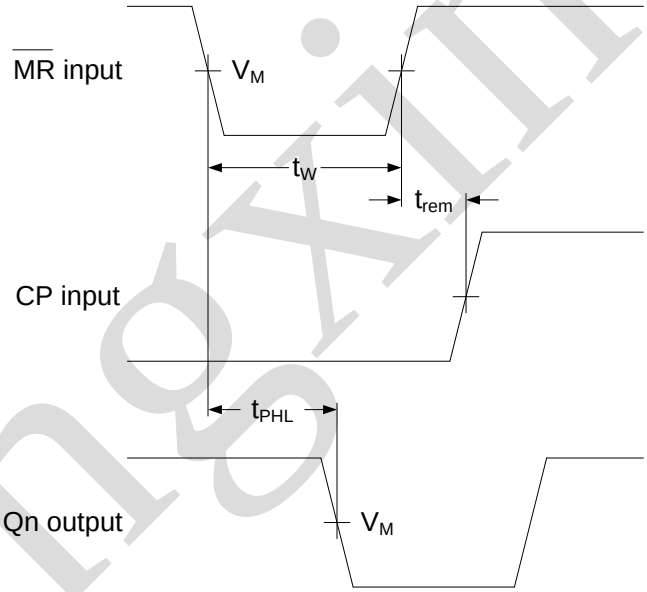


Figure 5. Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Qn) propagation delays and the master reset to clock (CP) removal time

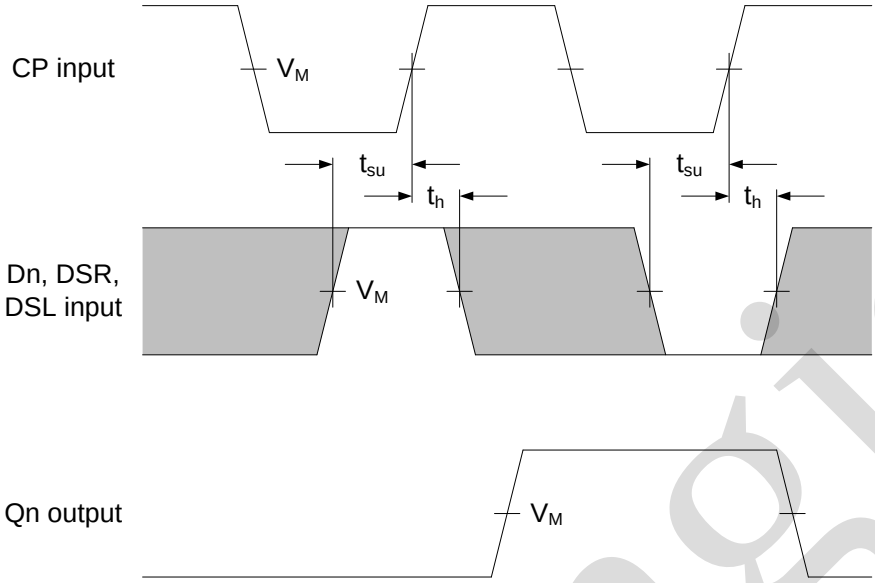


Figure 6. Waveforms showing the set-up and holdtimes from the data inputs (Dn, DSR and DSL) to the clock (CP).

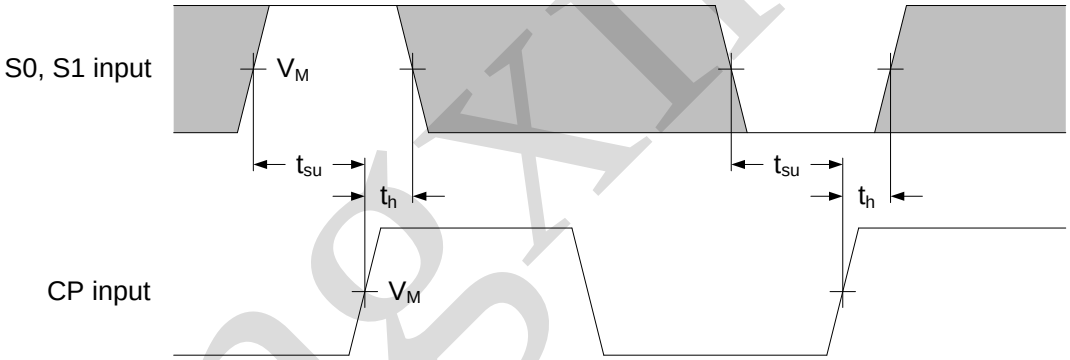


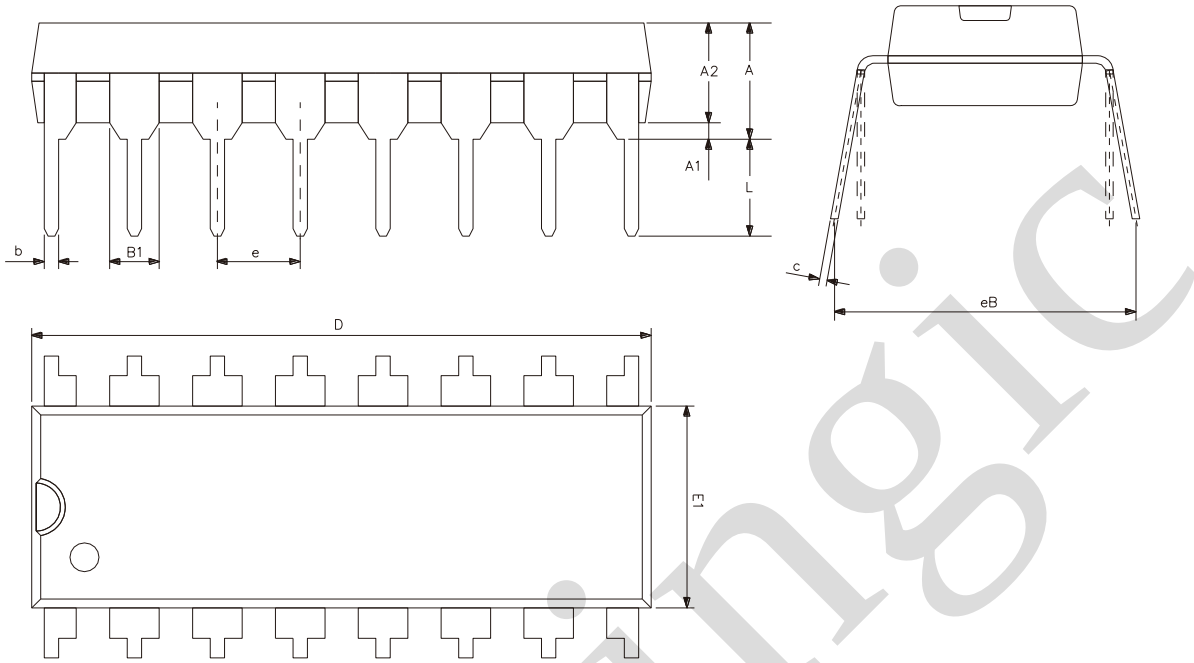
Figure 7. Waveforms showing the set-up and hold times from the mode control inputs (Sn) to the clock input (CP).

4.4、Measurement Points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
SN74HC194	$0.5\times V_{CC}$	$0.5\times V_{CC}$	$0.1\times V_{CC}$	$0.9\times V_{CC}$
SN74HCT194	1.3V	1.3V	$0.1\times V_{CC}$	$0.9\times V_{CC}$

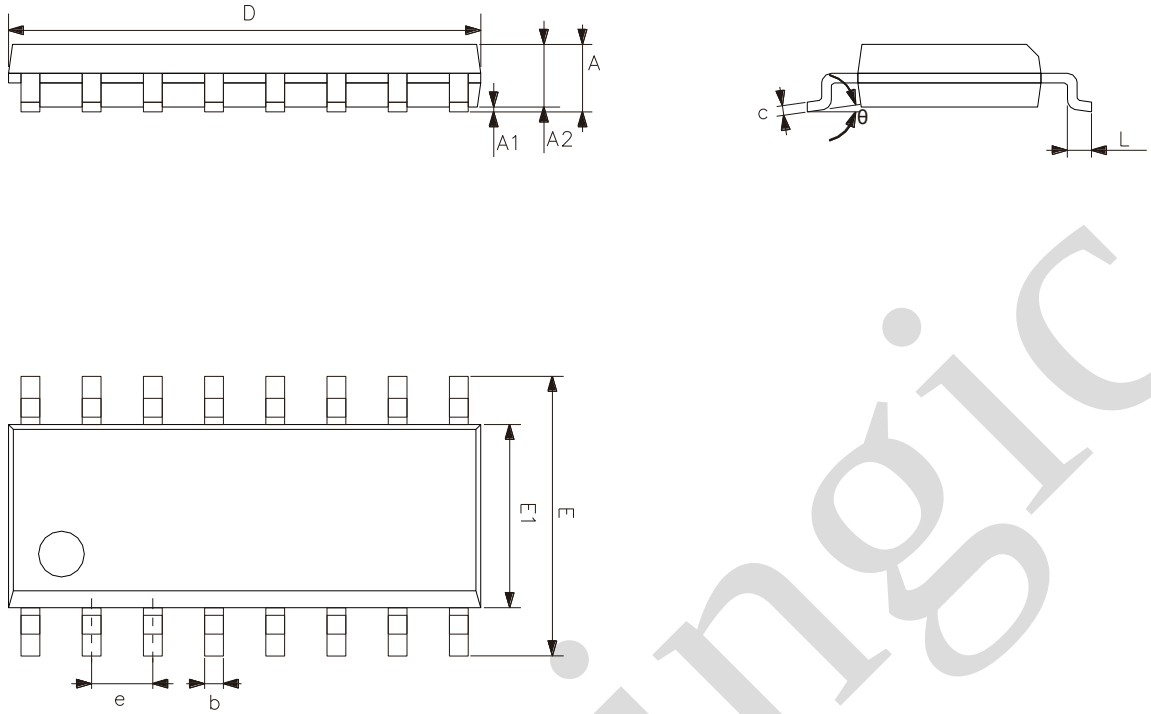
5、Package Information

5.1、DIP16



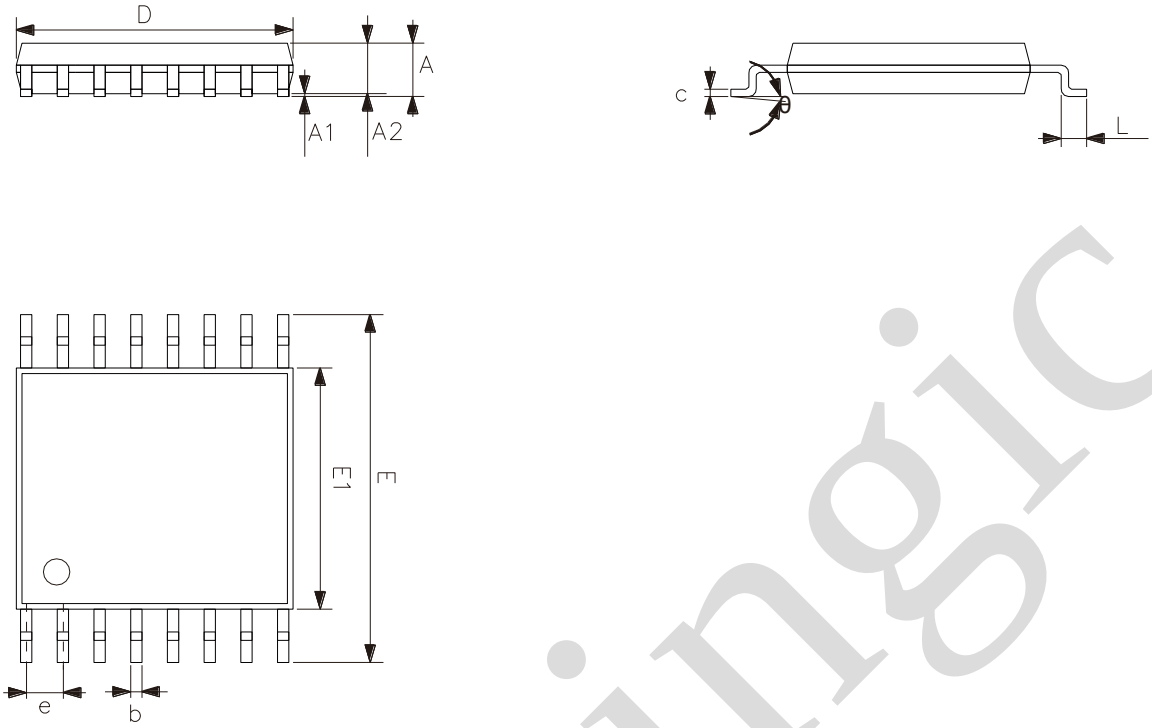
Symbol	Dimensions (mm)	
	Min.	Max.
A2	3.20	3.60
A1	0.51	-
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30

5.2、SOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°

5.3、TSSOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

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