

# JK-SMD0603-003 PPTC DEVICES

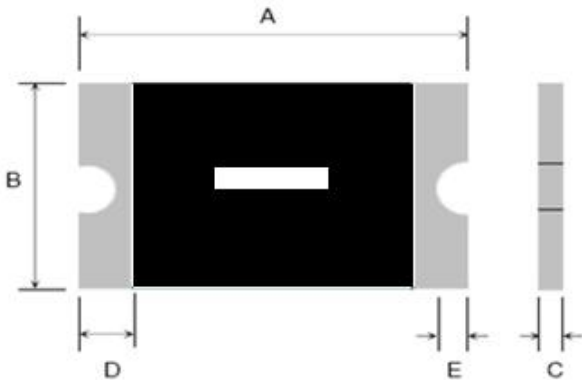
Part Number: Q/JKTD-24-003

Edition: A0

Page No: 1 OF 4



金瑞电子材料  
Jinrui Electronic material



Terminal pad materials :Tin-Plated Nickle-copper

Terminal pad solderability : Meets EIA specification  
RS 186-9E and ANSI/J-STD-002 Category 3.

Marking : Part identification — =003

Table1 :DIMENTION(Unit : mm)

Model	Marking	A		B		C		D	E
		Min.	Max.	Min.	Max.	Min.	Max	Min.	Max.
JK-SMD0603-003	—	1.45	1.85	0.65	1.05	0.40	1.00	0.15	0.40

Table2 :PERFORMANCE RATINGS:

Model	Marking	$V_{max}$ (Vdc)	$I_{max}$ (A)	$I_{hold}$ @25℃ (A)	$I_{trip}$ @25℃ (A)	$P_d$ Typ (W)	Maximum Time To Trip		Resistance	
							Current (A)	Time (Sec)	$R_{1min}$ (Ω)	$R_{1max}$ (Ω)
JK-SMD0603-003	—	24.0	40	0.03	0.09	0.50	0.2	1.00	6.0	65.000

Table3:Test Conditons and Standards

Item	Test Conditon	Standard
Initial Resistance	25℃	6.00~65.000Ω
$I_H$	25℃, 0.03A, 60min	No Trip
$T_{trip}$	25℃, 0.2A	≤1.0S
Trip endurance	24V, 40A, 60min	No arcing or burning

Operating Temperature: -40℃ TO 85℃

Packaging: Tape ,5000pcs per bag

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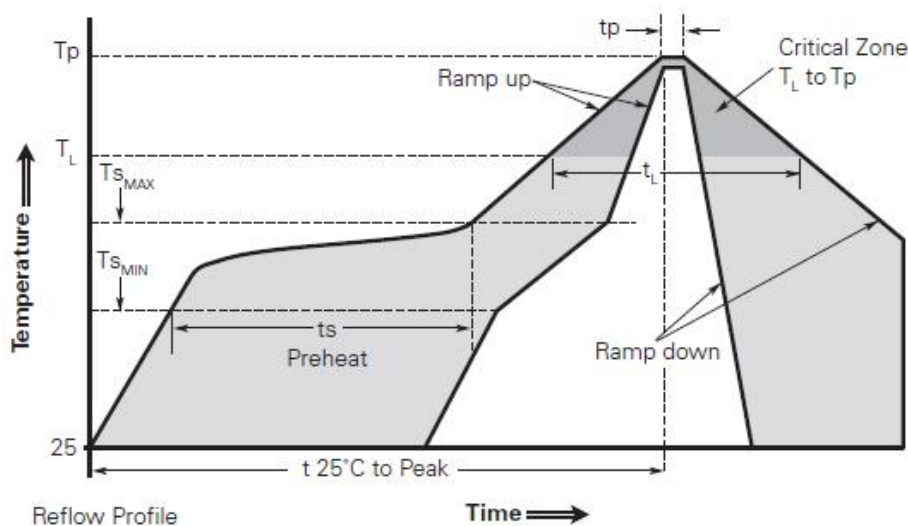
Edition: A0

Page No: 2 OF 4



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Solder reflow conditions



Profile Feature	Pb-Free Assembly
Average ramp up rate (Ts_MAX to Tp)	3°C/second max.
Preheat	
• Temperature min. (Ts_MIN)	150°C
• Temperature max. (Ts_MAX)	200°C
• Time (ts_MIN to ts_MAX)	60-120 seconds
Time maintained above:	
• Temperature (T_L)	217°C
• Time (t_L)	60-150 seconds
Peak/Classification temperature (Tp)	260°C
Time within 5°C of actual peak temperature	
Time (tp)	30 seconds max.
Ramp down rate	3°C/second max.
Time 25°C to peak temperature	8 minutes max.

Note: All temperatures refer to top side of the package, measured on the package body surface.

- Recommended reflow methods: IR, vapor phase oven, hot air oven, N2 environment for lead-free.
- Devices are not designed to be wave soldered to the bottom side of the board.
- Recommended maximum paste thickness is 0.25mm (0.010inch).
- Devices can be cleaned using standard industry methods and solvents.
- Soldering temperature profile meets RoHs leadfree process.

Notes: If reflow temperatures exceed the recommended profile, devices may not meet the performance requirements

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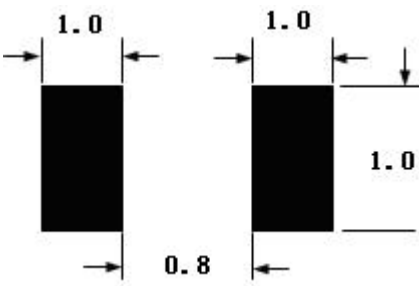
Page No: 3 OF 4



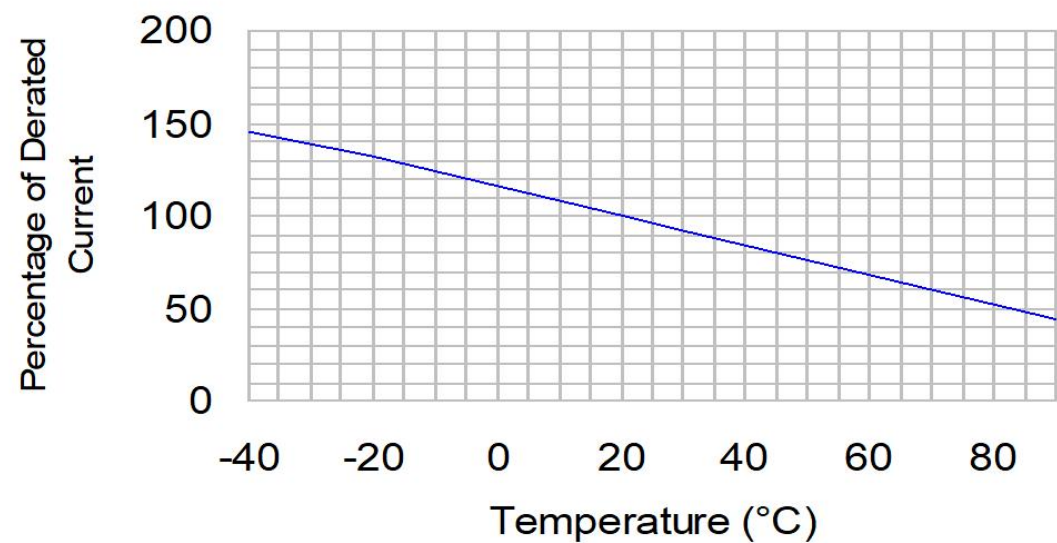
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Recommended pad layout (mm)



Derating Curves for SMD0603 Series



# JK-SMD0603-004 PPTC DEVICES

Part Number: Q/JKTD-24-004

Edition: A0

Page No: 4 OF 4



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## WARNING

- Use PPTC beyond the maximum ratings or improper use may result in device damage and possible electrical arcing and flame.
- PPTC are intended for protection against occasional over current or over temperature fault conditions and should not be used when repeated fault conditions or prolonged trip events are anticipated.
- Device performance can be impacted negatively if devices are handled in a manner inconsistent with recommended electronic, thermal, and mechanical procedures for electronic components.
- Use PPTC with a large inductance in circuit will generate a circuit voltage ( $L di/dt$ ) above the rated voltage of the PPTC.
- Avoid impact PPTC device its thermal expansion like placed under pressure or installed in limited space.
- Contamination of the PPTC material with certain silicon based oils or some aggressive solvents can adversely impact the performance of the devices. PPTC SMD can be cleaned by standard methods.
- Requests that customers comply with our recommended solder pad layouts and recommended reflow profile. Improper board layouts or reflow profile could negatively impact solderability performance of our devices.