

MSQ60P04D

P-Channel 60-V (D-S) MOSFET

Description

The device is the highest performance trench P-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge. It's well suited for high efficiency fast switching applications. The device meets RoHS and Green Product requirement.

Features

- $R_{DS(ON)} < 70\text{m}\Omega @ V_{GS} = -10\text{V}$
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

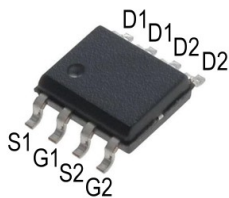
Typical Applications

- MB / VGA / Vcore
- POL Applications
- SMPS 2nd SR

Package type : SOP-8

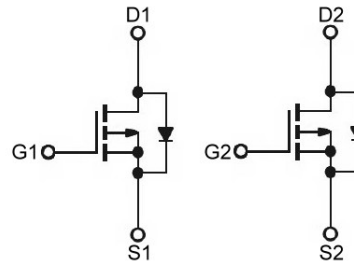
Packing & Order Information

3,000/Reel

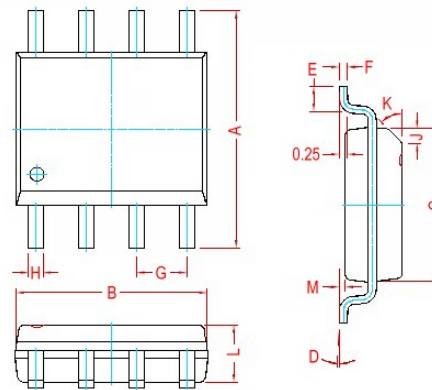


RoHS Compliant

Graphic Symbol

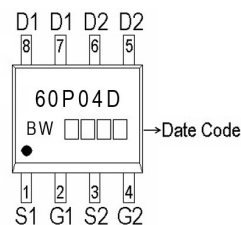


Package Dimension



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	M	0.10	0.25
B	4.80	5.00	H	0.35	0.51
C	3.80	4.00	L	1.35	1.75
D	0°	8°	J	0.40 Ref.	
E	0.40	0.90	K	45° Ref.	
F	0.19	0.26	G	1.27 Typ.	

Marking



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MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	-60	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current ¹ ($T_A = 25^\circ\text{C}$)	-3.7	A
	Continuous Drain Current ¹ ($T_A = 70^\circ\text{C}$)	-3	A
I_{DM}	Pulsed Drain Current ^{1,2}	-7.5	A
EAS	Single Pulse Avalanche Energy ³	35.4	mJ
I_{AS}	Avalanche Current	-26.6	A
P_D	Power Dissipation ⁴ ($T_A = 25^\circ\text{C}$)	1.5	W
T_J/T_{STG}	Operating Junction and Storage Temperature	-55 to +150	$^\circ\text{C}$

Thermal Resistance Ratings

Symbol	Parameter	Maximum	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ¹	85	$^\circ\text{C/W}$

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = -250\mu\text{A}$	-1.2	-	-2.5	V
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}$, $I_D = -250\mu\text{A}$	-60	-	-	V
g_{fs}	Forward Transconductance	$V_{DS} = -5\text{V}$, $I_D = -3\text{A}$	-	15	-	S
I_{GSS}	Gate-Source Leakage Current	$V_{DS} = 0\text{V}$, $V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
I_{DSS}	Drain-Source Leakage Current	$V_{DS} = -48\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 25^\circ\text{C}$	-	-	-1	μA
		$V_{DS} = -48\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 55^\circ\text{C}$	-	-	-5	
$R_{DS(on)}$	Static Drain-Source On-Resistance ²	$V_{GS} = -10\text{V}$, $I_D = -3\text{A}$	-	58	70	m Ω
		$V_{GS} = -4.5\text{V}$, $I_D = -2\text{A}$	-	78	105	
V_{SD}	Diode Forward Voltage ²	$I_S = -1\text{A}$, $V_{GS} = 0\text{V}$, $T_J = 25^\circ\text{C}$	-	-	-1.2	V
I_S	Continuous Source Current ^{1,4}	$V_G = V_D = 0\text{V}$, Force Current	-	-	-3.7	A
I_{SM}	Pulsed Source Current ^{2,4}		-	-	-7.5	

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Dynamic						
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Q _g	Total Gate Charge ²	V _{DS} = -48V	--	9.86	--	nC
Q _{gs}	Gate-Source Charge	I _D = -3A	--	3.08	--	
Q _{gd}	Gate-Drain Charge	V _{GS} = -4.5V	--	2.95	--	
t _{d(on)}	Turn-On Delay Time ²	V _{DS} = -15V	--	28.8	--	ns
t _r	Rise Time	I _D = -1A	--	19.8	--	
t _{d(off)}	Turn-Off Delay Time	V _{GS} = -10V	--	60.8	--	
t _f	Fall Time	R _G = 3.3Ω	--	7.2	--	
C _{iss}	Input Capacitance	V _{DS} = -15V	--	1447	--	pF
C _{oss}	Output Capacitance	V _{GS} = 0V	--	97.3	--	
C _{rss}	Reverse Transfer Capacitance	f = 1.0MHz	--	70	--	
R _g	Gate Resistance	V _{GS} = V _{DS} = 0V, f = 1.0MHz	--	13.5	--	Ω

Notes

1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
3. The EAS data shows Max. rating. The test condition is V_{DD} = -25V, V_{GS} = -10V, L = 0.1mH, I_{AS} = -26.6A
4. The power dissipation is limited by 150°C junction temperature.
5. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

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- Typical Electrical Characteristics

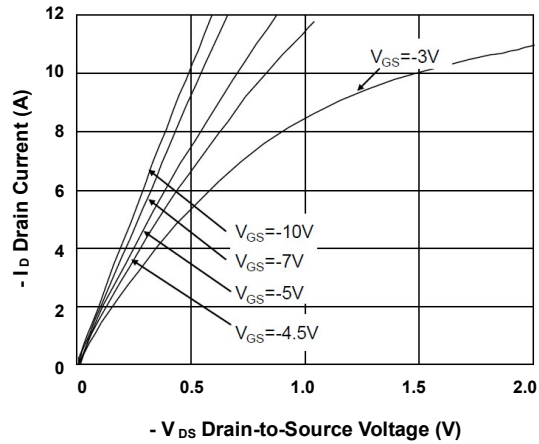


FIG.1-Typical Output Characteristics

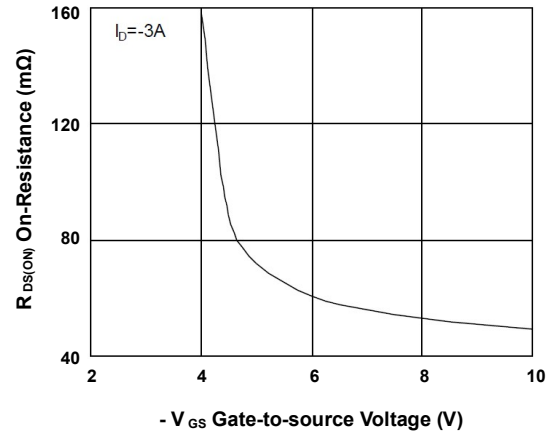


FIG.2-On-Resistance vs. G-S Voltage

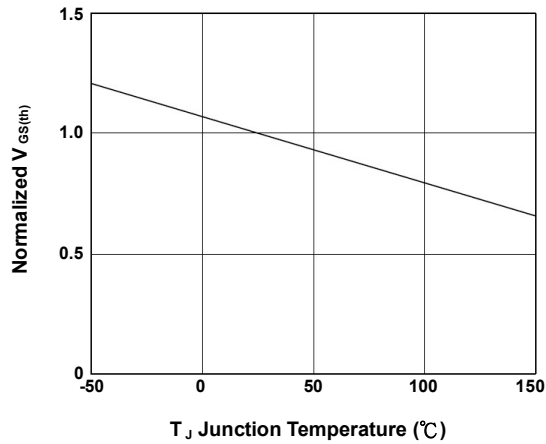


FIG.3-Normalized $V_{GS(th)}$ vs. T_J

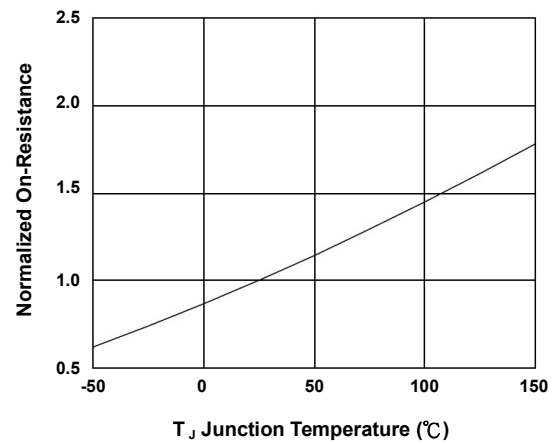


FIG.4-Normalized $R_{DS(ON)}$ vs. T_J

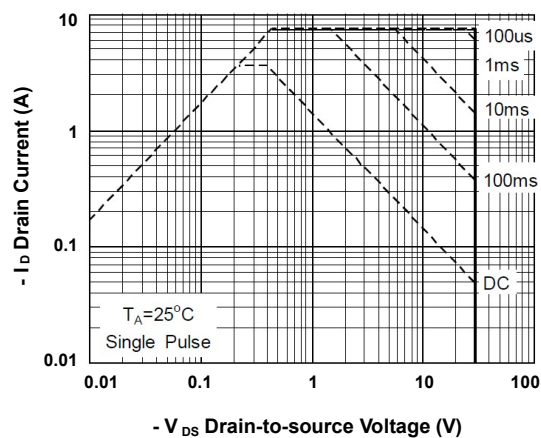


FIG.5-Safe Operating Area

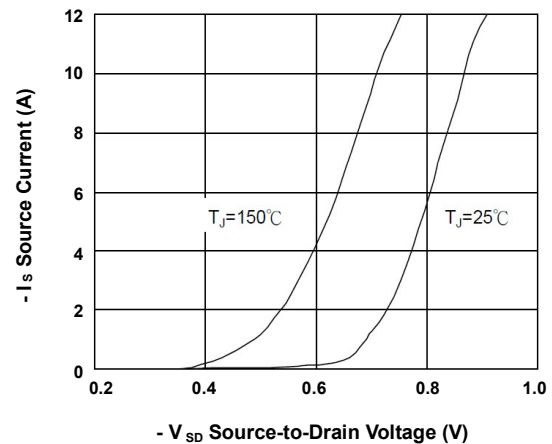


FIG.6-Forward Characteristics of Reverse

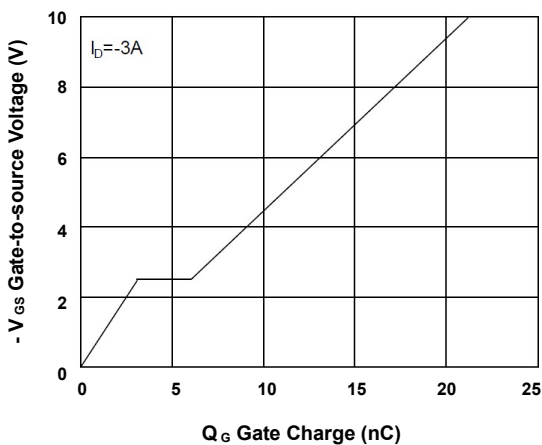


FIG.7-Gate Charge Characteristics

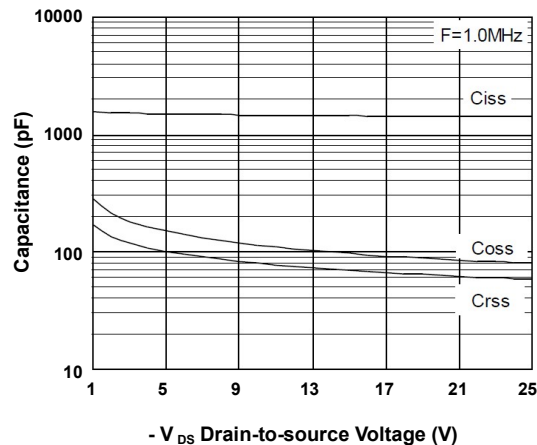


FIG.8-Capacitance Characteristics

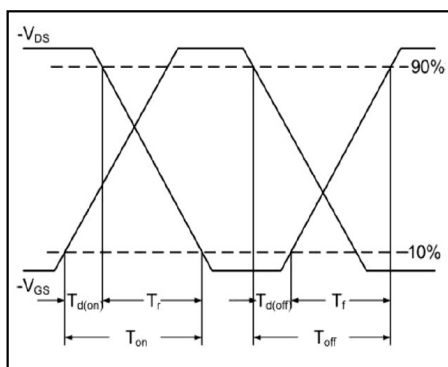


FIG.9-Switching Time Waveform

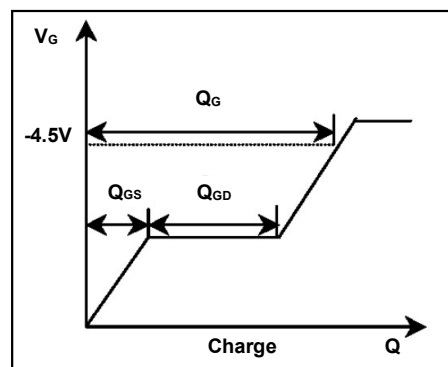


FIG.10-Gate Charge Waveform

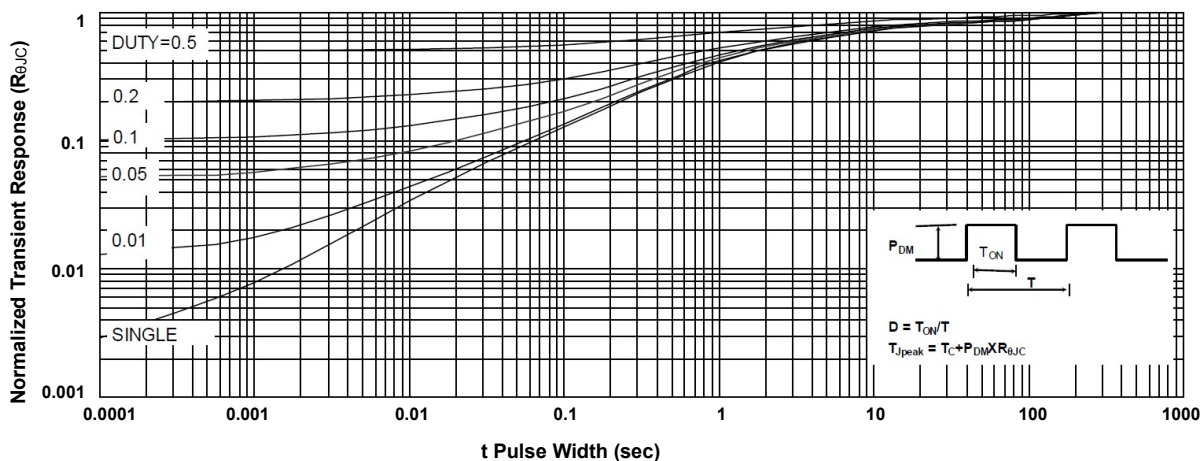


FIG.11-Normalized Maximum Transient Thermal Impedance

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