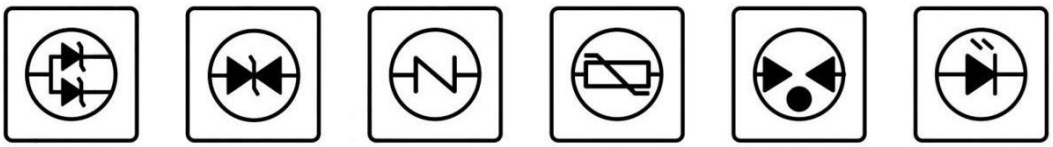
MSKSEMI 美森科
SEMICONDUCTOR



AT4950-MS

Product specification

GENERAL DESCRIPTION

The AT4950-MS devices are a brushed-DC motor driver for printers, appliances, industrial equipment, and other small machines. Two logic inputs control the H-bridge driver, which consists of four N-channel MOSFETs that can control motors bi-directionally with up to 3.6-A peak current. The inputs can be pulse width modulated (PWM) to control motor speed, using a choice of current-decay modes. Setting both inputs slow enter a low-power sleep mode.

The AT4950-MS devices feature integrated current regulation, based on the analog input VREF and the voltageon the ISEN pin, which is proportional to motor current through an external sense resistor. The ability to limit current to a known level can significantly reduce the system power requirements and bulk capacitance needed to maintain stable voltage, especially for motor startup and stall conditions.

The devices are fully protected from faults and short circuits, including UVLO，OCP, and TSD.

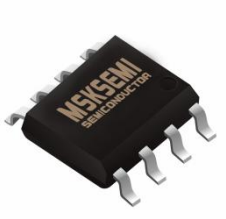
FEATURES

- H-Bridge Motor Driver
  Drives One DC Motor, One Winding of a Stepper Motor, or Other Loads
- Wide 6.5V to 40V Operating Voltage
- 3.6-A Peak Current Drive
- PWM Control Interface
- Integrated Current Regulation
- Low-Power Sleep Mode
- VM under voltage Lockout (UVLO)
- Overcurrent Protection (OCP)
  - Retry after OCP: AT4950-MS
- Thermal Shutdown (TSD)
- Automatic Fault Recovery
- ESOP8 Small Package and Footprint

APPLICATIONS

- Printers
- Appliances
- Industrial Equipment
- Other Mechatronics Applications

PACKAGE/ORDER INFORMATION

Part Number	Package		Marking	QTY
AT4950-MS	ESOP8		MSKSEMI AT4950 MS XXX	4000

TYPICAL APPILCATION

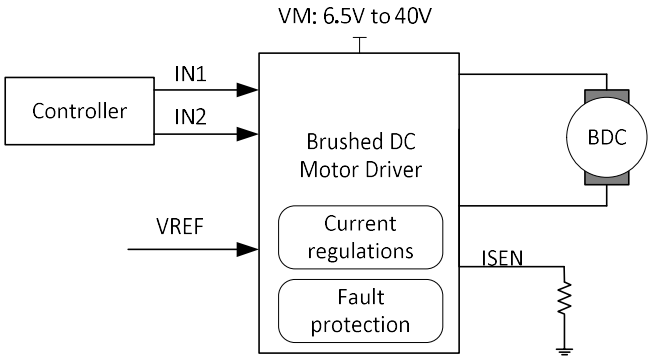
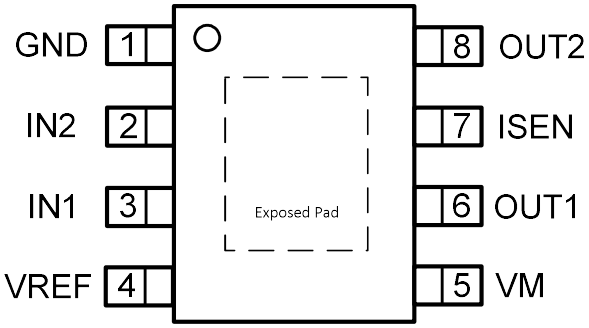


Figure 1. Basic Application Circuit

ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Value		Unit
	Min	Max	
Power supply voltage (VM)	-0.3	45	V
Logic input voltage (IN1, IN2)	-0.3	6	V
Reference input pin voltage (VREF)	-0.3	6	V
Continuous phase node pin voltage (OUT1, OUT2)	-0.7	VM+0.7	V
Current sense input pin voltage (ISEN)	-0.5	1	V
Output current (100% duty cycle)	0	3.5	A
Operating junction temperature (Note 2)	-40	150	°C
Storage temperature	-65	150	°C

PACKAGE/ORDER INFORMATION



ESOP8

PIN FUNCTIONS

Pin	Name	Function
1	GND	Logic ground. Connect to board ground
2	IN2	Logic inputs. Controls the H-bridge output. Has 100KΩ internal pulldowns.
3	IN1	Logic inputs. Controls the H-bridge output. Has 100KΩ internal pulldowns.
4	VREF	Analog input. Apply a voltage between 0.3V to 5 V.
5	VM	6.5V to 40V power supply. Connect a 0.1µF bypass capacitor to ground, as well as sufficient bulk capacitance, rated for the VM voltage.
6	OUT1	H-bridge output. Connect directly to the motor or other inductive load.
7	ISEN	High-current ground path. If using current regulation, connect ISEN to a resistor (low-value, high-power-rating) to ground. If not using current regulation, connect ISEN directly to ground.
8	OUT2	H-bridge output. Connect directly to the motor or other inductive load.

ESD RATING

Items	Description	Value	Unit
V_{ESD}	Human Body Model for all pins	±2000	V

JEDEC specification JS-001

RECOMMENDED OPERATING CONDITIONS

Items	Description	Min	Max	Unit
VM	Power supply voltage range	6.5	40	V
T_J	Operating Junction Temperature Range	-40	125	°C

ELECTRICAL CHARACTERISTICS (Note 3)

T_A = 25°C, over recommended operating conditions unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VM)						
VM operating voltage	VM		6.5		40	V
VM operating supply current	I_{VM}	VM = 24V		2	10	mA
VM sleep current	$I_{VMSLEEP}$	VM = 24V			15	μA
Turn-on time (Note 4)	t_{ON}	VM > VUVLO with IN1 or IN2 high		45		μs
LOGIC-LEVEL INPUTS (IN1, IN2)						
Input logic low voltage	V_{IL}				0.5	V
Input logic high voltage	V_{IH}		2			V
Input logic hysteresis	V_{HYS}			0.2		V
Input logic low current	I_{IL}	VIN = 0V	–1		1	μA
Input logic high current	I_{IH}	VIN = 3.3V		33		μA
Pulldown resistance	R_{PD}	to GND		100		kΩ
~~Propagation delay~~	t_{PD}	Inx H to OUTx H change		0.2		μs
		Inx L to OUTx L change		1.0		μs
Time to sleep	t_{sleep}	Inputs low to sleep		1.2	2.0	ms
MOTOR DRIVER OUTPUTS (OUT1, OUT2)						
High-side FET on resistance	$R_{DS(ON)\_High}$	VM = 24 V, I = 1A, f_{PWM} = 25 kHz		260	300	mΩ
Low-side FET on resistance	$R_{DS(ON)\_Low}$	VM = 24 V, I = 1A, f_{PWM} = 25kHz		260	300	mΩ
Output dead time	t_{DEAD}			200		ns
CURRENT REGULATION						
ISEN gain	A_V	VREF = 2.5V	9.4	10	10.4	V/V
PWM off-time	t_{OFF}			30		μs
PWM blanking time	t_{BLANK}			3.2		μs
PROTECTION CIRCUITS						
VM undervoltage lockout	V_{UVLO_fall}	VM falls until UVLO triggers		5.8		V
	V_{UVLO_rise}	VM rises until operation recovers		6.0		V
VM undervoltage hysteresis	$V_{UV,\_HYS}$	Rising to falling threshold		200		mV
Overcurrent protection trip level	I_{OCP}			4.2		A
Overcurrent deglitch time	t_{OCP}			2.5		μs
Overcurrent retry time	t_{RETRY}			4		ms

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal shutdown temperature	T_{SD}			170		°C
Thermal shutdown hysteresis	T_{HYS}			40		°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D) \times (250°C/W)$.

Note 3: 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

Note 4: t_{ON} applies when the device initially powers up, and when it exits sleep mode.

OPERATION

Overview

The AT4950-MS devices are optimized 8-pin devices for driving brushed DC motors with 6.5V to 40 V and up to 3.6-A peak current. The integrated current regulation restricts motor current to a predefined maximum. Two logic inputs control the H-bridge driver, which consists of four N-channel MOSFETs that have a typical $R_{DS(ON)}$ of 0.52Ω (including one high-side and one low-side FET). A single-power input, VM, serves as both device power and the motor winding bias voltage. The integrated charge pump of the device boosts VM internally and fully enhances the high-side FETs. Motor speed can be controlledwith pulse-width modulation, at frequencies between 0 to 100 kHz. The devices have an integrated sleep mode that is entered by bringing both inputs low. An assortment of protection features prevents the device from being damaged if a system fault occurs.

Bridge Control

The AT4950-MS output consists of four N-channel MOSFETs that are designed to drive high current. These outputs are controlled by the two logic inputs IN1 and IN2 as listed in Table 1.

Table 1. H-Bridge Control

IN1	IN2	OUT1	OUT2	DESCRIPTION
0	0	High-Z	High-Z	Coast; H-bridge disabled to High-Z (sleep entered after 1.2ms)
0	1	L	H	Reverse (Current OUT2 →OUT1)
1	0	H	L	Forward (Current OUT1 →OUT2)
1	1	L	L	Brake; low-side slow decay

The inputs can be set to static voltages for 100% duty cycle drive, or they can be pulse-width modulated (PWM) for variable motor speed. When using PWM, switching between driving and braking typically works best. For example, to drive a motor forward with 50% of the maximum RPM, IN1 = 1 and IN2 = 0 during the driving period, and IN1 = 1 and IN2 = 1 during the other period. Alternatively, the coast mode (IN1 = 0, IN2 = 0) for fast current decay is also available. The input pins can be powered before VM is applied.

Sleep Mode

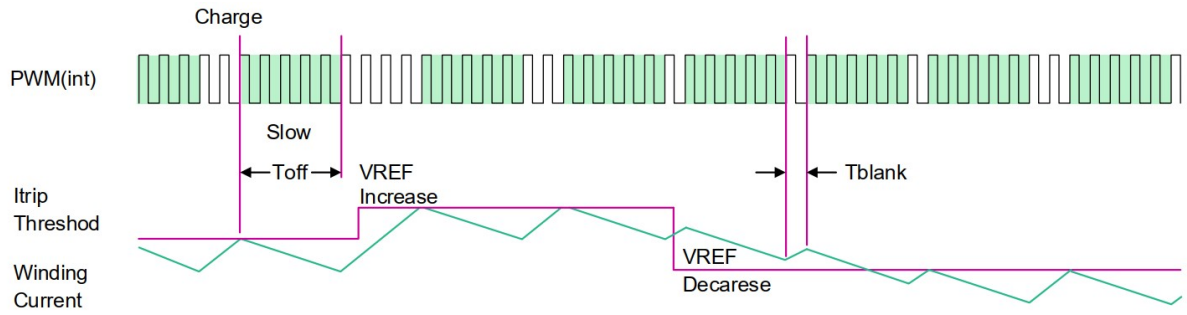
When the IN1 and IN2 pins are both low for time t_{SLEEP} (typically 1.2 ms), the AT4950-MS device enters a low-power sleep mode, where the outputs remain High-Z and the device uses $I_{VMSLEEP}$ (μA) of current. If the device is powered up while both inputs are low, it immediately enters sleep mode. After the IN1 or IN2 pins are high for at least 5 μs, the device is operational 45 μs (t_{ON}) later.

Current Regulation

In AT4950-MS, motor peak current can be limited by the analog reference input VREF and the resistance of external sense resistor on the ISEN pin according to the below equation:

$$I_{TRIP}\ (A) = \frac{VREF\ (V)}{A_V \times R_{ISEN}(\Omega)} = \frac{VREF\ (V)}{10 \times R_{ISEN}(\Omega)}$$

For example, if VREF =2.0V and a RISEN= 0.2Ω, the PWM current regulation mechanism will limits motor current to1.0A mps no matter how much load is applied. When ITRIP is reached, the H-bridge enforces the inductor current into slow decay path by enabling both low-side FETs, and it does this for a fixed off time, T_{OFF} (typically 30μs).



After Toff time passes, the H-bridge output is re-enabled according to the logic states of two inputs, IN1 and IN2, and motor winding current is charging until reaching another ITRIP event, this charge time is heavily depends on the VM voltage, the back-EMF of the motor, and the inductance of the motor.

VM under voltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the under voltage lockout threshold voltage, all FETs in the H-bridge will be disabled. Operation resumes when VM rises above the UVLO threshold.

Overcurrent Protection (OCP)

If the output current exceeds the OCP threshold, IOCP, for longer than t_{OCP}, all FETs in the H-bridge are disabled.

As to AT4950-MS, after a duration of t_{RETRY}, the H-bridge is re-enabled according to the state of the INx pins. If the overcurrent fault is still present, the cycle repeats; otherwise normal device operation resumes.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature has fallen to a safe level, operation automatically resumes.

Device Functional Modes

The AT4950-MS devices can be used in multiple ways to drive a brushed DC motor.

PWM With Current Regulation

This scheme uses all of the capabilities of the device. The I_{TRIP} current is set above the normal operating current, and high enough to achieve an adequate spin-up time, but low enough to constrain current to a desired level. Motor speed is controlled by the duty cycle of one of the inputs, while the other input is static. Brake or slow decay is typically used during the off-time.

PWM Without Current Regulation

If current regulation is not required, the ISEN pin should be directly connected to the PCB ground plane. The VREF voltage must still be 0.3V to 5 V, and larger voltages provide greater noise margin. This mode provides the highest-possible peak current which is up to 3.6 A for a few hundred milliseconds (depending on PCB characteristics and the ambient temperature). If current exceeds 3.6 A, the device might reach overcurrent protection (OCP) or over temperature shutdown (TSD). If that happens, the device disables and protects itself for about 4ms (t_{RETRY}) and then resumes normal operation.

Static Inputs with Current Regulation

The IN1 and IN2 pins can be set high and low for 100% duty cycle drive, and I_{TRIP} can be used to control the current of the motor, speed, and torque capability.

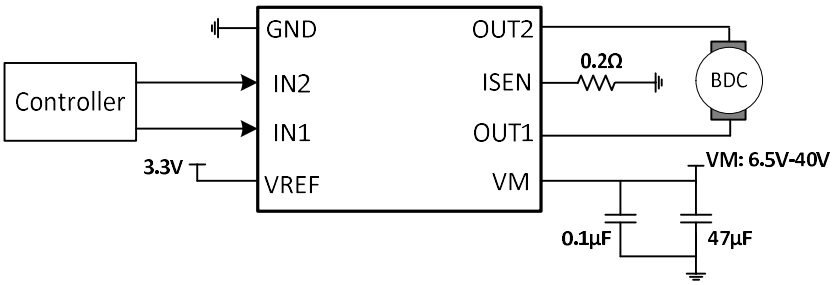
VM Control

In some systems, varying VM as a means of changing motor speed is desirable.

APPLICATION INFORMATION

Application information

The AT4950-MS devices are typically used to drive one brushed DC motor as below:



Block Diagram

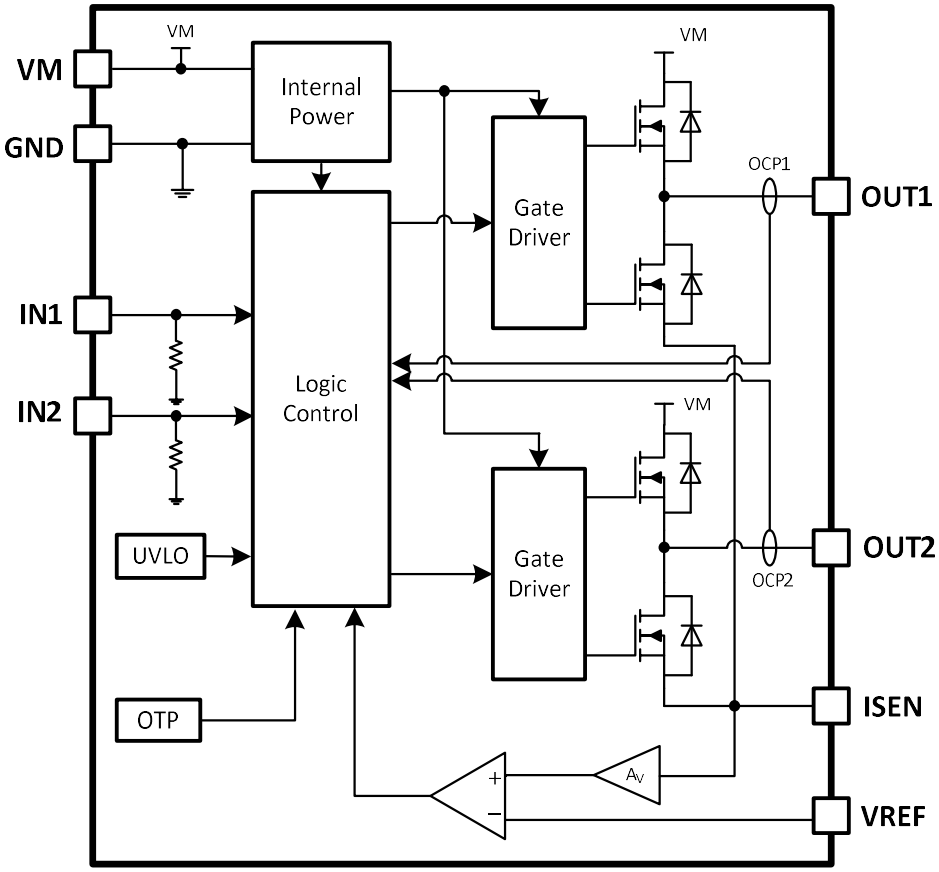
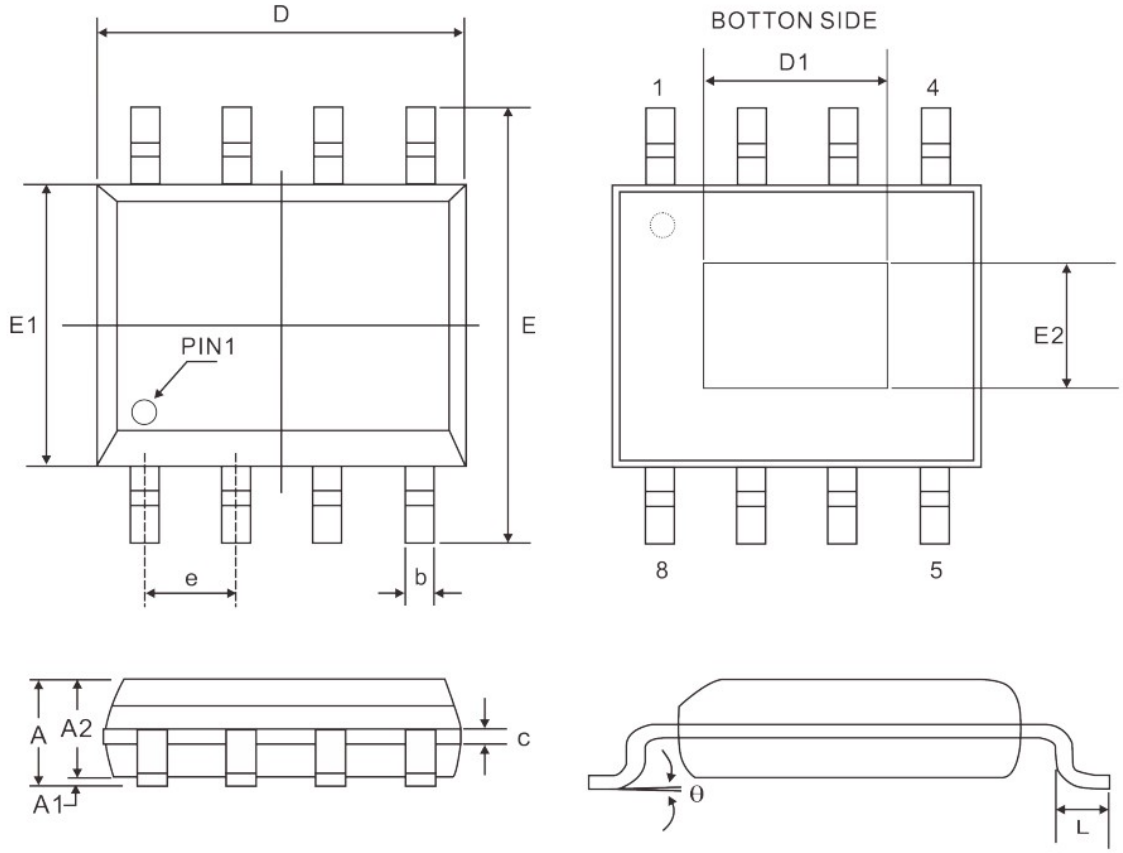


Figure 2. AT4950-MS **Block Diagram**

PACKAGE INFORMATION

ESOP8



Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A	-	-	1.70
A1	0.00	-	0.15
A2	1.25	-	-
b	0.31	-	0.51
c	0.10	-	0.25
e		1.27 BSC	
D		4.90 BSC	
D1	2.81	-	3.30
E		6.00 BSC	
E1		3.90 BSC	
E2	2.05	-	2.41
L	0.40	0.60	1.27
θ	0°	-	8°

Notes: Refer to JEDEC MS-012 BA

Attention

■ Any and all MSKSEMI Semiconductor products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your MSKSEMI Semiconductor representative nearest you before using any MSKSEMI Semiconductor products described or contained herein in such applications.

■ MSKSEMI Semiconductor assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specificationsof any andall MSKSEMI Semiconductor products described orcontained herein.

■ Specifications of any and all MSKSEMI Semiconductor products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer'sproducts orequipment.

■ MSKSEMI Semiconductor. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with someprobability. It is possiblethat these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits anderror prevention circuitsfor safedesign, redundant design, and structural design.

■ In the event that any or all MSKSEMI Semiconductor products(including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from theauthorities concerned in accordance with the above law.

■ No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of MSKSEMI Semiconductor.

■ Information (including circuit diagrams and circuit parameters) herein is for example only ; it is not guaranteed for volume production. MSKSEMI Semiconductor believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringementsof intellectual property rights or other rightsof third parties.

■ Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. Whendesigning equipment, referto the "Delivery Specification" for the MSKSEMI Semiconductor productthat you intend to use.