

**MOSFET Silicon N-Channel MOS****1. Applications**

Synchronous rectification in SMPS,  
Hard switching and High speed circuit  
DC/DC in telecoms and industrial

**2. Features**

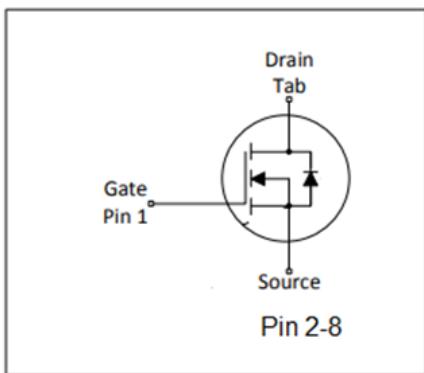
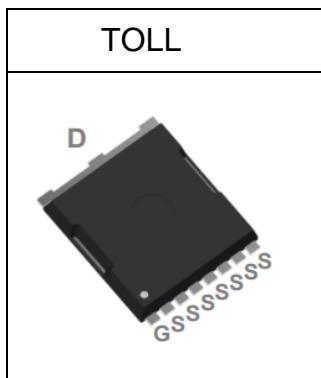
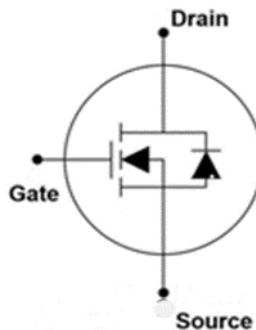
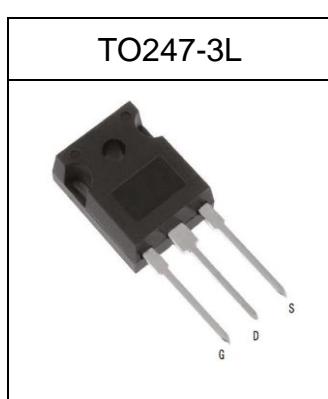
Low drain-source on-resistance:  
 $R_{DS(on)}$  TOLL = 1.6mΩ (typ.)  
 $R_{DS(on)}$  TO247 = 2.1mΩ (typ.)  
High speed power switching  
Enhanced body diode dv/dt capability  
Enhanced avalanche ruggedness

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$ @ $T_{j,max}$	100	V
$R_{DS(on),max}$ TOLL	2.0	mΩ
$R_{DS(on),max}$ TO247	2.5	mΩ
$Q_{g,typ}$	213	nC
$I_{D,pulse}$	1000	A

**3. Packaging and Internal Circuit**

Part Name	Package	Marking
AUR020N10	TOLL-8L	AUR020N10
AUW025N10	TO247-3L	AUW025N10

*Released*

## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$		-	305	A	$T_c=25^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,\text{pulse}}$	-	-	1000	A	$T_c=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	1176	mJ	$T_c=25^\circ\text{C}, VDD=50\text{V}, I_{av}=68.6\text{A}, L=0.5\text{mH}, RG=25\Omega$
Avalanche current, single pulse	$I_{AR}$	-	-	68.6	A	$T_c=25^\circ\text{C}, VDD=50\text{V}, L=0.5\text{mH}, RG=25\Omega$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Power dissipation	$P_{tot}$	-	-	375	W	$T_c=25^\circ\text{C}$
Storage temperature	$T_{stg}$	-55	-	150	°C	
Operating junction temperature	$T_j$	-55	-	150	°C	
Soldering Temperature Distance of 1.6mm from case for 10s	$T_L$			260	°C	

<sup>1)</sup>Limited by  $T_{j,\text{max}}$ . Maximum Duty Cycle D = 0.50

<sup>2)</sup>Pulse width  $t_p$  limited by  $T_{j,\text{max}}$

<sup>3)</sup>Identical low side and high side switch with identical RG

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## 2 Thermal characteristics

**Table Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	0.33	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	48	°C/W	device on PCB, minimal footprint

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### 3 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	100	-	-	V	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$
Gate threshold voltage	$V_{(\text{GS})\text{th}}$	2.5	3.1	4.5	V	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$
Zero gate voltage drain current	$I_{\text{DSS}}$	-	-	1	$\mu\text{A}$	$V_{\text{DS}}=100\text{V}, V_{\text{GS}}=0\text{V}, T_j=25^\circ\text{C}$
Gate-source leakage current	$I_{\text{GSS}}$	-	-	$\pm 100$	nA	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$
Drain-source on-state resistance(TOLL)	$R_{\text{DS}(\text{on})}$	-	1.6	2.0	$\text{m}\Omega$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=20\text{A}, T_j=25^\circ\text{C}$
Drain-source on-state resistance(TO247)	$R_{\text{DS}(\text{on})}$	-	2.1	2.5	$\text{m}\Omega$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=20\text{A}, T_j=25^\circ\text{C}$
Gate resistance (Intrinsic)	$R_{\text{G}}$	-	1.6	-	$\Omega$	$f=1\text{MHz}$ , open drain
Transconductance	$G_{\text{fs}}$	-	138.4	-	S	$V_{\text{DS}}=5\text{V}, I_{\text{D}}=50\text{A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{\text{iss}}$	-	14994	-	pF	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=35\text{V}, f=1\text{MHz}$
Output capacitance	$C_{\text{oss}}$	-	1577	-	pF	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=35\text{V}, f=1\text{MHz}$
Reverse transfer capacitance	$C_{\text{rss}}$	-	477	-	pF	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=35\text{V}, f=1\text{MHz}$
Turn-on delay time	$t_{\text{d}(\text{on})}$	-	35.5	-	ns	$V_{\text{DD}}=50\text{V}, V_{\text{GS}}=10\text{V}, I_{\text{D}}=20\text{A}, R_{\text{G}}=3\Omega$
Rise time	$t_{\text{r}}$	-	57.2	-	ns	$V_{\text{DD}}=50\text{V}, V_{\text{GS}}=10\text{V}, I_{\text{D}}=20\text{A}, R_{\text{G}}=3\Omega$
Turn-off delay time	$t_{\text{d}(\text{off})}$	-	112	-	ns	$V_{\text{DD}}=50\text{V}, V_{\text{GS}}=10\text{V}, I_{\text{D}}=20\text{A}, R_{\text{G}}=3\Omega$
Fall time	$t_{\text{f}}$	-	62	-	ns	$V_{\text{DD}}=50\text{V}, V_{\text{GS}}=10\text{V}, I_{\text{D}}=20\text{A}, R_{\text{G}}=3\Omega$

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{\text{gs}}$	-	60.6	-	nC	$V_{\text{DD}}=50\text{V}, I_{\text{D}}=20\text{A}, V_{\text{GS}}=0 \text{ to } 10\text{V}$
Gate to drain charge	$Q_{\text{gd}}$	-	50.7	-	nC	$V_{\text{DD}}=50\text{V}, I_{\text{D}}=20\text{A}, V_{\text{GS}}=0 \text{ to } 10\text{V}$
Gate charge total	$Q_{\text{g}}$	-	213	-	nC	$V_{\text{DD}}=50\text{V}, I_{\text{D}}=20\text{A}, V_{\text{GS}}=0 \text{ to } 10\text{V}$
Gate plateau voltage	$V_{\text{plateau}}$	-	4.72	-	V	$V_{\text{DD}}=50\text{V}, I_{\text{D}}=20\text{A}, V_{\text{GS}}=0 \text{ to } 10\text{V}$

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**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	0.67	1.2	V	$V_{GS}=0V$ , $I_F=1A$ , $T_j=25^\circ C$
Reverse recovery time	$t_{rr}$	-	84.44	-	ns	$V_R=50V$ , $I_F=20A$ , $dI_F/dt=100A/\mu s$
Reverse recovery charge	$Q_{rr}$	-	236	-	nC	$V_R=50V$ , $I_F=20A$ , $dI_F/dt=100A/\mu s$
Peak reverse recovery current	$I_{frm}$	-	4.31	-	A	$V_R=50V$ , $I_F=20A$ , $dI_F/dt=100A/\mu s$

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## 4 Electrical characteristics diagram

Diagram 1: Typ. Output characteristics	Diagram 2: Typ. transfer characteristics
<p>Diagram 1 shows typical output characteristics curves for the AUR020N10 and AUW025N10 MOSFETs. The Y-axis is Drain Current (<math>I_{DS}</math>) in Amperes (A), ranging from 0 to 300. The X-axis is Drain-to-source voltage (<math>V_{DS}</math>) in Volts (V), ranging from 0 to 6. Five curves are plotted for different Gate-to-source voltages (<math>V_{GS}</math>): 10V (orange), 6V (blue), 5.5V (purple), 5V (green), and 4.5V (red). The curves show saturation current increasing with <math>V_{GS}</math> and decreasing with <math>V_{DS}</math>.</p>	<p>Diagram 2 shows typical transfer characteristics curves for the devices. The Y-axis is Drain Current (<math>I_D</math>) in Amperes (A), ranging from 0 to 20. The X-axis is Gate-to-source voltage (<math>V_{GS}</math>) in Volts (V), ranging from 0 to 8. Two curves are shown for Junction Temperature (<math>T_J</math>): 25°C (blue) and 125°C (red). The curves show a sharp increase in current as <math>V_{GS}</math> approaches the threshold voltage, with higher <math>T_J</math> resulting in lower threshold voltage.</p>
$I_D = f(V_{DS})$ ; $T_j = 25^\circ\text{C}$ ; parameter: $V_{GS}$	$I_D = f(V_{GS})$ ; $V_{DS} = 5\text{V}$ ; parameter: $T_j$
Diagram 3: Typ. On-Resistance vs. ID (TOLL)	Diagram 4: Typ. Rdson – Junction Temperature
<p>Diagram 3 shows typical on-resistance (<math>R_{DS(on)}</math>) in milliohms (mΩ) versus drain current (<math>ID</math>) in Amperes (A) for the TOLL condition. The Y-axis ranges from 0.00 to 5.00 mΩ, and the X-axis ranges from 0 to 20 A. A single black curve is shown, labeled with a red "Releasoo" watermark. The resistance remains relatively constant around 1.5 mΩ across the current range.</p>	<p>Diagram 4 shows the normalization of on-resistance (<math>R_{DS(on)}</math>) versus junction temperature (<math>T_j</math>) in degrees Celsius (°C). The Y-axis is Normalization <math>R_{DS(on)}</math>, ranging from 0.6 to 2.0. The X-axis is <math>T_j</math> in °C, ranging from -50 to 150. A single black curve shows that as <math>T_j</math> increases, the normalized on-resistance increases linearly from approximately 0.65 at -50°C to about 1.8 at 150°C.</p>
$R_{DS(on)} = f(ID)$ ; $T_j = 25^\circ\text{C}$ ; parameter: $V_{GS} = 10\text{V}$ (TOLL)	$(R_{DS(on)}) = f(T_j)$ ; $V_{GS} = 10\text{V}$ / $I_D = 20\text{A}$
Diagram 5: Typ. Body-Diode Characteristics	Diagram 6: Typ. Capacitance vs. Vds
<p>Diagram 5 shows typical body-diode characteristics for the devices. The Y-axis is Drain current (<math>I_{SD}</math>) in Amperes (A), on a logarithmic scale from 0.001 to 10. The X-axis is Drain-to-source voltage (<math>V_{SD}</math>) in Volts (V), ranging from 0.0 to 1.0. Two curves are shown for Junction Temperature (<math>T_j</math>): 125°C (green) and 25°C (blue). The current increases exponentially with <math>V_{SD}</math> and is higher at higher temperatures.</p>	<p>Diagram 6 shows typical capacitance versus drain-to-source voltage (<math>V_{DS}</math>) for the devices. The Y-axis is Capacitance in picofarads (pF), on a logarithmic scale from 100 to 100,000. The X-axis is <math>V_{DS}</math> in Volts (V), ranging from 0 to 100. A blue curve is shown for <math>f = 1\text{MHz}</math> and <math>V_{GS} = 0\text{V}</math>. The capacitance is high at low <math>V_{DS}</math> (around 10,000 pF) and decreases as <math>V_{DS}</math> increases, leveling off at approximately 1,000 pF for <math>V_{DS} &gt; 40\text{V}</math>.</p>
$I_f = f(V_{DS})$ ; parameter: $T_j$	$C = f(V_{DS})$ ; $V_{GS} = 0\text{V}$ ; $f = 1\text{MHz}$

Diagram 7: Typ. Drain-source breakdown voltage

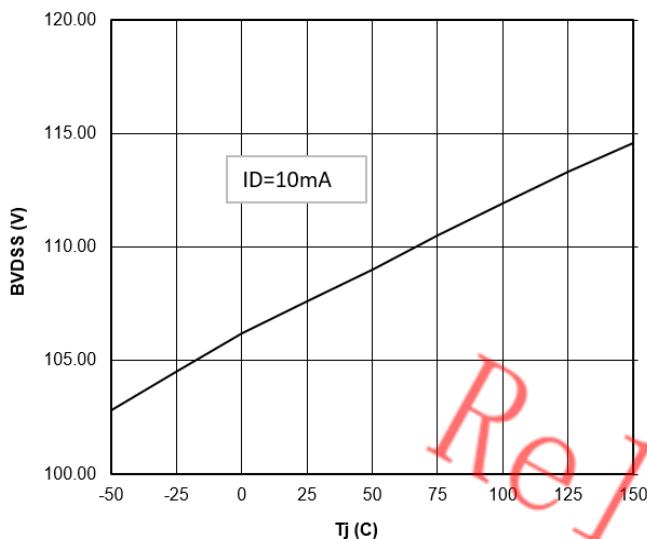
 $V_{BR(DSS)}=f(T_J); I_D=10\text{mA}$ 

Diagram 8: Typ. Threshold voltage

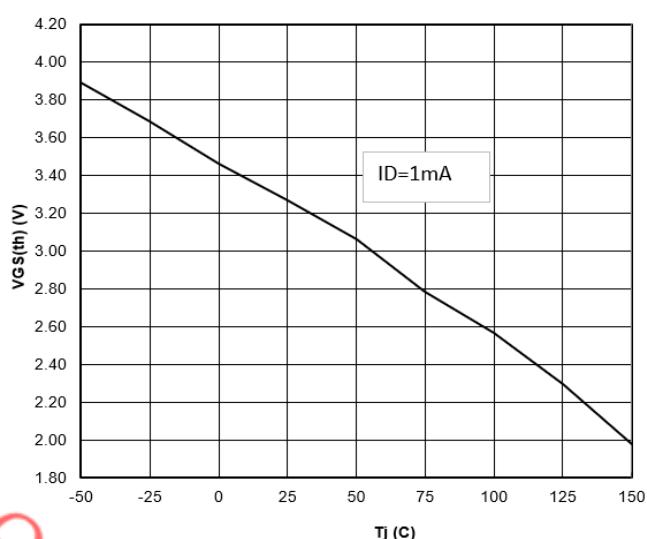
 $V_{th}=f(T_J)$ 

Diagram 9: Typ. Gate charge

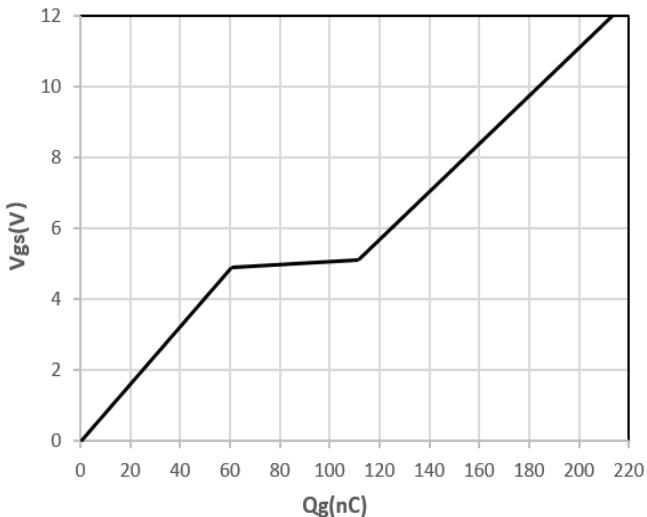
 $V_{GS}=f(Q_{gate}); I_D=20\text{A pulsed}; \text{parameter: } V_{DD}$ 

Diagram 10: Typ. Maximum Safe Operating Area

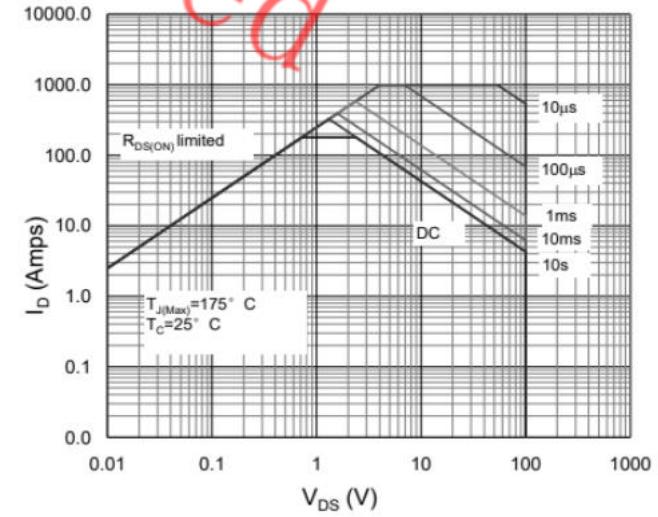
 $I_D=f(V_{DS}); T_C=25^\circ\text{C}; D=0; \text{parameter tp}$ 

Diagram 11: Typ. Power Dissipation

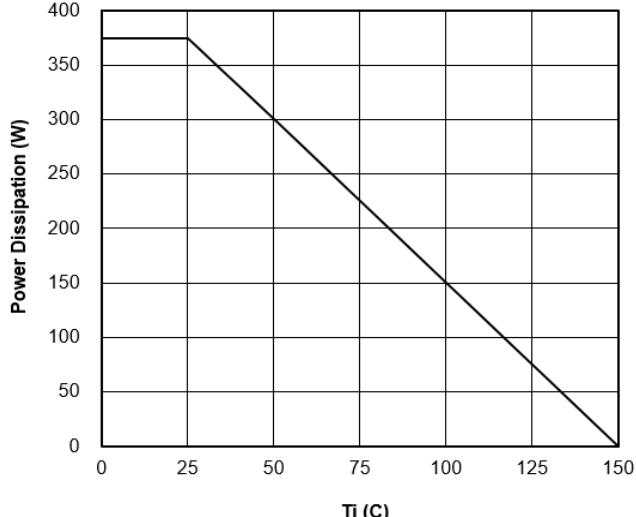
 $P_{tot}=f(T_C);$ 

Diagram 12: Typ. Drain Current De-rating

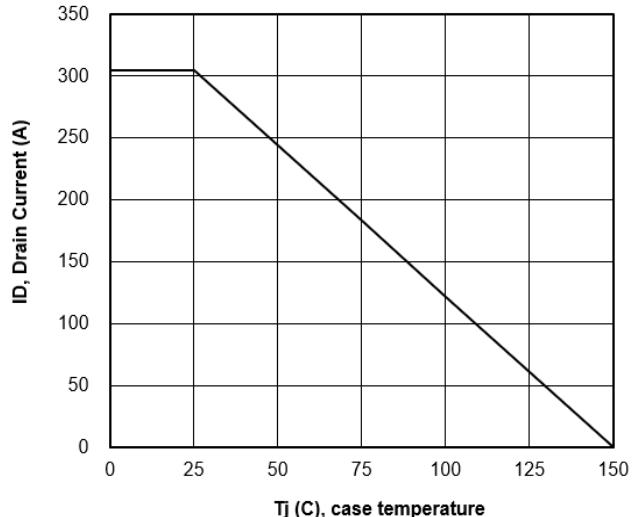
 $I_d=f(T_C);$

Diagram 13: Typ. On-Resistance vs. ID (TO247)

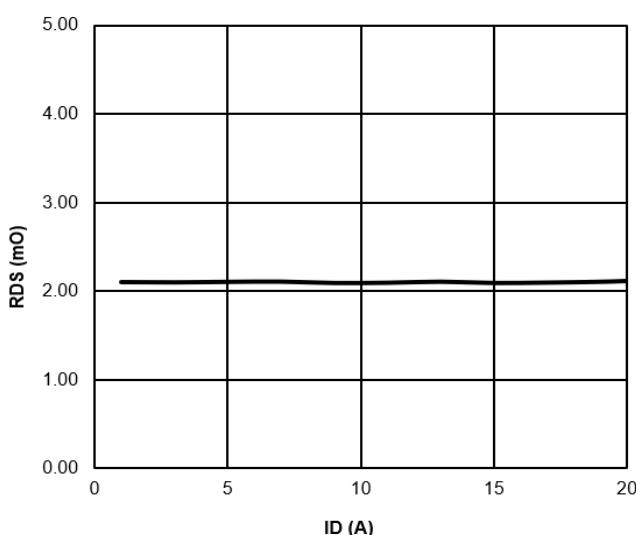
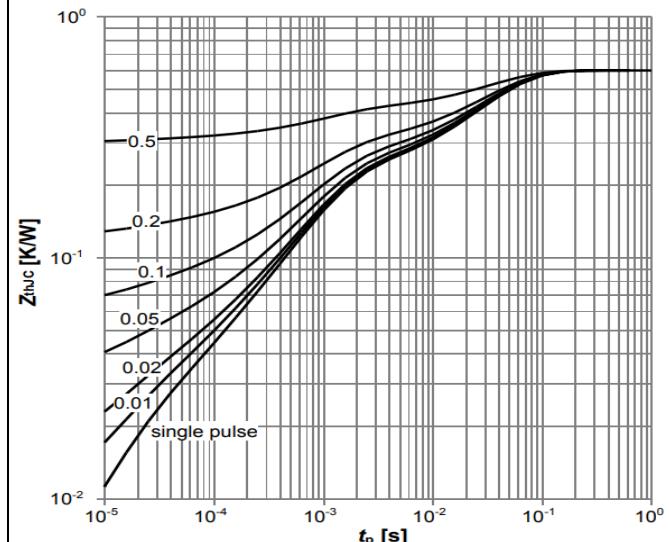

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}; \text{ parameter: } V_{GS} = 10\text{V (TO247)}$ 

Diagram 14: Typ. Max. transient thermal impedance


 $Z_{thJC} = f(t_p); \text{ parameter: } D = t_p/T$ 

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## 5 Test Circuits

**Table 8 Diode characteristics**

Test circuit for diode characteristics	Diode recovery waveform
 $R_{G1} = R_{G2}$	

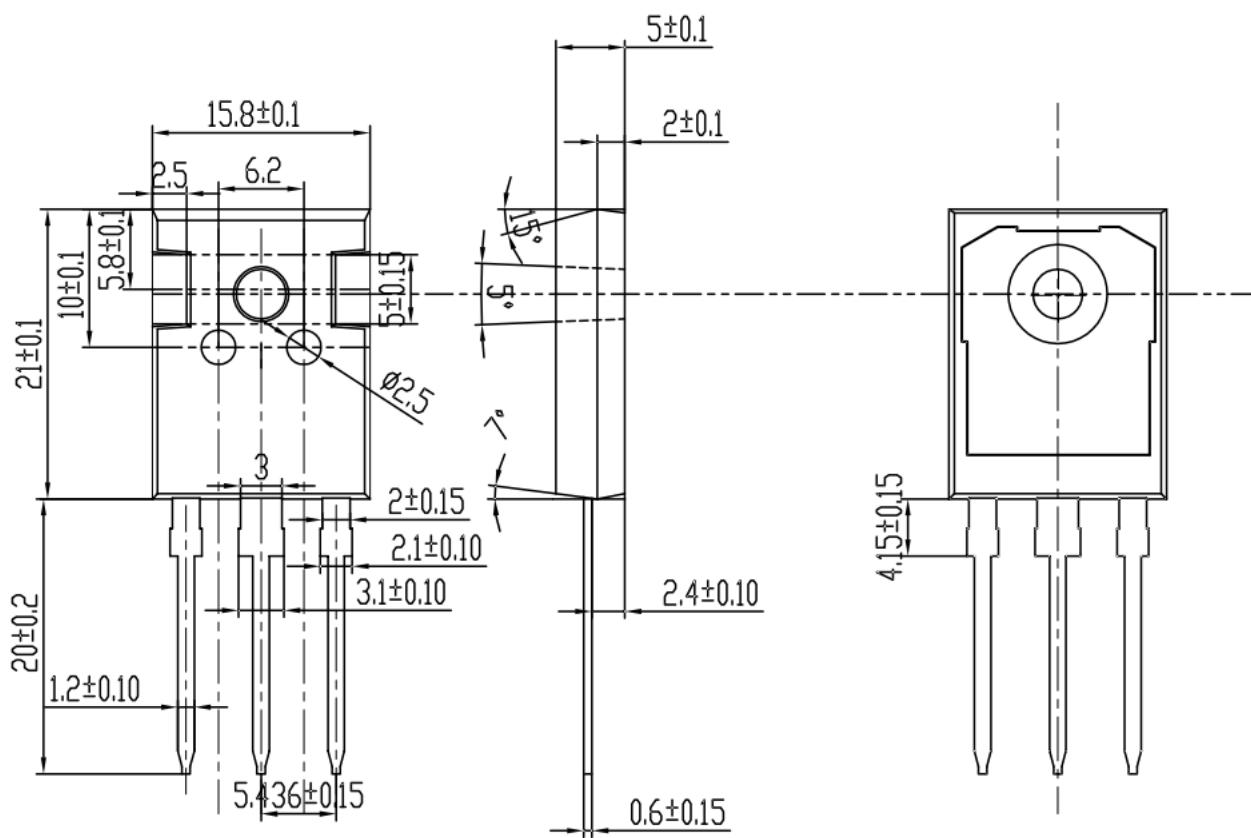
**Table 9 Switching times**

Switching times test circuit for inductive load	Switching times waveform

**Table 10 Unclamped inductive load**

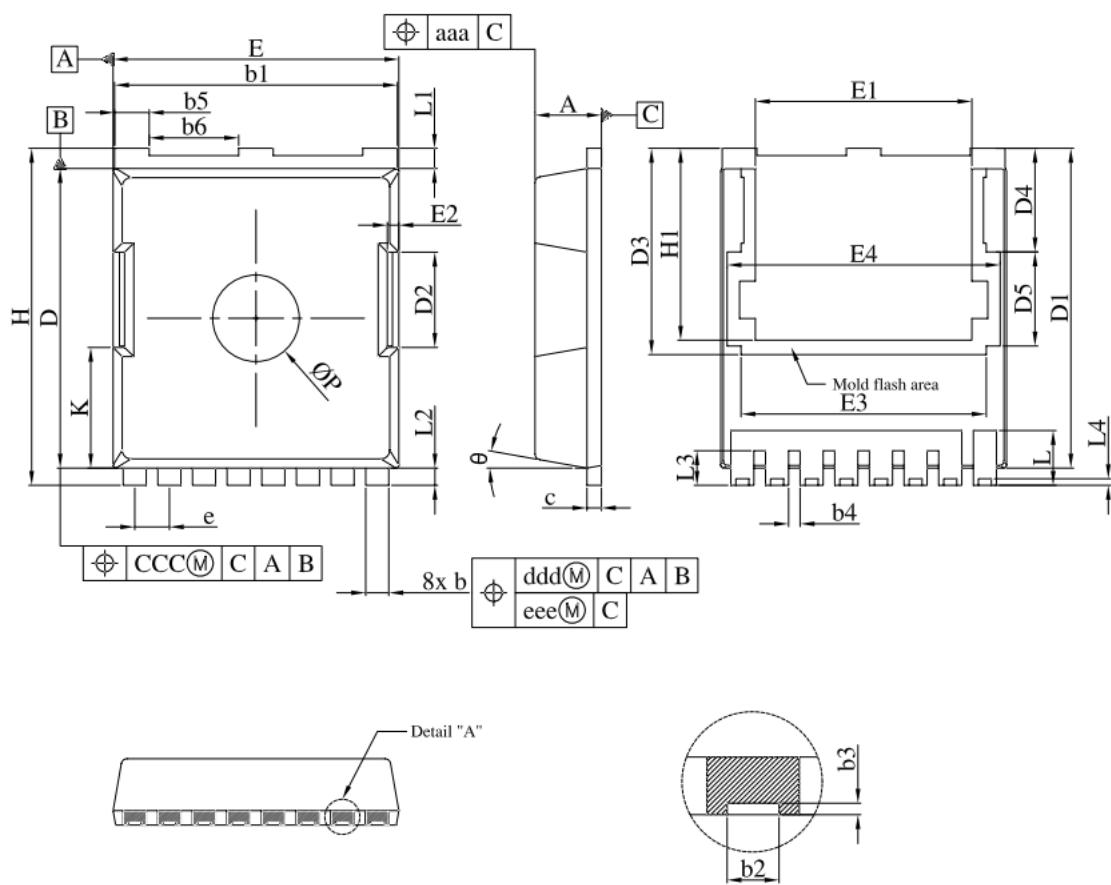
Unclamped inductive load test circuit	Unclamped inductive waveform

## 6 Package Outlines



Outline PG-T0247-3L(HT)

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SYMBOL	COMMON		
	MILLIMETER		
	MIN.	NOMINAL	MAX.
A	2.20	2.30	2.40
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.36	0.45	0.55
b3	0.05	0.100	/
b4	0.30	0.40	0.50
b5	1.10	1.20	1.30
b6	3.00	3.10	3.20
c	0.40	0.50	0.60
D	10.28	10.38	10.55
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3		7.15	
D4		3.59	
D5		3.26	
e	1.10	1.20	1.30
E	9.80	9.90	10.00
E1	7.40	7.50	7.60
E2	0.30	0.40	0.50
E3		8.50	
E4		9.46	
H	11.50	11.68	11.85
H1	6.55	6.65	6.75
K	4.08	4.18	4.28
L	1.60	1.90	2.10
L1	0.50	0.70	0.90
L2	0.50	0.60	0.70
L3	1.00	1.20	1.30
L4	0.13	0.23	0.33
P	2.85	3.00	3.15
θ		10° REF	
aaa		0.20	
ccc		0.20	
ddd		0.25	
eee		0.20	

Outline PG-TOLL(JQ)

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**Revision History**

Revision	Date	Subjects (major changes since last revision)
1.0	2023-12-11	Preliminary version

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