MOSFET Silicon N-Channel MOS

1. Applications

Single-ended flyback or two-transistor forward topologies.
PC power, PD Adaptor, LCD & PDP TV and LED lighting.

2. Features

Low drain-source on-resistance: RDS(ON) = 240mΩ (typ.)
Easy to control Gate switching
Enhancement mode: Vth = 2.8 to 4.2 V

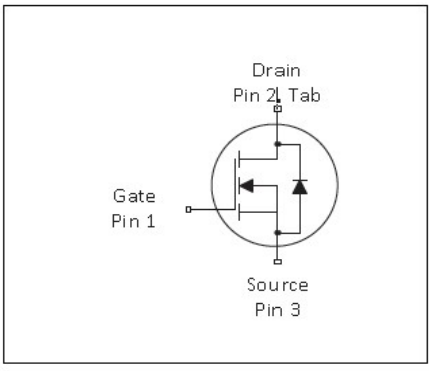
Table 1 Key Performance Parameters

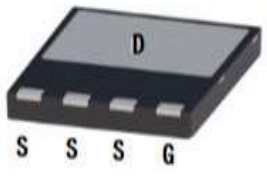
Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	700	V
$R_{DS(on),max}$	280	mΩ
$Q_{g,typ}$	19.4	nC
$I_{D,pulse}$	45	A
Body diode dv/dt	50	V/ns

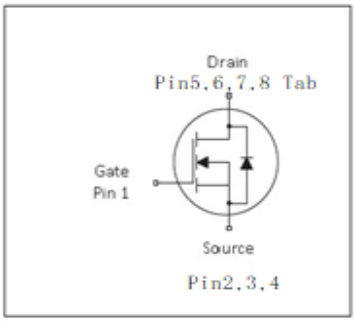
3. Packaging and Internal Circuit

Part Name	Package	Marking
ASA65R280E	TO220F	ASA65R280E
ASD65R280E	TO252	ASD65R280E
ASM65R280E	DFN8X8	ASM65R280E

TO220F	TO252
	



DFN8X8




1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D		-	15	A	T_C=25°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	45	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	120	mJ	Tc=25°C,VDD=50V, Iav=4.9A, L=10mH, RG=25Ω
Avalanche current, single pulse	I_{AR}	-	-	4.9	A	Tc=25°C,VDD=50V, L=10mH, RG=25Ω
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation (TO220F)	P_{tot}	-	-	33	W	T_C=25°C
Power dissipation (TO252&DFN8X8)	P_{tot}	-	-	126	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	
Operating junction temperature	T_j	-55	-	150	°C	
Soldering Temperature Distance of 1.6mm from case for 10s	T_L			260	°C	
Reverse diode dv/dt3)	dv/dt	-	-	15	V/ns	VDS=0...400V, ISD<=58A, Tj=25°C

[1] Limited by $T_{j,max}$. Maximum Duty Cycle D = 0.50
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Thermal characteristics (TO220F)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.8	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	device on PCB, minimal footprint

Thermal characteristics (TO252&DFN8X8)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.99	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{(GS)th}$	2.8	3.5	4.2	V	V_{DS}=V_{GS}, I_D=250uA
Zero gate voltage drain current	I_{DSS}	-	-	1	uA	V_{DS}=650V, V_{GS}=0V, T_j=25°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=30V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	240	280	mΩ	V_{GS}=10V, I_D=5.5A, T_j=25°C
Gate resistance (Intrinsic)	R_G	-	4.0	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	953.8	-	pF	V_{GS}=0V, V_{DS}=50V, f=1MHz
Output capacitance	C_{oss}	-	40.67	-	pF	V_{GS}=0V, V_{DS}=50V, f=1MHz
Reverse transfer capacitance	C_{rss}	-	1.21	-	pF	V_{GS}=0V, V_{DS}=50, f=1MHz
Turn-on delay time	$t_{d(on)}$	-	7.7	-	ns	V_{DD}=400V,V_{GS}=10V,I_D=8A, R_G=2Ω
Rise time	t_r	-	7.5	-	ns	V_{DD}=400V,V_{GS}=10V,I_D=8A, R_G=2Ω
Turn-off delay time	$t_{d(off)}$	-	24.44	-	ns	V_{DD}=400V,V_{GS}=10V,I_D=8A, R_G=2Ω
Fall time	t_f	-	8.4	-	ns	V_{DD}=400V,V_{GS}=10V,I_D=8A, R_G=2Ω

Table 6 Gate charge characteristics

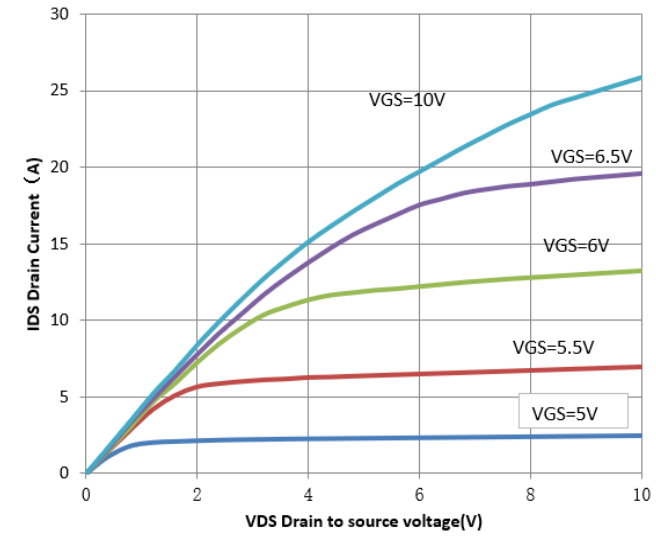
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	4.83	-	nC	V_{DD}=400V, I_D=8A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	7.08	-	nC	V_{DD}=400V, I_D=8A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	19.4	-	nC	V_{DD}=400V, I_D=8A, V_{GS}=0 to 10V
Gate plateau voltage	$Vplateau$	-	5.6	-	V	V_{DD}=400V, I_D=8A, V_{GS}=0 to 10V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.73	-	V	V_{GS}=0V, I_F=1A, T_j=25°C
Reverse recovery time	t_{rr}	-	237.7	-	ns	V_R=400V, I_F=8A, di_F/dt=100A/µs
Reverse recovery charge	Q_{rr}	-	2.604	-	uC	V_R=400V, I_F=8A, di_F/dt=100A/µs
Peak reverse recovery current	I_{rrm}	-	23.32	-	A	V_R=400V, I_F=8A, di_F/dt=100A/µs

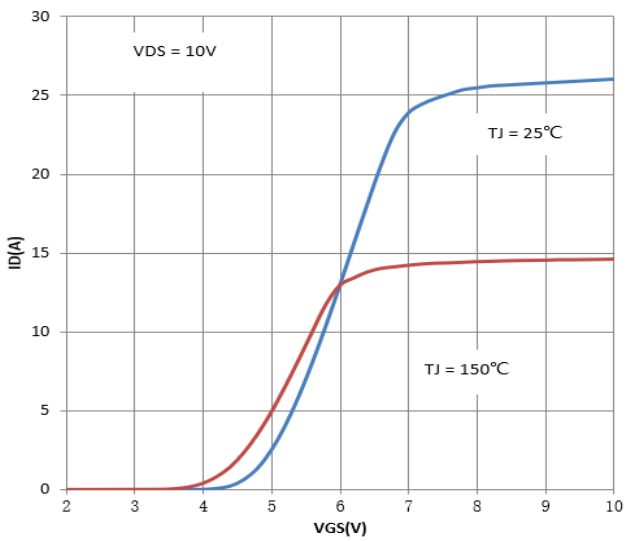
4 Electrical characteristics diagram

Diagram 1: Typ. Output characteristics



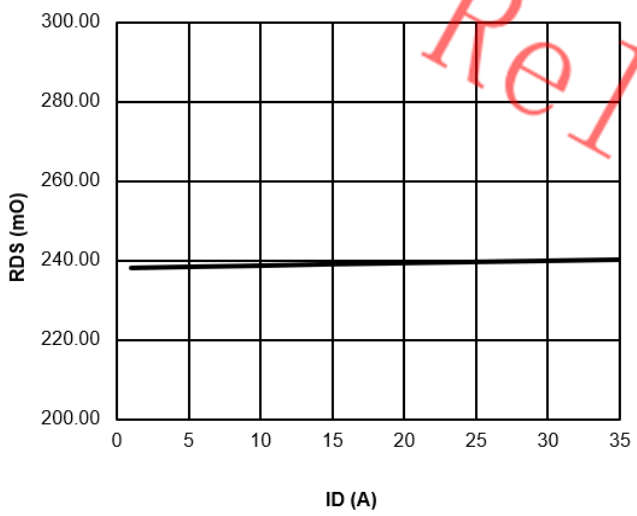
I_D=f(V_{DS});T_j=25 °C; parameter: V_{GS}

Diagram 2: Typ. transfer characteristics



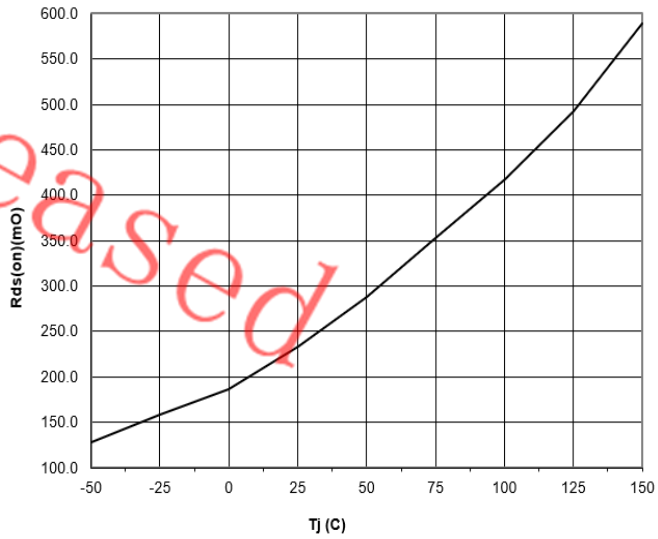
ID=f(VGS); VDS=10V; parameter:Tj

Diagram 3: Typ. On-Resistance vs. ID



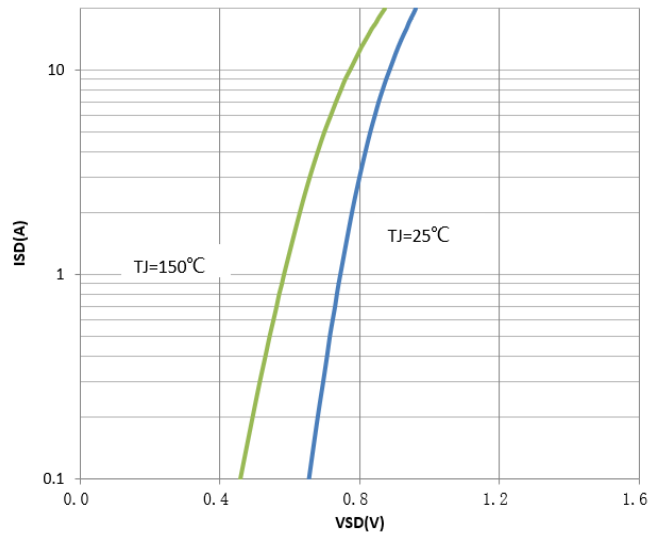
$R_{DS(on)}$=f(I_D); T_j=25°C; parameter:V_{GS}=10V

Diagram 4: Typ. Rdson – Junction Temperature



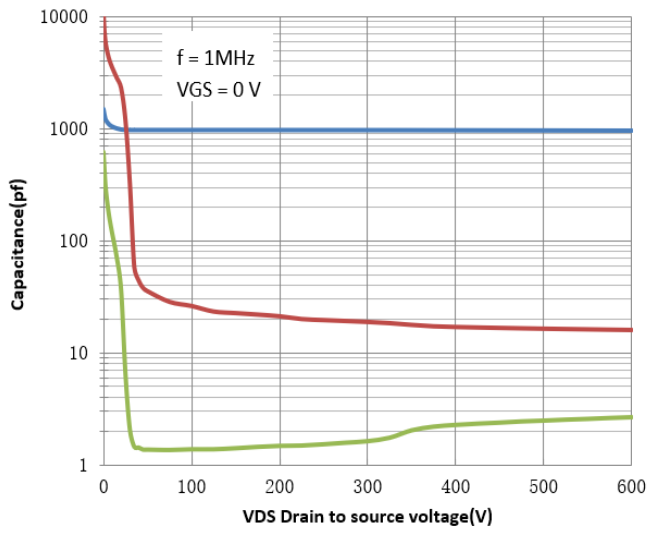
$R_{ds(on)}$=f(T_j);Vgs=10V/I_D=5.5A

Diagram 5: Typ. Body-Diode Characteristics



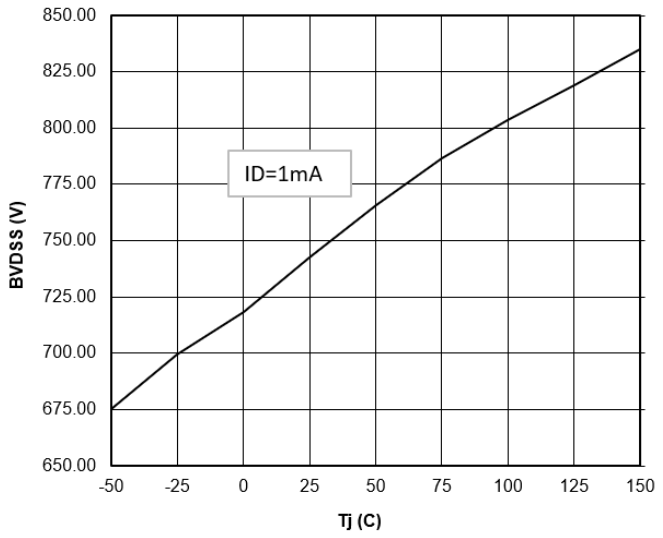
I_F=f(V_{DS});parameter: Tj

Diagram 6: Typ. Capacitance vs. Vds



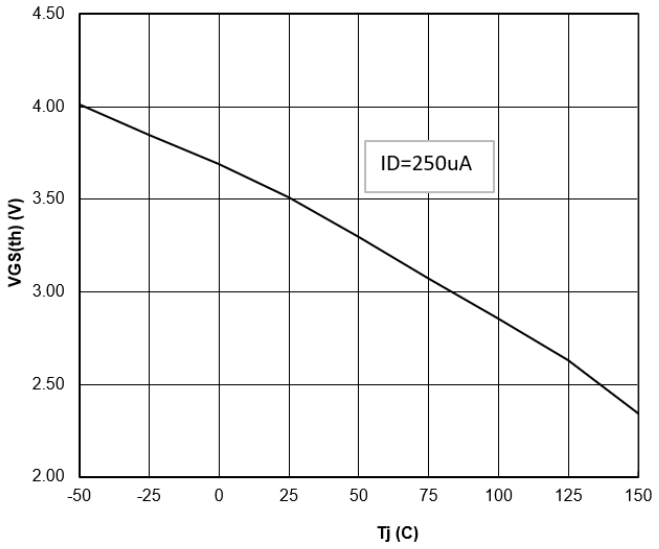
C=f(V_{DS});V_{GS}=0V; f=1MHz

Diagram 7: Typ. Drain-source breakdown voltage



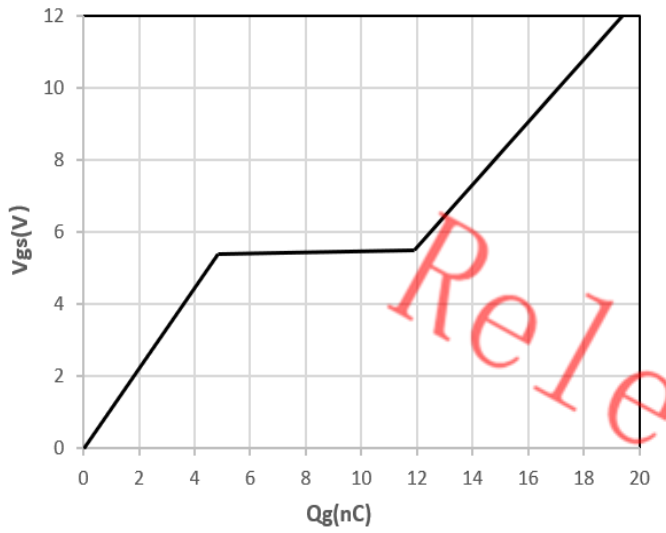
$V_{BR(DSS)}$=f(T_j); I_D=1mA

Diagram 8: Typ. Threshold voltage



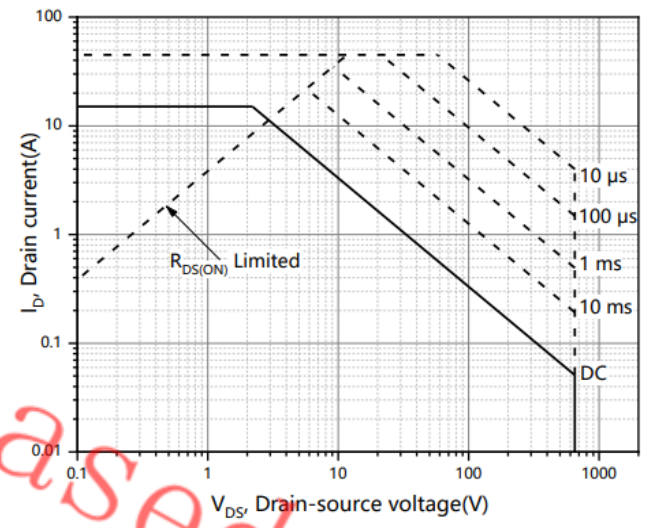
Vth=f(T_C);

Diagram 9: Typ. Gate charge



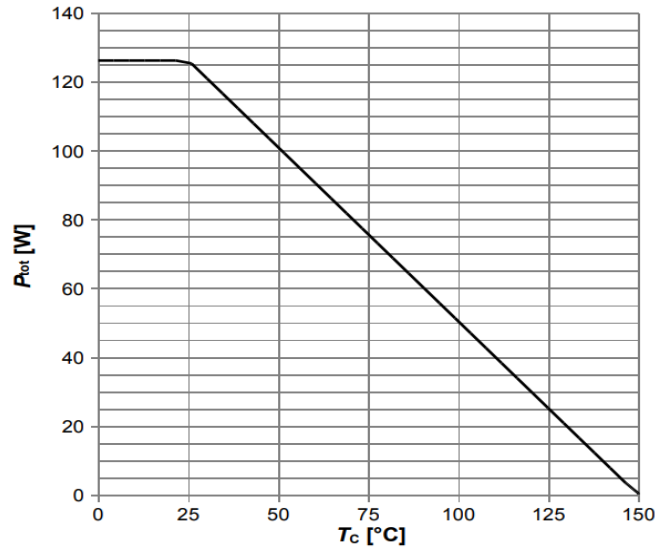
V_{GS}=f(Q_{gate});I_D=50A pulsed; parameter: V_{DD}

Diagram 10: Typ. Maximum Safe Operating Area



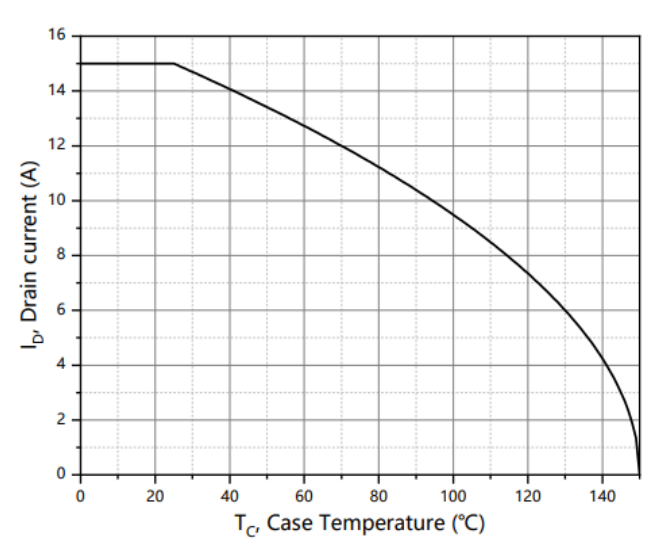
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter tp

Diagram 11: Typ. Power Dissipation

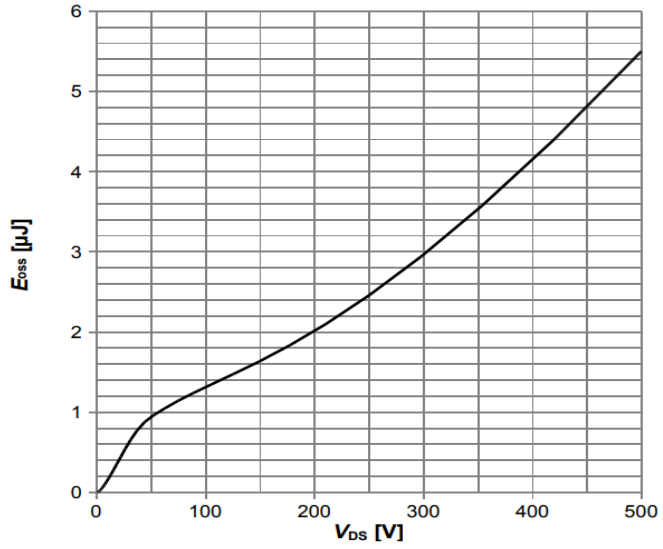
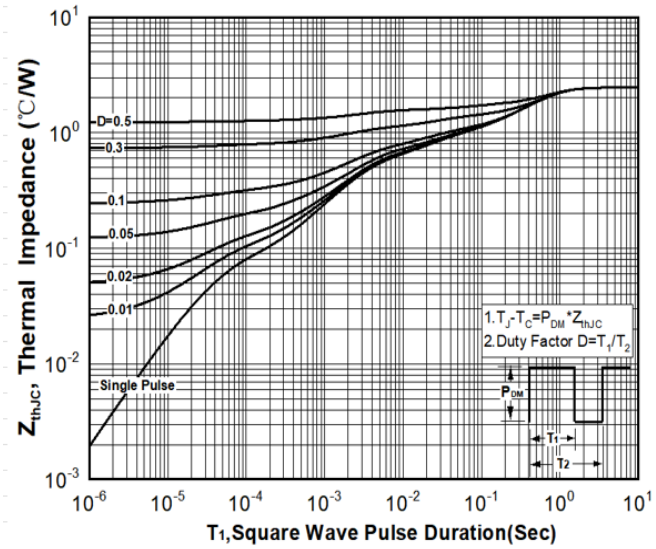


P_{tot}=f(T_C); TO252

Diagram 12: Typ. Drain Current De-rating



Id=f(T_C);

Diagram 13: Typ. Coss stored energy	Diagram 14: Typ. Max. transient thermal impedance
	
$E_{oss}=f(V_{DS})$	$Z_{thJC}=f(t_P)$; parameter: $D=t_p/T$

5 Test Circuits

Table 8 Diode characteristics

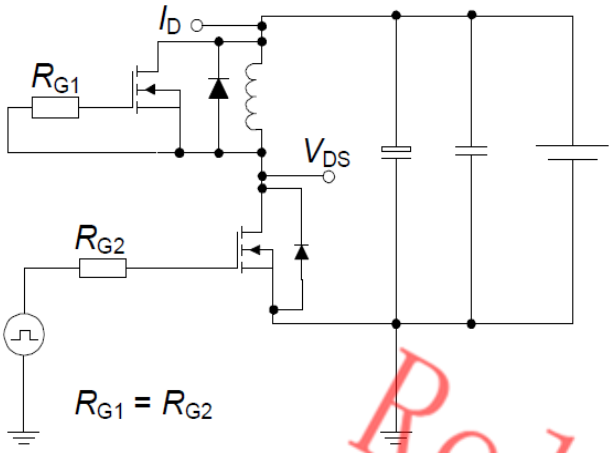
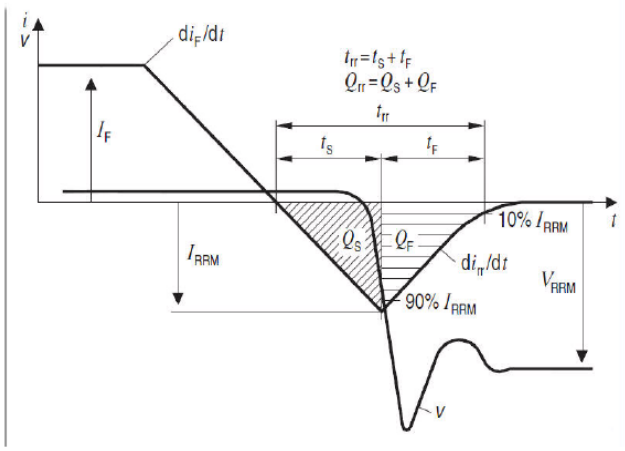
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

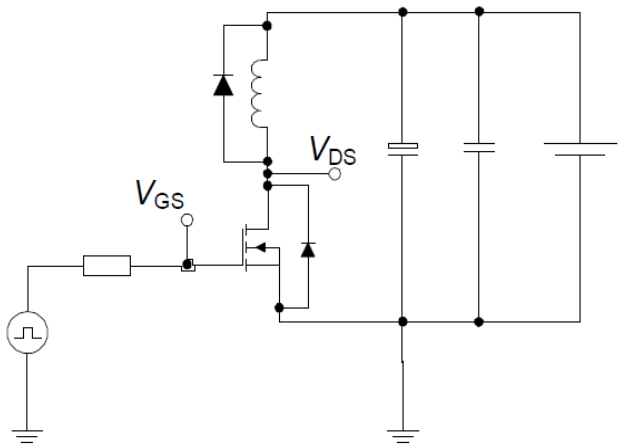
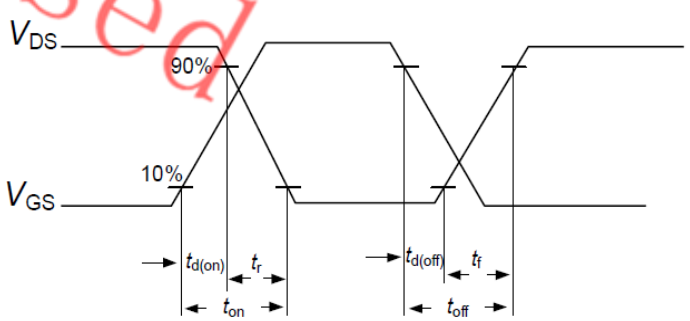
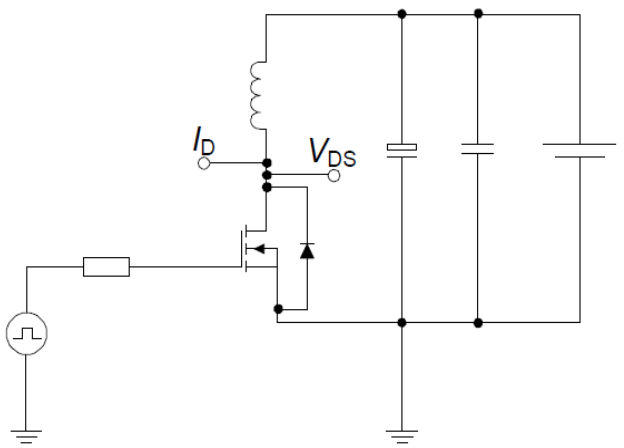
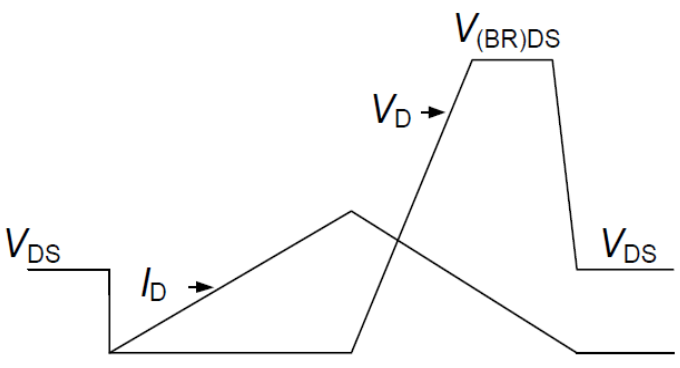
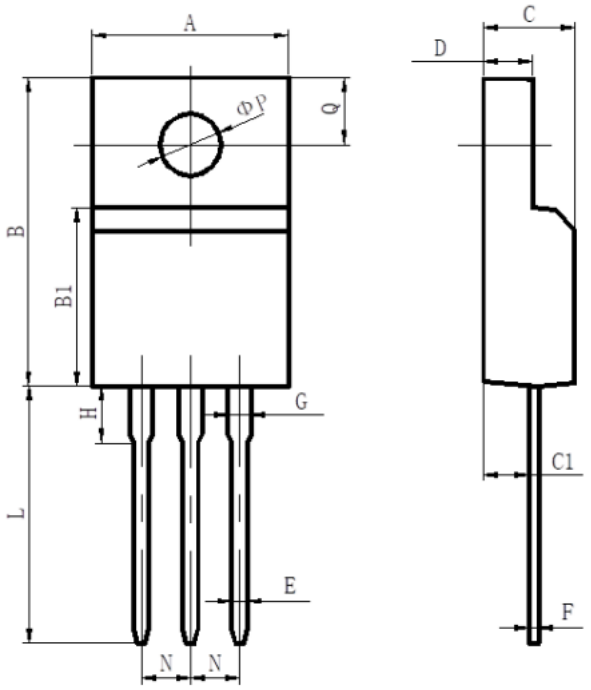
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

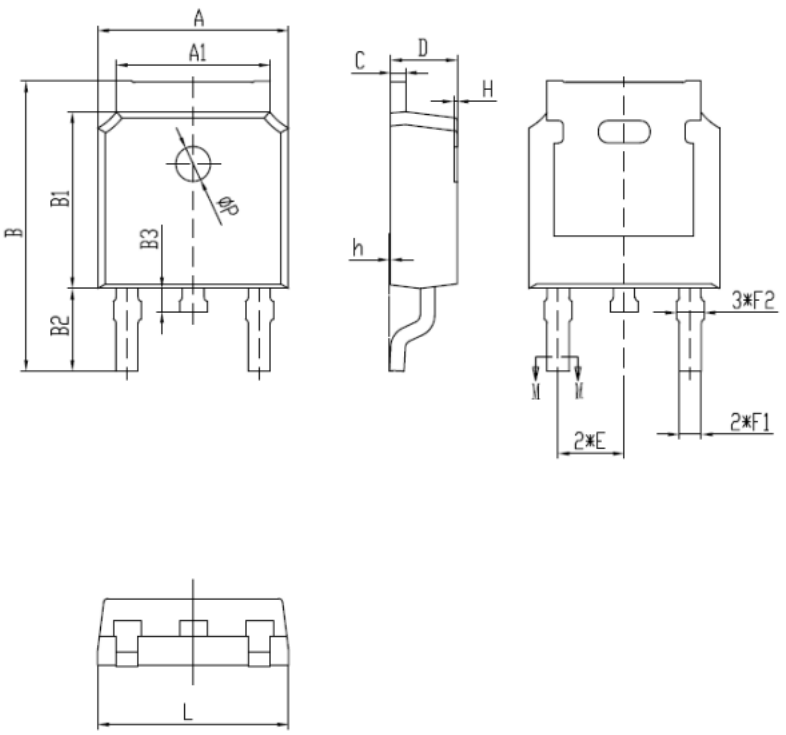
Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



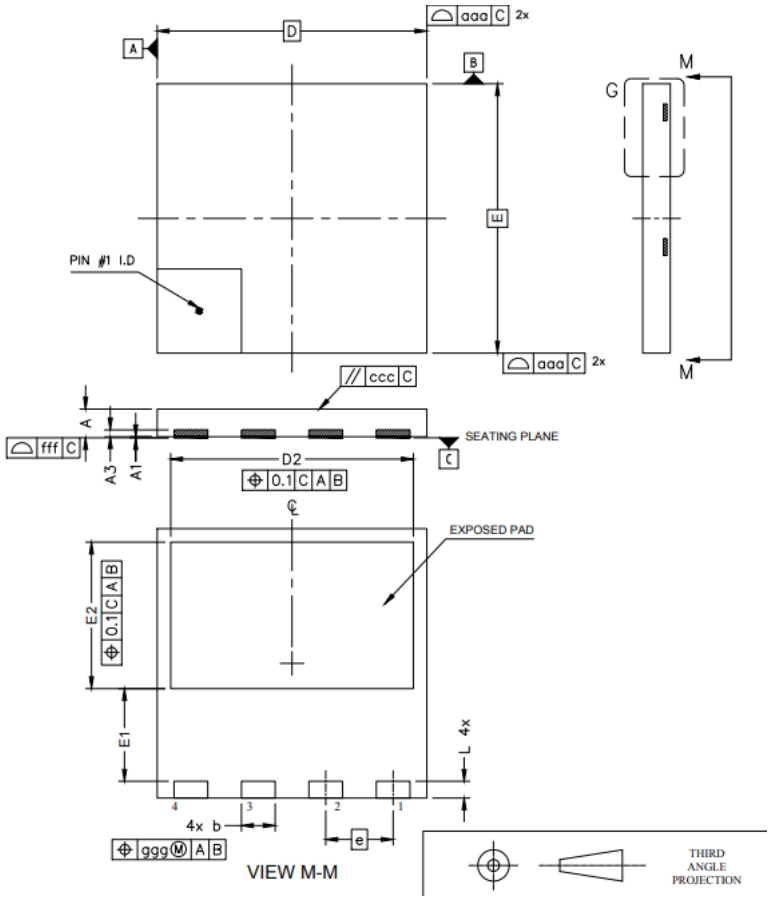
项目	规范(mm)	
	MIN	MAX
A	9.70	10.30
B	15.50	16.10
B1	8.99	9.39
C	4.40	4.80
C1	2.15	2.55
D	2.50	2.90
E	0.70	0.90
F	0.40	0.60
G	1.12	1.42
H	3.40	3.80
L	12.6	13.6
N	2.34	2.74
Q	3.15	3.55
ϕP	3.00	3.30

Figure1：Outline PG-TO220F(HT)



项目	规范(mm)	
	MIN	MAX
A	6.50	6.70
A1	5.16	5.46
B	9.77	10.17
B1	6.00	6.20
B2	2.60	3.00
B3	0.70	0.90
C	0.45	0.61
D	2.20	2.40
E	2.186	2.386
F1	0.67	0.87
F2	0.76	0.96
H	0.00	0.30
h	0.00	0.127
L	6.50	6.70
ΦP	1.10	1.30

Figure2：Outline PG-TO252(HT)



SYMBOL	MIN	MAX
A	0.75	0.95
A1	0.00	0.05
A3	0.10	0.30
b	0.90	1.10
D	7.90	8.10
E	7.90	8.10
D2	7.10	7.30
E1	2.65	2.85
E2	4.25	4.45
e	2.00 BSC	
L	0.40	0.60
aaa	0.10	
ggg	0.05	
ccc	0.05	
fff	0.05	

Figure3：Outline PG-DFN8X8(RYX)

Revision History

Revision	Date	Subjects (major changes since last revision)
1.0	2023-11-14	Preliminary version
1.1	2023-12-25	Added package DFN8X8