**MOSFET Silicon N-Channel MOS**

## 1. Applications

Single-ended flyback or two-transistor forward topologies.
PC power, PD Adaptor, LCD & PDP TV and LED lighting.

## 2. Features

Low drain-source on-resistance: RDS(ON) = 39mΩ (typ.)
Easy to control Gate switching
Enhancement mode: Vth = 3.2 to 4.5 V

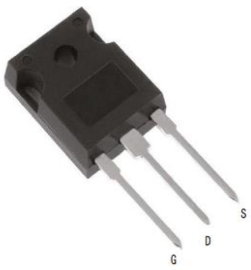
**Table 1 Key Performance Parameters**

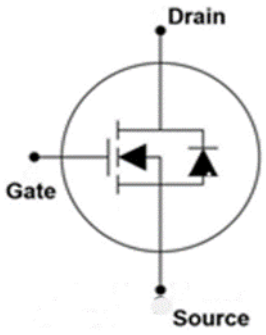
| Parameter | Value | Unit |
|---|---|---|
| $V_{DS}$ @ $T_{j,max}$ | 700 | V |
| $R_{DS(on),max}$ | 46 | mΩ |
| $Q_{g,typ}$ | 111 | nC |
| $I_{D,pulse}$ | 236 | A |
| Body diode dv/dt | 50 | V/ns |

## 3. Packaging and Internal Circuit

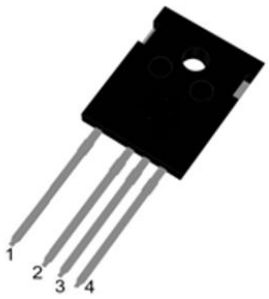
| Part Name | Package | Marking |
|---|---|---|
| ASW65R046EFD | TO247-3L | ASW65R046EFD |
| ASQ65R046EFD | TO247-4L | ASQ65R046EFD |
| ASR65R046EFD | TOLL-8L | ASR65R046EFD |

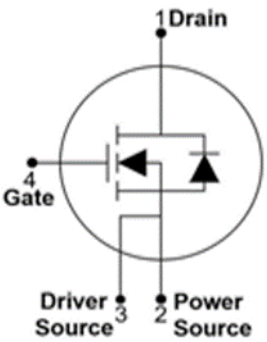
TO247-3L

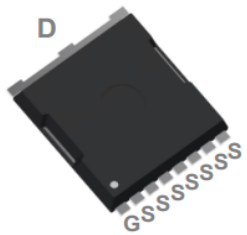


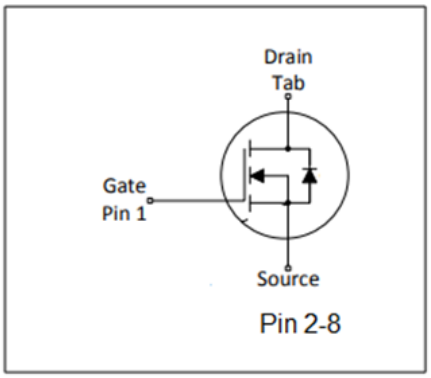

TO247-4L



| TOLL |
| --- |
|  |





# 1 Maximum ratings

at $T_j$ = 25°C, unless otherwise specified

## Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current[1)] | $I_D$ | | - | 59 | A | $T_C$=25°C |
| Pulsed drain current[2)] | $I_{D,pulse}$ | - | - | 236 | A | $T_C$=25°C |
| Avalanche energy, single pulse | $E_{AS}$ | - | - | 414 | mJ | Tc=25°C,VDD=50V, Iav=9.1A, L=10mH, RG=25Ω |
| Avalanche current, single pulse | $I_{AR}$ | - | - | 9.1 | A | Tc=25°C,VDD=50V, L=10mH, RG=25Ω |
| MOSFET dv/dt ruggedness | dv/dt | - | - | 50 | V/ns | $V_{DS}$=0...400V |
| Gate source voltage (static) | $V_{GS}$ | -20 | - | 20 | V | static; |
| Gate source voltage (dynamic) | $V_{GS}$ | -30 | - | 30 | V | AC (f>1 Hz) |
| Power dissipation | $P_{tot}$ | - | - | 347 | W | $T_C$=25°C |
| Storage temperature | $T_{stg}$ | -55 | - | 150 | °C | |
| Operating junction temperature | $T_j$ | -55 | - | 150 | °C | |
| Soldering Temperature<br>Distance of 1.6mm from case for 10s | $T_L$ | | | 260 | °C | |
| Reverse diode dv/dt3) | dv/dt | - | - | 15 | V/ns | VDS=0...400V, ISD<=58A, Tj=25°C |



[1)] Limited by $T_{j,max}$. Maximum Duty Cycle D = 0.50
[2)] Pulse width $t_p$ limited by $T_{j,max}$
[3)] Identical low side and high side switch with identical $R_G$

## 2 Thermal characteristics

### Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | $R_{thJC}$ | - | - | 0.36 | °C/W | - |
| Thermal resistance, junction - ambient | $R_{thJA}$ | - | - | 46.2 | °C/W | device on PCB, minimal footprint |

# 3 Electrical characteristics

at $T_j$=25°C, unless otherwise specified

## Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 650 | - | - | V | $V_{GS}$=0V, $I_D$=250uA |
| Gate threshold voltage | $V_{(GS)th}$ | 3.2 | 3.9 | 4.5 | V | $V_{DS}$=$V_{GS}$, $I_D$=250uA |
| Zero gate voltage drain current | $I_{DSS}$ | - | - | 3 | uA | $V_{DS}$=650V, $V_{GS}$=0V, $T_j$=25°C |
| Gate-source leakage current | $I_{GSS}$ | - | - | 100 | nA | $V_{GS}$=30V, $V_{DS}$=0V |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 39 | 46 | mΩ | $V_{GS}$=10V, $I_D$=29.4A, $T_j$=25°C |
| Gate resistance (Intrinsic) | $R_G$ | - | 3.5 | - | Ω | $f$=1MHz, open drain |

## Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance | $C_{iss}$ | - | 5309 | - | pF | $V_{GS}$=0V, $V_{DS}$=100V, $f$=1MHz |
| Output capacitance | $C_{oss}$ | - | 101.8 | - | pF | $V_{GS}$=0V, $V_{DS}$=100V, $f$=1MHz |
| Reverse transfer capacitance | $C_{rss}$ | - | 10.73 | - | pF | $V_{GS}$=0V, $V_{DS}$=100, $f$=1MHz |
| Turn-on delay time | $t_{d(on)}$ | - | 14.4 | - | ns | $V_{DD}$=400V,$V_{GS}$=13V,$I_D$=44.2A, $R_G$=1.8Ω |
| Rise time | $t_r$ | - | 35.1 | - | ns | $V_{DD}$=400V,$V_{GS}$=13V,$I_D$=44.2A, $R_G$=1.8Ω |
| Turn-off delay time | $t_{d(off)}$ | - | 86.2 | - | ns | $V_{DD}$=400V,$V_{GS}$=13V,$I_D$=44.2A, $R_G$=1.8Ω |
| Fall time | $t_f$ | - | 6.4 | - | ns | $V_{DD}$=400V,$V_{GS}$=13V,$I_D$=44.2A, $R_G$=1.8Ω |

## Table 6 Gate charge characteristics

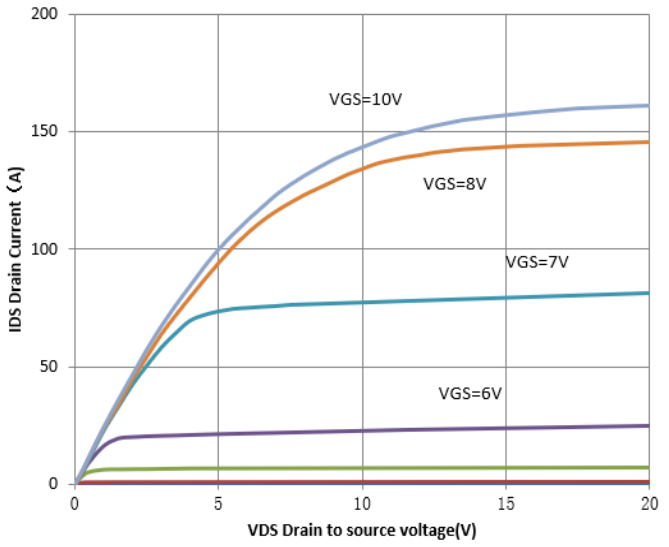
| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | $Q_{gs}$ | - | 28.0 | - | nC | $V_{DD}$=480V, $I_D$=44.2A, $V_{GS}$=0 to 10V |
| Gate to drain charge | $Q_{gd}$ | - | 48.3 | - | nC | $V_{DD}$=480V, $I_D$=44.2A, $V_{GS}$=0 to 10V |
| Gate charge total | $Q_g$ | - | 111 | - | nC | $V_{DD}$=480V, $I_D$=44.2A, $V_{GS}$=0 to 10V |
| Gate plateau voltage | $Vplateau$ | - | 6.18 | - | V | $V_{DD}$=480V, $I_D$=44.2A, $V_{GS}$=0 to 10V |

**Table 7 Reverse diode characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Diode forward voltage | $V_{SD}$ | - | 0.65 | - | V | $V_{GS}$=0V, $I_F$=1A, $T_j$=25°C |
| Reverse recovery time | $t_{rr}$ | - | 168.9 | - | ns | $V_R$=400V, $I_F$=44.2A, d$i_F$/d$t$=100A/µs |
| Reverse recovery charge | $Q_{rr}$ | - | 1.44 | - | uC | $V_R$=400V, $I_F$=44.2A, d$i_F$/d$t$=100A/µs |
| Peak reverse recovery current | $I_{rrm}$ | - | 15.67 | - | A | $V_R$=400V, $I_F$=44.2A, d$i_F$/d$t$=100A/µs |

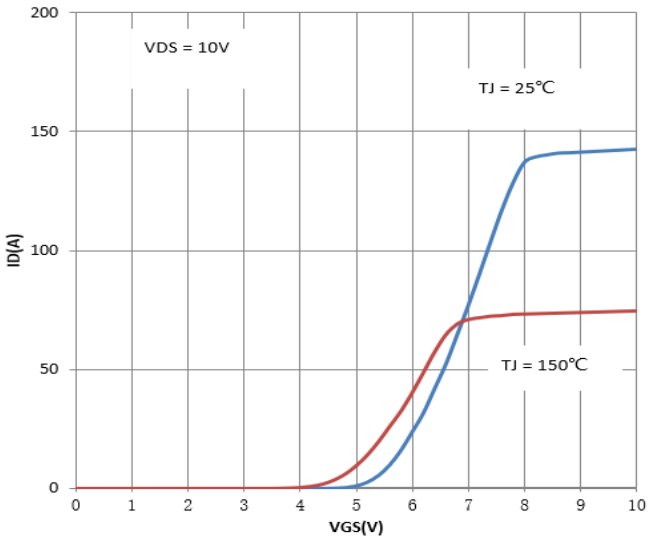
## 4 Electrical characteristics diagram

**Diagram 1: Typ. Output characteristics**



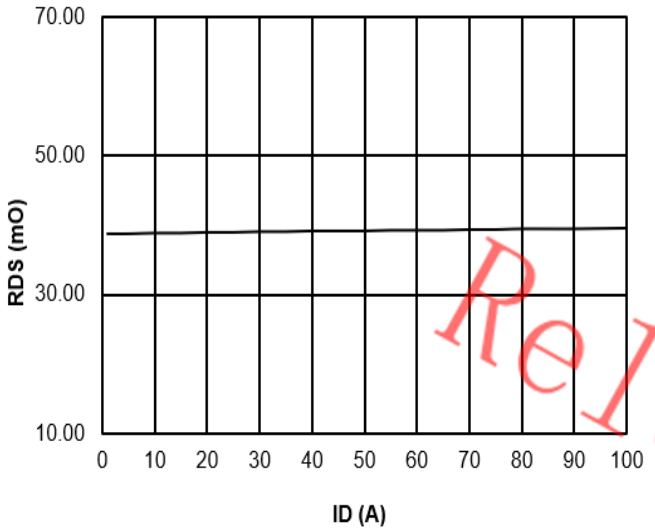

$I_D$=f($V_{DS}$);$T_j$=25 °C; parameter: $V_{GS}$

**Diagram 2: Typ. transfer characteristics**



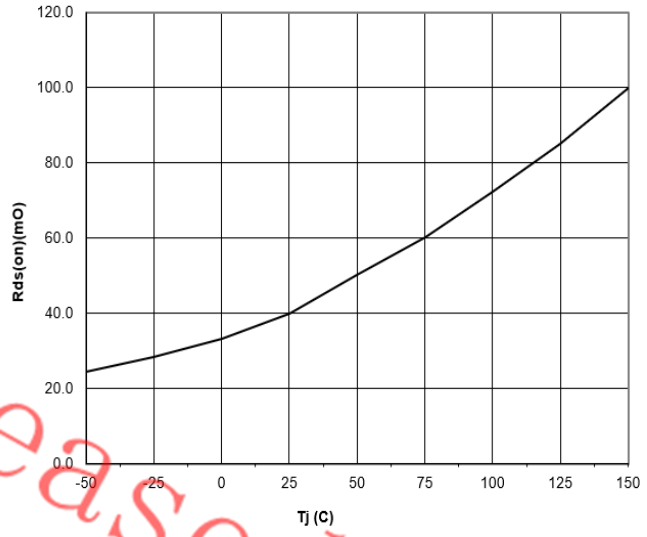

ID=f(VGS); VDS=10V; parameter:Tj

**Diagram 3: Typ. On-Resistance vs. ID**



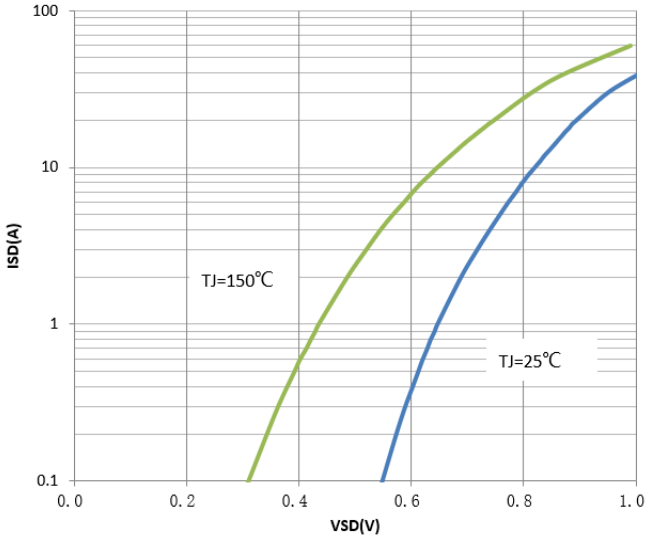

$R_{DS(on)}$=f($I_D$); $T_j$=25°C; parameter:$V_{GS}$=10V

**Diagram 4: Typ. Rdson – Junction Temperature**



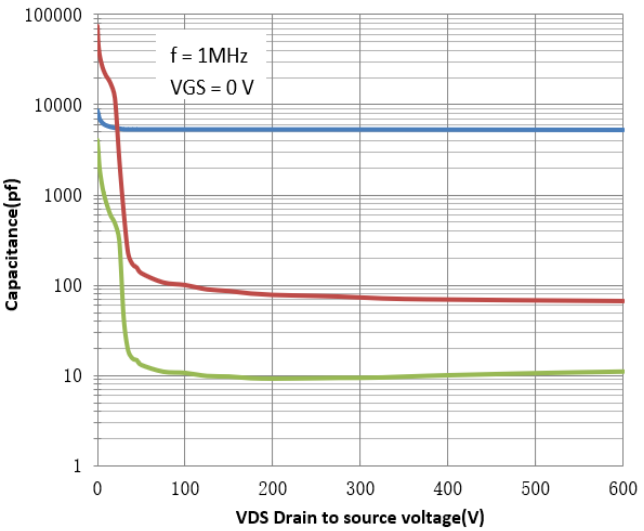

$R_{ds(on)}$=f($T_j$);Vgs=10V/$I_D$=29.4A

**Diagram 5: Typ. Body-Diode Characteristics**



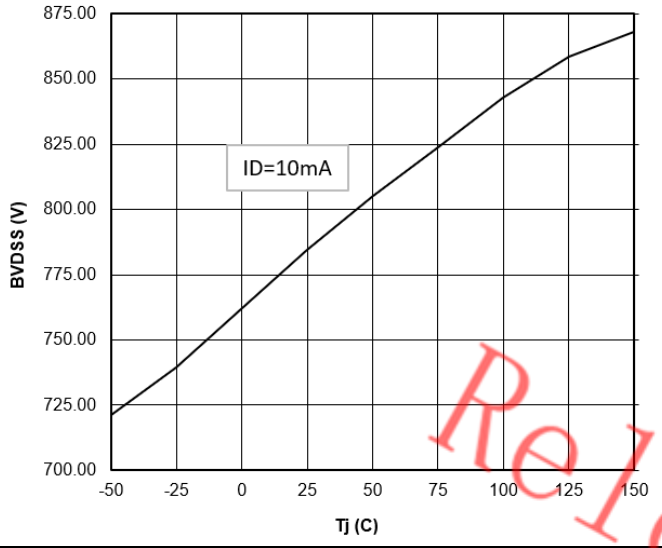

$I_F$=f($V_{DS}$);parameter: $T_j$

**Diagram 6: Typ. Capacitance vs. Vds**



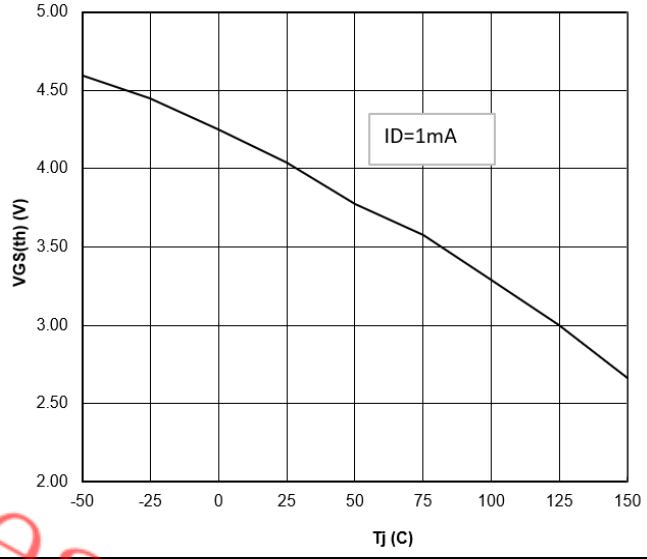

$C$=f($V_{DS}$);$V_{GS}$=0V; $f$=1MHz

**Diagram 7: Typ. Drain-source breakdown voltage**




$V_{BR(DSS)}$=f($T_j$); $I_D$=10mA

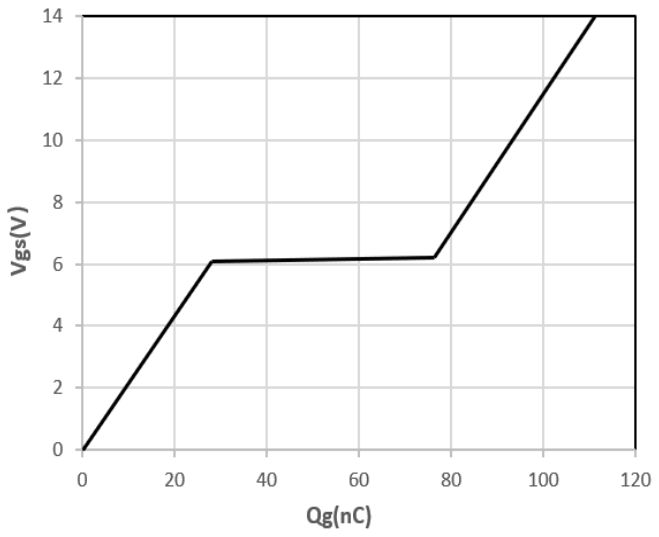
**Diagram 8: Typ. Threshold voltage**




*Vth*=f($T_C$);

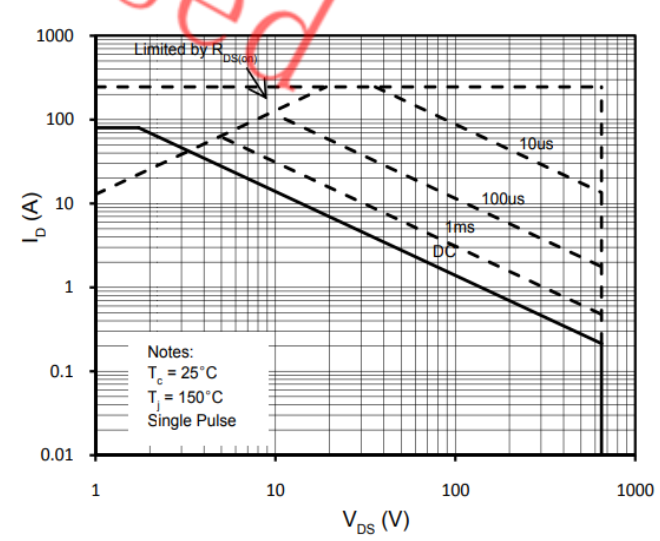


**Diagram 9: Typ. Gate charge**



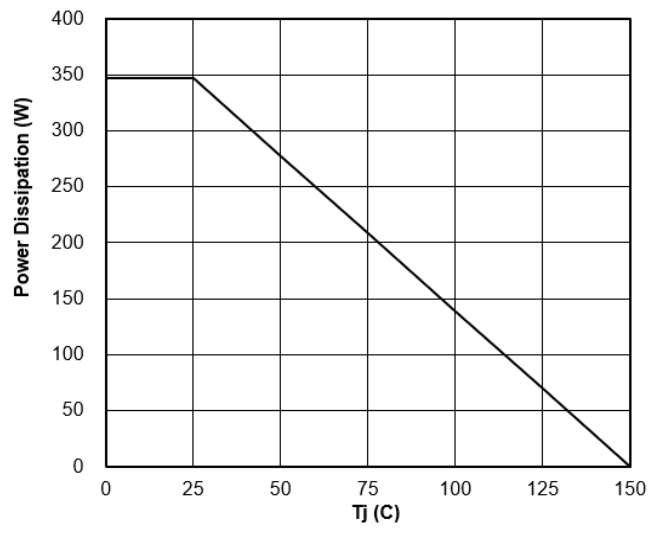

$V_{GS}$=f($Q_{gate}$);$I_D$=50A pulsed; parameter: $V_{DD}$

**Diagram 10: Typ. Maximum Safe Operating Area**



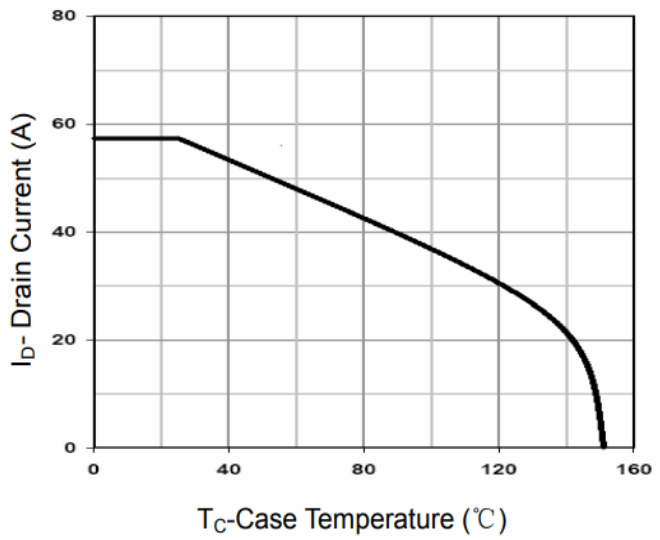

$I_D$=f($V_{DS}$); $T_C$=25 °C; D=0; parameter tp

**Diagram 11: Typ. Power Dissipation**

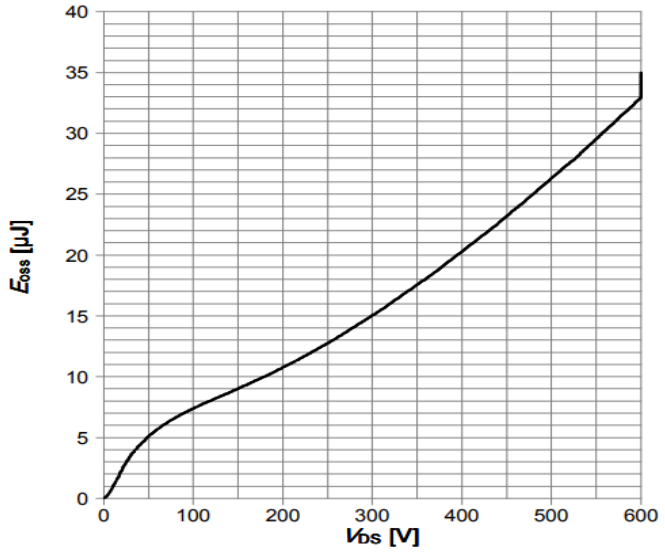
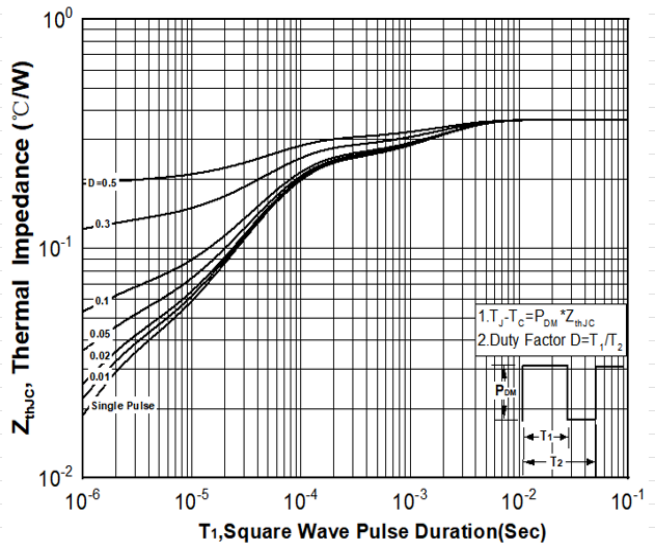



$P_{tot}$=f($T_C$);

**Diagram 12: Typ. Drain Current De-rating**




*Id*=f($T_C$);

| Diagram 13: Typ. Coss stored energy | Diagram 14: Typ. Max. transient thermal impedance |
|---|---|
|  |  |
| $E_{oss}=f(V_{DS})$ | $Z_{thJC}=f(t_P)$; parameter: $D=t_p/T$ |

## 5 Test Circuits

**Table 8 Diode characteristics**

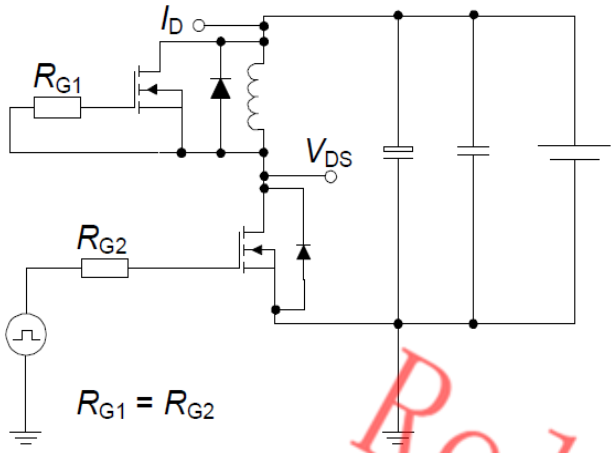
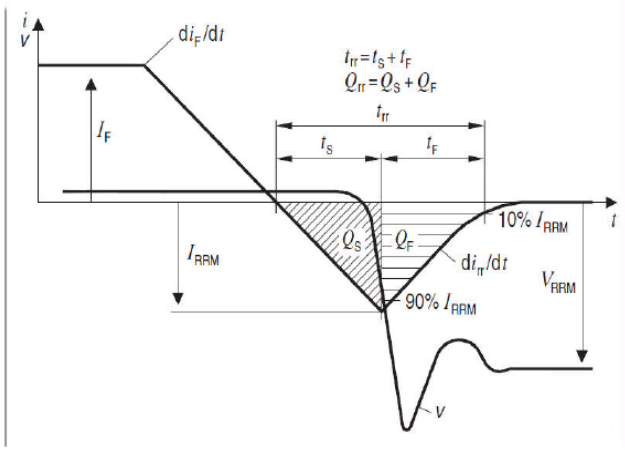
| Test circuit for diode characteristics | Diode recovery waveform |
|---|---|
|  |  |







**Table 9 Switching times**

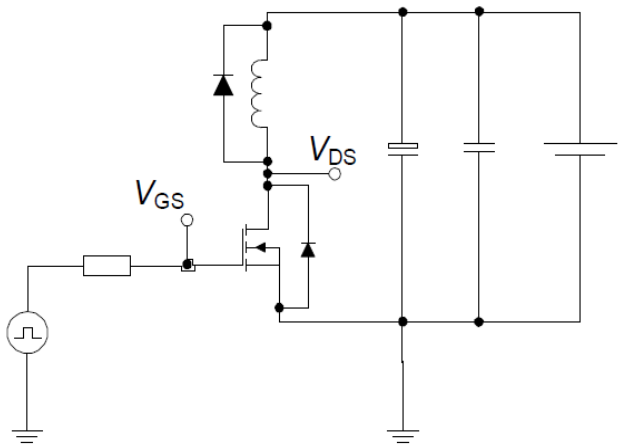
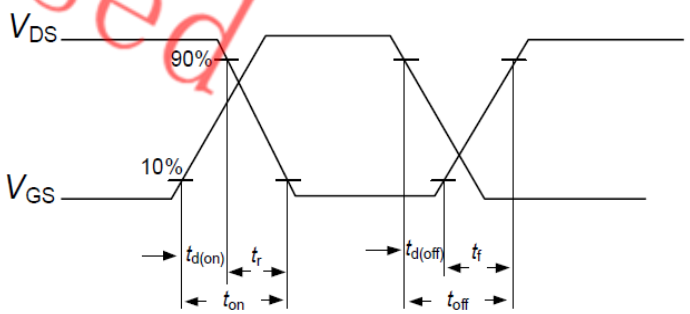
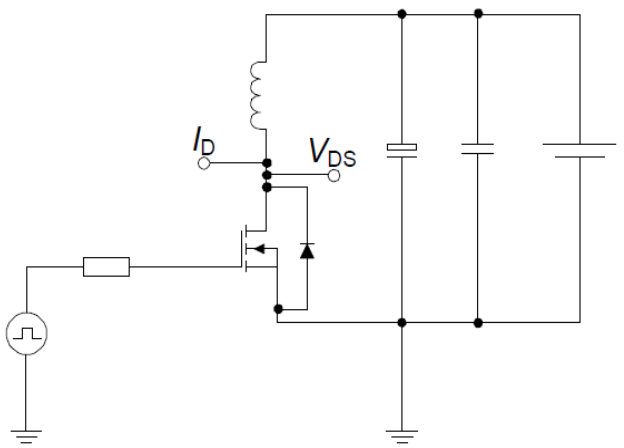
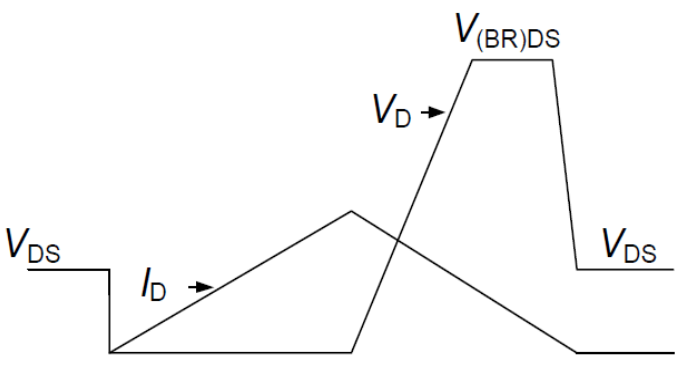
| Switching times test circuit for inductive load | Switching times waveform |
|---|---|
|  |  |

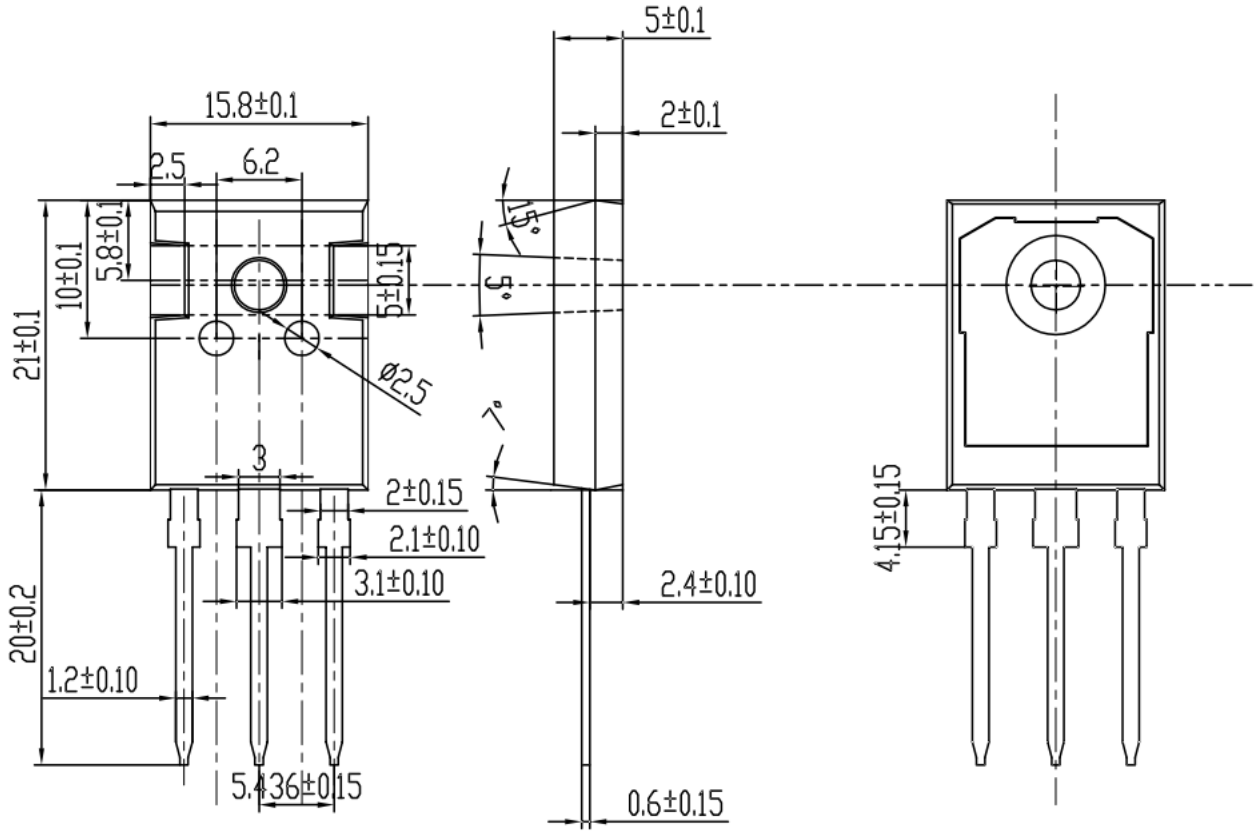




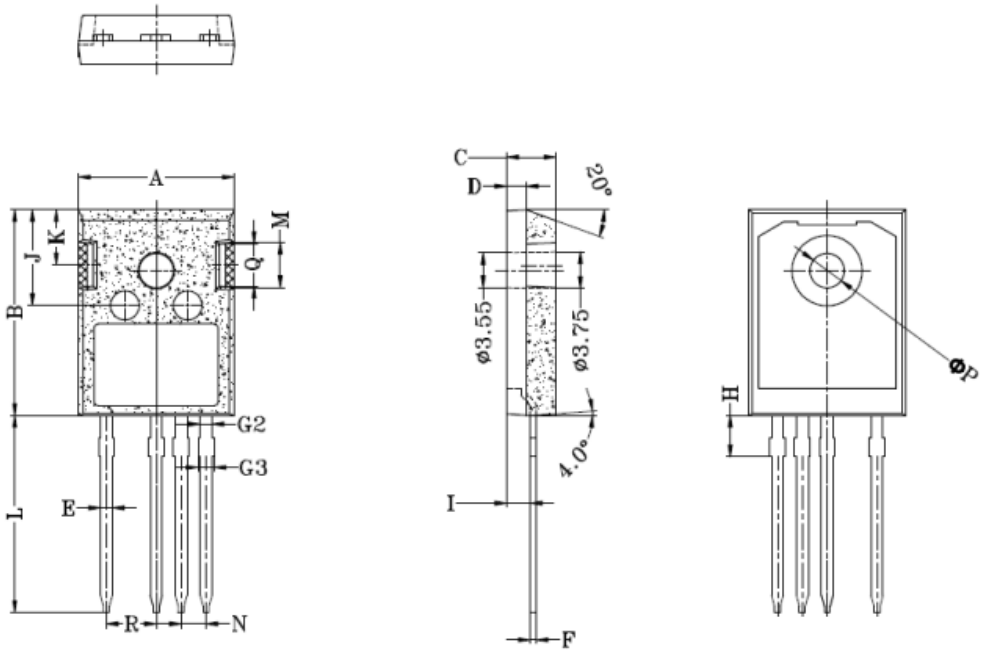
**Table 10 Unclamped inductive load**

| Unclamped inductive load test circuit | Unclamped inductive waveform |
|---|---|
|  |  |

## 6 Package Outlines

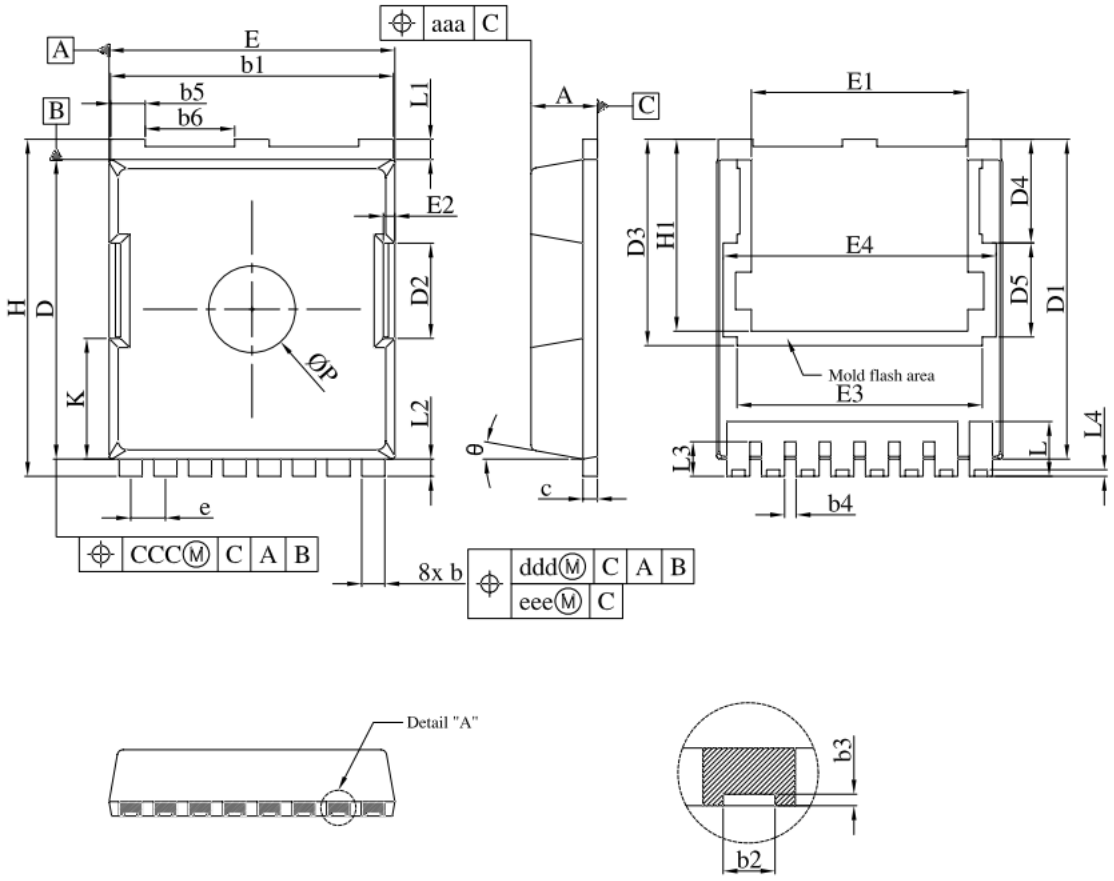



Outline PG-TO247-3L(HT)




| 项目 | 规范(mm) | |
|---|---|---|
| | MIN | MAX |
| A | 15.80 | 16.00 |
| B | 20.90 | 21.10 |
| C | 4.90 | 5.10 |
| D | 1.90 | 2.10 |
| E | 1.10 | 1.30 |
| F | 0.50 | 0.70 |
| G2 | 1.10 | 1.30 |
| G3 | 1.18 | 1.38 |
| H | 4.18 | 4.38 |
| I | 2.30 | 2.50 |
| J | 9.65 | 9.85 |
| K | 5.54 | 5.74 |
| L | 19.80 | 20.20 |
| M | 4.50 | 4.70 |
| N | 2.34 | 2.74 |
| ϕP | 3.40 | 3.60 |
| Q | 4.232 | 4.432 |
| R | 4.88 | 5.28 |

Outline PG-TO247-4L(HT)







| SYMBOL | COMMON MILLIMETER | | |
|---|---|---|---|
| | MIN. | NOMINAL | MAX. |
| A | 2.20 | 2.30 | 2.40 |
| b | 0.70 | 0.80 | 0.90 |
| b1 | 9.70 | 9.80 | 9.90 |
| b2 | 0.36 | 0.45 | 0.55 |
| b3 | 0.05 | 0.100 | / |
| b4 | 0.30 | 0.40 | 0.50 |
| b5 | 1.10 | 1.20 | 1.30 |
| b6 | 3.00 | 3.10 | 3.20 |
| c | 0.40 | 0.50 | 0.60 |
| D | 10.28 | 10.38 | 10.55 |
| D1 | 10.98 | 11.08 | 11.18 |
| D2 | 3.20 | 3.30 | 3.40 |
| D3 | | 7.15 | |
| D4 | | 3.59 | |
| D5 | | 3.26 | |
| e | 1.10 | 1.20 | 1.30 |
| E | 9.80 | 9.90 | 10.00 |
| E1 | 7.40 | 7.50 | 7.60 |
| E2 | 0.30 | 0.40 | 0.50 |
| E3 | | 8.50 | |
| E4 | | 9.46 | |
| H | 11.50 | 11.68 | 11.85 |
| H1 | 6.55 | 6.65 | 6.75 |
| K | 4.08 | 4.18 | 4.28 |
| L | 1.60 | 1.90 | 2.10 |
| L1 | 0.50 | 0.70 | 0.90 |
| L2 | 0.50 | 0.60 | 0.70 |
| L3 | 1.00 | 1.20 | 1.30 |
| L4 | 0.13 | 0.23 | 0.33 |
| P | 2.85 | 3.00 | 3.15 |
| θ | | 10° REF | |
| aaa | | 0.20 | |
| ccc | | 0.20 | |
| ddd | | 0.25 | |
| eee | | 0.20 | |

Outline PG-TOLL(JQ)

## Revision History

| Revision | Date | Subjects (major changes since last revision) |
|---|---|---|
| 1.0 | 2023-11-13 | Preliminary version |
| 1.1 | 2023-11-17 | Added TOLL package |