



# TXB010X (LX) X-Bit Bidirectional Level-Shifting, Voltage-Level Translator

## Product Specification

### Specification Revision History:

Version	Date	Description
2021-04-A1	2021-04	New
2023-04-B1	2023-04	Update the template
2024-01-B2	2024-01	Modify the content



# Contents

<b>1、General Description.....</b>	<b>4</b>
<b>2、Block Diagram And Pin Description .....</b>	<b>7</b>
2.1、Block Diagram .....	7
2.2、Pin Configurations.....	7
2.3、Pin Description.....	8
2.3.1、SOT23-6/SOT363.....	8
2.3.2、TSSOP8/VSSOP8.....	8
2.3.3、SOP14/TSSOP14/DHVQFN14 .....	8
2.3.4、SOP16/TSSOP16.....	9
2.3.5、SOP20/TSSOP20.....	9
2.4、Function Table.....	10
<b>3、Electrical Parameter .....</b>	<b>10</b>
3.1、Absolute Maximum Ratings.....	10
3.2、Recommended operating conditions .....	11
3.3、Electrical Characteristics.....	11
3.3.1、DC Characteristics 1 .....	11
3.3.2、DC Characteristics 2 .....	13
3.3.3、DC Characteristics 3.....	14
3.3.4、AC Characteristics 1 .....	15
3.3.5、AC Characteristics 2.....	16
3.3.6、AC Characteristics 3 .....	18
3.3.7、Typical Power Dissipation Capacitance .....	20
<b>4、Testing Circuit.....</b>	<b>21</b>
4.1、AC Testing Circuit .....	21
4.2、AC Testing Waveforms.....	22
4.3、Measurement Points .....	22
4.4、Test Data .....	23
<b>5、Typical Application Circuit And Application Note.....</b>	<b>23</b>
5.1、Applications .....	23
5.2、Architecture.....	23
5.3、Input Driver Requirements.....	24



灵星芯微 芯片经营

<b>6、Package Information .....</b>	<b>26</b>
6.1、SOT23-6.....	26
6.2、SOT363 .....	27
6.3、TSSOP8.....	28
6.4、VSSOP8 .....	29
6.5、SOP14 .....	30
6.6、TSSOP14.....	31
6.7、SOP16 .....	32
6.8、TSSOP16.....	33
6.9、SOP20 .....	34
6.10、TSSOP20.....	35
<b>7、Statements And Notes .....</b>	<b>36</b>
7.1、The name and content of Hazardous substances or Elements in the product.....	36
7.2、Notes .....	36



灵星芯微 集成电路

## 1、General Description

The TXB010X is an 8-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 8-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins ( $V_{CC(A)}$  and  $V_{CC(B)}$ ).  $V_{CC(A)}$  can be supplied at any voltage between 1.2V and 3.6V and  $V_{CC(B)}$  can be supplied at any voltage between 1.65V and 5.5V, making the device suitable for translating between any of the low voltage nodes (1.2V, 1.5V, 1.8V, 2.5V, 3.3V and 5.0 V). Pins An and OE are referenced to  $V_{CC(A)}$  and pins Bn are referenced to  $V_{CC(B)}$ . A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

### Features:

- Wide supply voltage range:  
 $V_{CC(A)}$ : 1.2V to 3.6V  
 $V_{CC(B)}$ : 1.65V to 5.5V
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5V
- Specified from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Packaging information:  
TXB0101: SOT23-6/SOT363  
TXB0102: TSSOP8/VSSOP8  
TXB0104: SOP14/TSSOP14/DHVQFN14  
TXB0106: SOP16/TSSOP16  
TXB0108: SOP20/TSSOP20



**Ordering Information:**

**Tube packing specifications:**

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
TXB0102DCT (LX)	TSSOP8	DEXX	100 PCS/tube	200 tube/box	20000 PCS/box	Dimensions of plastic enclosure: 3.0mm×3.0mm Pin spacing: 0.65mm
TXB0104DR (LX)	SOP14	TXB0104	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing:1.27mm
TXB0104PW (LX)	TSSOP14	TXB0104	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm
TXB0106DR (LX)	SOP16	TXB0106	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
TXB0106PW (LX)	TSSOP16	TXB0106	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm
TXB0108DR (LX)	SOP20	TXB0108	35 PCS/tube	80 tube/box	2800 PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing:1.27mm
TXB0108PW (LX)	TSSOP20	TXB0108	70 PCS/tube	200 tube/box	14000 PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing:0.65mm



**Reel packing specifications:**

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
TXB0101DB (LX)	SOT23-6	DDXX	3000PCS/reel	30000PCS/box	Dimensions of plastic enclosure: 2.9mm×1.6mm Pin spacing:0.95mm
TXB0101DC (LX)	SOT363	DDXX	3000PCS/reel	30000PCS/box	Dimensions of plastic enclosure: 2.1mm×1.3mm Pin spacing:0.65mm
TXB0102DCT (LX)	TSSOP8	DEXX	3000PCS/reel	3000PCS/box	Dimensions of plastic enclosure: 3.0mm×3.0mm Pin spacing:0.65mm
TXB0102DCU (LX)	VSSOP8	DEXX	3000PCS/reel	3000PCS/box	Dimensions of plastic enclosure: 2.0mm×2.3mm Pin spacing:0.50mm
TXB0104DR (LX)	SOP14	TXB0104	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing:1.27mm
TXB0104PW (LX)	TSSOP14	TXB0104	5000PCS/reel	10000PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm
TXB0106DR (LX)	SOP16	TXB0106	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
TXB0106PW (LX)	TSSOP16	TXB0106	5000PCS/reel	10000PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm
TXB0108DR (LX)	SOP20	TXB0108	2000PCS/reel	2000PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing:1.27mm
TXB0108PW (LX)	TSSOP20	TXB0108	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing:0.65mm

Note 1 : "XX" refers to variable content, meaning year and package batch serial number.

Note 2 : If the physical information is inconsistent with the ordering information, please refer to the actual product.



## 2、Block Diagram And Pin Description

### 2.1、Block Diagram

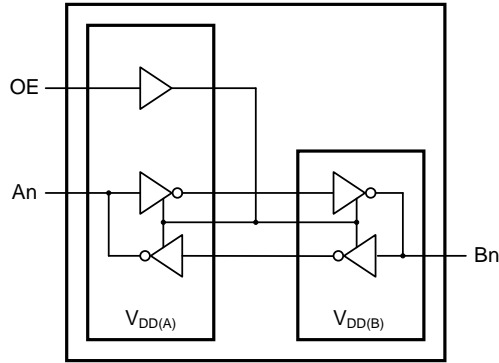
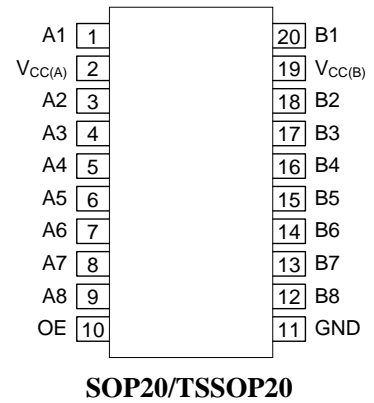
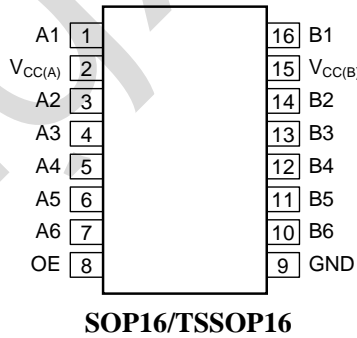
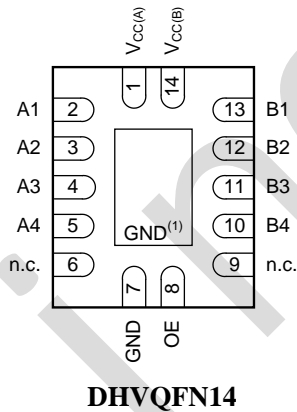
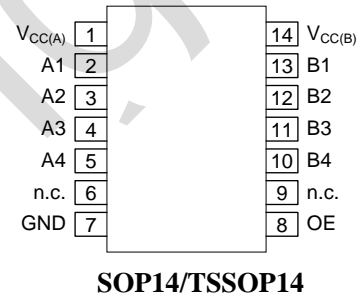
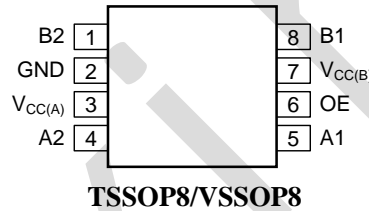
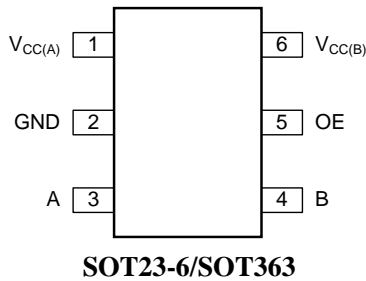


Figure 1. Logic symbol (one channel)

### 2.2、Pin Configurations





灵星芯微 专注经营

### 2.3、Pin Description

#### 2.3.1、SOT23-6/SOT363

Pin No.	Pin Name	Description
1	V <sub>CC(A)</sub>	supply voltage A
2	GND	ground (0V)
3	A	data input or output (referenced to V <sub>CC(A)</sub> )
4	B	data input or output (referenced to V <sub>CC(B)</sub> )
5	OE	output enable input (active HIGH; referenced to V <sub>CC(A)</sub> )
6	V <sub>CC(B)</sub>	supply voltage B

#### 2.3.2、TSSOP8/VSSOP8

Pin No.	Pin Name	Description
1	B2	data input or output (referenced to V <sub>CC(B)</sub> )
2	GND	ground (0V)
3	V <sub>CC(A)</sub>	supply voltage A
4	A2	data input or output (referenced to V <sub>CC(A)</sub> )
5	A1	data input or output (referenced to V <sub>CC(A)</sub> )
6	OE	output enable input (active HIGH; referenced to V <sub>CC(A)</sub> )
7	V <sub>CC(B)</sub>	supply voltage B
8	B1	data input or output (referenced to V <sub>CC(B)</sub> )

#### 2.3.3、SOP14/TSSOP14/DHVQFN14

Pin No.	Pin Name	Description
1	V <sub>CC(A)</sub>	supply voltage A
2	A1	data input or output (referenced to V <sub>CC(A)</sub> )
3	A2	data input or output (referenced to V <sub>CC(A)</sub> )
4	A3	data input or output (referenced to V <sub>CC(A)</sub> )
5	A4	data input or output (referenced to V <sub>CC(A)</sub> )
6	n.c.	not connected
7	GND	ground (0V)
8	OE	output enable input (active HIGH; referenced to V <sub>CC(A)</sub> )
9	n.c.	not connected
10	B4	data input or output (referenced to V <sub>CC(B)</sub> )
11	B3	data input or output (referenced to V <sub>CC(B)</sub> )
12	B2	data input or output (referenced to V <sub>CC(B)</sub> )
13	B1	data input or output (referenced to V <sub>CC(B)</sub> )
14	V <sub>CC(B)</sub>	supply voltage B





灵星芯微 集成电路

### 2.3.4、SOP16/TSSOP16

Pin No.	Pin Name	Description
1	A1	data input or output (referenced to $V_{CC(A)}$ )
2	$V_{CC(A)}$	supply voltage A
3	A2	data input or output (referenced to $V_{CC(A)}$ )
4	A3	data input or output (referenced to $V_{CC(A)}$ )
5	A4	data input or output (referenced to $V_{CC(A)}$ )
6	A5	data input or output (referenced to $V_{CC(A)}$ )
7	A6	data input or output (referenced to $V_{CC(A)}$ )
8	OE	output enable input (active HIGH; referenced to $V_{CC(A)}$ )
9	GND	ground (0V)
10	B6	data input or output (referenced to $V_{CC(B)}$ )
11	B5	data input or output (referenced to $V_{CC(B)}$ )
12	B4	data input or output (referenced to $V_{CC(B)}$ )
13	B3	data input or output (referenced to $V_{CC(B)}$ )
14	B2	data input or output (referenced to $V_{CC(B)}$ )
15	$V_{CC(B)}$	supply voltage B
16	B1	data input or output (referenced to $V_{CC(B)}$ )

### 2.3.5、SOP20/TSSOP20

Pin No.	Pin Name	Description
1	A1	data input or output (referenced to $V_{CC(A)}$ )
2	$V_{CC(A)}$	supply voltage A
3	A2	data input or output (referenced to $V_{CC(A)}$ )
4	A3	data input or output (referenced to $V_{CC(A)}$ )
5	A4	data input or output (referenced to $V_{CC(A)}$ )
6	A5	data input or output (referenced to $V_{CC(A)}$ )
7	A6	data input or output (referenced to $V_{CC(A)}$ )
8	A7	data input or output (referenced to $V_{CC(A)}$ )
9	A8	data input or output (referenced to $V_{CC(A)}$ )
10	OE	output enable input (active HIGH; referenced to $V_{CC(A)}$ )
11	GND	ground (0V)
12	B8	data input or output (referenced to $V_{CC(B)}$ )
13	B7	data input or output (referenced to $V_{CC(B)}$ )
14	B6	data input or output (referenced to $V_{CC(B)}$ )
15	B5	data input or output (referenced to $V_{CC(B)}$ )
16	B4	data input or output (referenced to $V_{CC(B)}$ )
17	B3	data input or output (referenced to $V_{CC(B)}$ )
18	B2	data input or output (referenced to $V_{CC(B)}$ )
19	$V_{CC(B)}$	supply voltage B
20	B1	data input or output (referenced to $V_{CC(B)}$ )



## 2.4、Function Table

Supply voltage		Input	Input/output	
$V_{CC(A)}$	$V_{CC(B)}$	OE	A	B
1.2V to $V_{CC(B)}$	1.65V to 5.5V	L	Z	Z
1.2V to $V_{CC(B)}$	1.65V to 5.5V	H	input or output	output or input
GND	GND	X	Z	Z

Note:

[1] H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state.

[2] When either  $V_{CC(A)}$  or  $V_{CC(B)}$  is at GND level, the device goes into power-down mode.

## 3、Electrical Parameter

### 3.1、Absolute Maximum Ratings

( $T_{amb}=25^{\circ}\text{C}$ , All voltage referenced to GND, unless otherwise specified)

Characteristic	Symbol	Conditions	Min.	Max.	Unit
supply voltage A	$V_{CC(A)}$	-	-0.5	+6.5	V
supply voltage B	$V_{CC(B)}$	-	-0.5	+6.5	V
input voltage	$V_I$	- <sup>[1]</sup>	-0.5	+6.5	V
output voltage	$V_O$	Power-down or 3-state mode <sup>[1]</sup>	-0.5	+6.5	V
		Active mode <sup>[1][2][3]</sup>	-0.5	$V_{CCO}+0.5$	V
input clamping current	$I_{IK}$	$V_I < 0\text{V}$	-50	-	mA
output clamping current	$I_{OK}$	$V_O < 0\text{V}$	-50	-	mA
output current	$I_O$	$V_O = 0\text{V}$ to $V_{CCO}$ <sup>[2]</sup>	-	$\pm 50$	mA
supply current	$I_{CC}$	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
ground current	$I_{GND}$	-	-100	-	mA
storage temperature	$T_{stg}$	-	-65	+150	$^{\circ}\text{C}$
total power dissipation	$P_{tot}$	-	-	500	mW
soldering temperature	$T_L$	10s	260		$^{\circ}\text{C}$

Note:

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.

[2]  $V_{CCO}$  is the supply voltage associated with the output.

[3]  $V_{CCO}+0.5\text{V}$  should not exceed 6.5V.



### 3.2、Recommended operating conditions

Parameter	Symbol	Conditions	Min.	Max.	Unit	
supply voltage A	$V_{CC(A)}$	-	1.2	3.6	V	
supply voltage B	$V_{CC(B)}$	-	1.65	5.5	V	
input voltage	$V_I$	-	0	5.5	V	
output voltage	$V_O$	Power-down or 3-state mode; $V_{CC(A)}=1.2V$ to $3.6V$ ; $V_{CC(B)}=1.65V$ to $5.5V$	A port	0	3.6	V
			B port	0	5.5	V
ambient temperature	$T_{amb}$	-	-40	+125	°C	
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{CC(A)}=1.2V$ to $3.6V$ ; $V_{CC(B)}=1.65V$ to $5.5V$	-	40	ns/V	

Note:

[1] The A and B sides of an unused I/O pair must be held in the same state, both at  $V_{CCI}$  or both at GND.

[2]  $V_{CC(A)}$  must be less than or equal to  $V_{CC(B)}$ .

### 3.3、Electrical Characteristics

#### 3.3.1、DC Characteristics 1

( $T_{amb}=25^\circ C$ , voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
HIGH-level output voltage	$V_{OH}$	A port; $V_{CC(A)}=1.2V$ ; $I_O=-20\mu A$	-	1.1	-	V	
LOW-level output voltage	$V_{OL}$	A port; $V_{CC(A)}=1.2V$ ; $I_O=20\mu A$	-	0.09	-	V	
input leakage current	$I_I$	OE input; $V_I=0V$ to $3.6V$ ; $V_{CC(A)}=1.2V$ to $3.6V$ ; $V_{CC(B)}=1.65V$ to $5.5V$	-	-	$\pm 1$	$\mu A$	
OFF-state output current	$I_{OZ}$	A or B port; $V_O=0V$ or $V_{CCO}$ ; $V_{CC(A)}=1.2V$ to $3.6V$ ; $V_{CC(B)}=1.65V$ to $5.5V$	-	-	$\pm 1$	$\mu A$	
power-off leakage current	$I_{OFF}$	A port; $V_I$ or $V_O=0V$ to $3.6V$ ; $V_{CC(A)}=0V$ ; $V_{CC(B)}=0V$ to $5.5V$	-	-	$\pm 1$	$\mu A$	
		B port; $V_I$ or $V_O=0V$ to $5.5V$ ; $V_{CC(B)}=0V$ ; $V_{CC(A)}=0V$ to $3.6V$	-	-	$\pm 1$	$\mu A$	
input capacitance	$C_I$	OE input; $V_{CC(A)}=1.2V$ to $3.6V$ ; $V_{CC(B)}=1.65V$ to $5.5V$	-	5	-	pF	
input/output capacitance	$C_{I/O}$	A port; $V_{CC(A)}=1.2V$ to $3.6V$ ; $V_{CC(B)}=1.65V$ to $5.5V$	-	5	-	pF	
		B port; $V_{CC(A)}=1.2V$ to $3.6V$ ; $V_{CC(B)}=1.65V$ to $5.5V$	-	8	-	pF	
supply current	$I_{CC(A)}$	$V_{CC(A)}=1.2V$	$V_{CC(B)}=1.8V$	-	10	-	nA
			$V_{CC(B)}=2.5V$	-	10	-	nA
			$V_{CC(B)}=3.3V$	-	10	-	nA
			$V_{CC(B)}=5.0V$	-	10	-	nA
		$V_{CC(A)}=1.5V$	$V_{CC(B)}=1.8V$	-	10	-	nA
			$V_{CC(B)}=2.5V$	-	10	-	nA



			$V_{CC(B)}=3.3V$	-	10	-	nA
			$V_{CC(B)}=5.0V$	-	10	-	nA
		$V_{CC(A)}=1.8V$	$V_{CC(B)}=1.8V$	-	10	-	nA
			$V_{CC(B)}=2.5V$	-	10	-	nA
			$V_{CC(B)}=3.3V$	-	10	-	nA
			$V_{CC(B)}=5.0V$	-	10	-	nA
			$V_{CC(B)}=1.8V$	-	-	-	nA
		$V_{CC(A)}=2.5V$	$V_{CC(B)}=2.5V$	-	10	-	nA
			$V_{CC(B)}=3.3V$	-	10	-	nA
			$V_{CC(B)}=5.0V$	-	10	-	nA
			$V_{CC(B)}=1.8V$	-	-	-	nA
		$V_{CC(A)}=3.3V$	$V_{CC(B)}=2.5V$	-	-	-	nA
			$V_{CC(B)}=3.3V$	-	10	-	nA
			$V_{CC(B)}=5.0V$	-	10	-	nA
			$V_{CC(B)}=1.8V$	-	-	-	nA
		$I_{CC(B)}$	$V_{CC(A)}=1.2V$	$V_{CC(B)}=1.8V$	-	10	-
	$V_{CC(B)}=2.5V$			-	10	-	nA
	$V_{CC(B)}=3.3V$			-	20	-	nA
	$V_{CC(B)}=5.0V$			-	1050	-	nA
	$V_{CC(A)}=1.5V$		$V_{CC(B)}=1.8V$	-	10	-	nA
			$V_{CC(B)}=2.5V$	-	10	-	nA
			$V_{CC(B)}=3.3V$	-	10	-	nA
			$V_{CC(B)}=5.0V$	-	150	-	nA
	$V_{CC(A)}=1.8V$		$V_{CC(B)}=1.8V$	-	10	-	nA
			$V_{CC(B)}=2.5V$	-	10	-	nA
			$V_{CC(B)}=3.3V$	-	10	-	nA
			$V_{CC(B)}=5.0V$	-	350	-	nA
	$V_{CC(A)}=2.5V$		$V_{CC(B)}=1.8V$	-	-	-	nA
			$V_{CC(B)}=2.5V$	-	10	-	nA
			$V_{CC(B)}=3.3V$	-	10	-	nA
			$V_{CC(B)}=5.0V$	-	40	-	nA
	$V_{CC(A)}=3.3V$		$V_{CC(B)}=1.8V$	-	-	-	nA
$V_{CC(B)}=2.5V$			-	-	-	nA	
$V_{CC(B)}=3.3V$			-	10	-	nA	
$V_{CC(B)}=5.0V$			-	10	-	nA	



### 3.3.2、DC Characteristics 2

( $T_{amb}=-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	
HIGH-level input	$V_{IH}$	A or B port and OE input	$V_{CC(A)}=1.2\text{V to }3.6\text{V};$ $V_{CC(B)}=1.65\text{V to }5.5\text{V}$	$0.65V_{CCI}$	-	-	V	
LOW-level input	$V_{IL}$	A or B port and OE input	$V_{CC(A)}=1.2\text{V to }3.6\text{V};$ $V_{CC(B)}=1.65\text{V to }5.5\text{V}$	-	-	$0.35V_{CCI}$	V	
HIGH-level output voltage	$V_{OH}$	A or B port; $I_O=-20\mu\text{A};$	A port; $V_{CC(A)}=1.4\text{V to }3.6\text{V};$	$V_{CCO}-0.4$	-	-	V	
			B port; $V_{CC(B)}=1.65\text{V to }5.5\text{V}$	$V_{CCO}-0.4$	-	-	V	
LOW-level output voltage	$V_{OL}$	A or B port; $I_O=20\mu\text{A};$	A port; $V_{CC(A)}=1.4\text{V to }3.6\text{V};$	-	-	0.4	V	
			B port; $V_{CC(B)}=1.65\text{V to }5.5\text{V}$	-	-	0.4	V	
input leakage current	$I_I$	OE input; $V_I=0\text{V to }3.6\text{V};$ $V_{CC(A)}=1.2\text{V to }3.6\text{V};$ $V_{CC(B)}=1.65\text{V to }5.5\text{V}$		-	-	$\pm 2$	$\mu\text{A}$	
OFF-state output current	$I_{OZ}$	A or B port; $V_O=0\text{V or }V_{CCO};$ $V_{CC(A)}=1.2\text{V to }3.6\text{V};$ $V_{CC(B)}=1.65\text{V to }5.5\text{V}$		-	-	$\pm 2$	$\mu\text{A}$	
power-off leakage current	$I_{OFF}$	A port; $V_I$ or $V_O=0\text{V to }3.6\text{V};$ $V_{CC(A)}=0\text{V}; V_{CC(B)}=0\text{V to }5.5\text{V}$		-	-	$\pm 2$	$\mu\text{A}$	
		B port; $V_I$ or $V_O=0\text{V to }5.5\text{V};$ $V_{CC(B)}=0\text{V}; V_{CC(A)}=0\text{V to }3.6\text{V}$		-	-	$\pm 2$	$\mu\text{A}$	
supply current	$I_{CC}$	$V_I=0\text{V or }V_{CCI}; I_O=0\text{A}$						
		$I_{CC(A)}$	OE=LOW; $V_{CC(A)}=1.4\text{V to }3.6\text{V};$ $V_{CC(B)}=1.65\text{V to }5.5\text{V}$		-	-	5	$\mu\text{A}$
			OE=HIGH; $V_{CC(A)}=1.4\text{V to }3.6\text{V};$ $V_{CC(B)}=1.65\text{V to }5.5\text{V}$		-	-	5	$\mu\text{A}$
			$V_{CC(A)}=3.6\text{V}; V_{CC(B)}=0\text{V}$		-	-	2	$\mu\text{A}$
			$V_{CC(A)}=0\text{V}; V_{CC(B)}=5.5\text{V}$		-	-	-2	$\mu\text{A}$
		$I_{CC(B)}$	OE=LOW; $V_{CC(A)}=1.4\text{V to }3.6\text{V};$ $V_{CC(B)}=1.65\text{V to }5.5\text{V}$		-	-	5	$\mu\text{A}$
			OE=HIGH; $V_{CC(A)}=1.4\text{V to }3.6\text{V};$ $V_{CC(B)}=1.65\text{V to }5.5\text{V}$		-	-	13	$\mu\text{A}$
			$V_{CC(A)}=3.6\text{V}; V_{CC(B)}=0\text{V}$		-	-	-2	$\mu\text{A}$
			$V_{CC(A)}=0\text{V}; V_{CC(B)}=5.5\text{V}$		-	-	2	$\mu\text{A}$
		$I_{CC(A)}+I_{CC(B)}$		$V_{CC(A)}=1.4\text{V to }3.6\text{V};$ $V_{CC(B)}=1.65\text{V to }5.5\text{V}$		-	-	15



Note:

[1]  $V_{CCI}$  is the supply voltage associated with the input.

[2]  $V_{CCO}$  is the supply voltage associated with the output.

### 3.3.3、DC Characteristics 3

( $T_{amb}=-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	
HIGH-level input voltage	$V_{IH}$	A or B port and OE input	$V_{CC(A)}=1.2\text{V to }3.6\text{V};$ $V_{CC(B)}=1.65\text{V to }5.5\text{V}$	$0.65V_{CCI}$	-	-	V	
LOW-level input voltage	$V_{IL}$	A or B port and OE input	$V_{CC(A)}=1.2\text{V to }3.6\text{V};$ $V_{CC(B)}=1.65\text{V to }5.5\text{V}$	-	-	$0.35V_{CCI}$	V	
HIGH-level output voltage	$V_{OH}$	A or B port; $I_O=-20\mu\text{A};$	A port; $V_{CC(A)}=1.4\text{V to }3.6\text{V};$	$V_{CCO}-0.4$	-	-	V	
			B port; $V_{CC(B)}=1.65\text{V to }5.5\text{V}$	$V_{CCO}-0.4$	-	-	V	
LOW-level output voltage	$V_{OL}$	A or B port; $I_O=20\mu\text{A};$	A port; $V_{CC(A)}=1.4\text{V to }3.6\text{V};$	-	-	0.4	V	
			B port; $V_{CC(B)}=1.65\text{V to }5.5\text{V}$	-	-	0.4	V	
input leakage current	$I_I$	OE input; $V_I=0\text{V to }3.6\text{V};$ $V_{CC(A)}=1.2\text{V to }3.6\text{V};$ $V_{CC(B)}=1.65\text{V to }5.5\text{V}$		-	-	$\pm 5$	$\mu\text{A}$	
OFF-state output current	$I_{OZ}$	A or B port; $V_O=0\text{V or }V_{CCO};$ $V_{CC(A)}=1.2\text{V to }3.6\text{V};$ $V_{CC(B)}=1.65\text{V to }5.5\text{V}$		-	-	$\pm 10$	$\mu\text{A}$	
power-off leakage current	$I_{OFF}$	A port; $V_I$ or $V_O=0\text{V to }3.6\text{V};$ $V_{CC(A)}=0\text{V}; V_{CC(B)}=0\text{V to }5.5\text{V}$		-	-	$\pm 10$	$\mu\text{A}$	
		B port; $V_I$ or $V_O=0\text{V to }5.5\text{V};$ $V_{CC(B)}=0\text{V}; V_{CC(A)}=0\text{V to }3.6\text{V}$		-	-	$\pm 10$	$\mu\text{A}$	
supply current	$I_{CC}$	$V_I=0\text{V or }V_{CCI}; I_O=0\text{A}$						
		$I_{CC(A)}$	OE=LOW; $V_{CC(A)}=1.4\text{V to }3.6\text{V};$ $V_{CC(B)}=1.65\text{V to }5.5\text{V}$		-	-	15	$\mu\text{A}$
			OE=HIGH; $V_{CC(A)}=1.4\text{V to }3.6\text{V};$ $V_{CC(B)}=1.65\text{V to }5.5\text{V}$		-	-	20	$\mu\text{A}$
			$V_{CC(A)}=3.6\text{V}; V_{CC(B)}=0\text{V}$		-	-	15	$\mu\text{A}$
			$V_{CC(A)}=0\text{V}; V_{CC(B)}=5.5\text{V}$		-	-	-15	$\mu\text{A}$
		$I_{CC(B)}$	OE=LOW; $V_{CC(A)}=1.4\text{V to }3.6\text{V};$ $V_{CC(B)}=1.65\text{V to }5.5\text{V}$		-	-	20	$\mu\text{A}$
OE=HIGH; $V_{CC(A)}=1.4\text{V to }3.6\text{V};$ $V_{CC(B)}=1.65\text{V to }5.5\text{V}$			-	-	65	$\mu\text{A}$		



			$V_{CC(A)}=3.6V; V_{CC(B)}=0V$	-	-	-15	uA
			$V_{CC(A)}=0V; V_{CC(B)}=5.5V$	-	-	15	uA
		$I_{CC(A)}+I_{CC(B)}$	$V_{CC(A)}=1.4V$ to $3.6V$ ; $V_{CC(B)}=1.65V$ to $5.5V$	-	-	70	uA

Note:

[1]  $V_{CCI}$  is the supply voltage associated with the input.

[2]  $V_{CCO}$  is the supply voltage associated with the output.

### 3.3.4、AC Characteristics 1

( $T_{amb}=25^{\circ}C$ ,  $V_{CC(A)}=1.2V$ , voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions	$V_{CC(B)}$				Unit
			1.8V	2.5V	3.3V	5.0V	
propagation delay	$t_{PHL}$	A to B	19.3	18.1	18.0	18.0	ns
		B to A	22.9	21.5	21.0	21.5	ns
	$t_{PLH}$	A to B	21.8	19.8	19.2	18.7	ns
		B to A	24.5	23.4	22.8	22.8	ns
enable time	$t_{PZL}, t_{PZH}$	OE to A, B	500	500	500	500	ns
disable time	$t_{PLZ}, t_{PHZ}$	OE to A; no external load <sup>[1]</sup>	20	20	20	20	ns
		OE to B; no external load <sup>[1]</sup>	20	18	16	16	ns
		OE to A; see Figure 4	101	92	104	91	ns
		OE to B; see Figure 4	101	92	104	91	ns
transition time	$t_{THL}$	A port	4.1	4.6	5.2	5.7	ns
		B port	2.0	1.9	1.7	1.7	ns
	$t_{TLH}$	A port	11.0	11.9	12.2	12.8	ns
		B port	2.7	2.1	1.9	1.7	ns
output skew time	$t_{sk(o)}$	between channels <sup>[2]</sup>	1.4	0.7	0.6	0.5	ns
pulse width	$t_w$	data inputs	22	22	22	22	ns
data rate	$f_{data}$	-	45	45	45	45	Mbps

Note:

[1] These values are guaranteed by design.

[2] Skew between any two outputs of the same package switching in the same direction.



### 3.3.5、AC Characteristics 2

( $T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions	$V_{CC(B)}$								Unit
			1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$V_{CC(A)}=1.5V\pm0.1V$											
propagation delay	$t_{PLH}, t_{PHL}$	A to B	1.4	26.4	1.2	22.8	1.1	21.4	0.8	21.0	ns
		B to A	0.9	25.4	0.7	21.6	0.4	19.6	0.3	18.0	ns
enable time	$t_{PZL}, t_{PZH}$	OE to A, B	-	1	-	1	-	1	-	1	us
disable time	$t_{PLZ}, t_{PHZ}$	OE to A; no external load <sup>[1]</sup>	3.7	18	3.7	18	3.7	18	3.7	18	ns
		OE to B; no external load <sup>[1]</sup>	3.7	23	3.5	22	3.0	21	1.7	20	ns
		OE to A; see Figure 4	-	320	-	320	-	320	-	320	ns
		OE to B; see Figure 4	-	200	-	200	-	200	-	200	ns
transition time	$t_{THL}, t_{TLH}$	A port	0.8	5.6	0.8	5.9	0.8	6.8	0.8	6.5	ns
		B port	1.0	4.4	0.7	3.2	0.7	2.9	0.6	2.6	ns
output skew time	$t_{sk(o)}$	between channels <sup>[2]</sup>	-	2.6	-	1.9	-	1.6	-	1.3	ns
pulse width	$t_W$	data inputs	20	-	20	-	20	-	20	-	ns
data rate	$f_{data}$	-	-	50	-	50	-	50	-	50	Mbps
$V_{CC(A)}=1.8V\pm0.15V$											
propagation delay	$t_{PLH}, t_{PHL}$	A to B	1.6	21.2	1.4	17.0	1.3	15.6	1.2	15.0	ns
		B to A	1.5	20.2	1.3	15.4	0.8	13.8	0.5	13.2	ns
enable time	$t_{PZL}, t_{PZH}$	OE to A, B	-	1	-	1	-	1	-	1	us
disable time	$t_{PLZ}, t_{PHZ}$	OE to A; no external load <sup>[1]</sup>	2.9	17	2.9	17	2.9	17	2.9	17	ns
		OE to B; no external load <sup>[1]</sup>	4.0	22	3.0	22	2.5	21	1.5	20	ns
		OE to A; see Figure 4	-	260	-	260	-	260	-	260	ns
		OE to B; see Figure 4	-	200	-	200	-	200	-	200	ns
transition time	$t_{THL}, t_{TLH}$	A port	0.7	4.2	0.7	3.8	1.0	3.5	0.7	3.2	ns
		B port	1.0	4.5	0.7	3.5	0.7	3.0	0.6	2.6	ns
output skew	$t_{sk(o)}$	between channels <sup>[2]</sup>	-	0.8	-	0.8	-	0.8	-	0.8	ns
pulse width	$t_W$	data inputs	22	-	18	-	17	-	17	-	ns
data rate	$f_{data}$	-	-	45	-	55	-	60	-	60	Mbps
$V_{CC(A)}=2.5V\pm0.2V$											
propagation delay	$t_{PLH}, t_{PHL}$	A to B	-	-	1.1	12.2	1.0	11.0	0.9	10.0	ns
		B to A	-	-	1.0	11.6	0.6	10.2	0.3	9.0	ns
enable time	$t_{PZL}, t_{PZH}$	OE to A, B	-	-	-	1	-	1	-	1	us
disable time	$t_{PLZ}, t_{PHZ}$	OE to A; no external load <sup>[1]</sup>	-	-	2.5	12	2.5	12	2.5	11	ns
		OE to B; no external load <sup>[1]</sup>	-	-	2.0	17	2.8	16	1.2	15	ns
		OE to A; see Figure 4	-	-	-	200	-	200	-	200	ns
		OE to B; see Figure 4	-	-	-	200	-	200	-	200	ns





transition time	$t_{THL}, t_{TLH}$	A port	-	-	0.8	3.0	0.6	3.0	0.5	3.5	ns
		B port	-	-	0.6	3.2	0.7	3.0	0.6	2.7	ns
output skew time	$t_{sk(o)}$	between channels <sup>[2]</sup>	-	-	-	0.4	-	0.3	-	0.3	ns
pulse width	$t_W$	data inputs	-	-	13	-	11	-	10	-	ns
data rate	$f_{data}$	-	-	-	-	80	-	90	-	100	Mbps
<b><math>V_{CC(A)}=3.3V\pm 0.3V</math></b>											
propagation delay	$t_{PLH}, t_{PHL}$	A to B	-	-	-	-	0.9	9.2	0.8	8.2	ns
		B to A	-	-	-	-	0.5	8.4	0.2	7.2	ns
enable time	$t_{PZL}, t_{PZH}$	OE to A, B	-	-	-	-	-	1	-	1	us
disable time	$t_{PLZ}, t_{PHZ}$	OE to A; no external load <sup>[1]</sup>	-	-	-	-	2.1	13	2.0	12	ns
		OE to B; no external load <sup>[1]</sup>	-	-	-	-	1.0	12	1.7	11	ns
		OE to A; see Figure 4	-	-	-	-	-	200	-	200	ns
		OE to B; see Figure 4	-	-	-	-	-	200	-	200	ns
transition time	$t_{THL}, t_{TLH}$	A port	-	-	-	-	0.5	2.9	0.5	3.0	ns
		B port	-	-	-	-	0.7	3.0	0.6	2.6	ns
output skew time	$t_{sk(o)}$	between channels <sup>[2]</sup>	-	-	-	-	-	0.4	-	0.3	ns
pulse width	$t_W$	data inputs	-	-	-	-	10.0	-	9.0	-	ns
data rate	$f_{data}$	-	-	-	-	-	-	100	-	110	Mbps

Note:

[1] These values are guaranteed by design.

[2] Skew between any two outputs of the same package switching in the same direction.



### 3.3.6. AC Characteristics 3

( $T_{amb} = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions	$V_{CC(B)}$								Unit
			1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$V_{CC(A)}=1.5V\pm0.1V$											
propagation delay	$t_{PLH}, t_{PHL}$	A to B	1.4	29.0	1.2	25.0	1.1	23.5	0.8	23.1	ns
		B to A	0.9	27.9	0.7	23.7	0.4	21.5	0.3	19.8	ns
enable time	$t_{PZL}, t_{PZH}$	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	us
disable time	$t_{PLZ}, t_{PHZ}$	OE to A; no external load <sup>[1]</sup>	3.7	19.8	3.7	19.8	3.7	19.8	3.7	19.8	ns
		OE to B; no external load <sup>[1]</sup>	3.7	25.3	3.5	24.2	3.0	23.1	1.7	22	ns
		OE to A; see Figure 4	-	350	-	350	-	350	-	350	ns
		OE to B; see Figure 4	-	220	-	220	-	220	-	220	ns
transition time	$t_{THL}, t_{TLH}$	A port	0.8	6.2	0.8	6.2	0.8	7.5	0.8	7.1	ns
		B port	1.0	4.9	0.7	3.5	0.7	3.2	0.6	2.9	ns
output skew time	$t_{sk(o)}$	between channels <sup>[2]</sup>	-	2.9	-	2.1	-	1.8	-	1.5	ns
pulse width	$t_W$	data inputs	30	-	28	-	25	-	25	-	ns
data rate	$f_{data}$	-	-	33	-	35	-	40	-	40	Mbps
$V_{CC(A)}=1.8V\pm0.15V$											
propagation delay	$t_{PLH}, t_{PHL}$	A to B	1.6	23.3	1.4	18.6	1.3	17.1	1.2	16.5	ns
		B to A	1.5	22.2	1.2	16.9	0.8	15.2	0.5	14.5	ns
enable time	$t_{PZL}, t_{PZH}$	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	us
disable time	$t_{PLZ}, t_{PHZ}$	OE to A; no external load <sup>[1]</sup>	2.9	18.7	2.9	18.7	2.9	18.7	2.9	18.7	ns
		OE to B; no external load <sup>[1]</sup>	4.0	24.0	3.0	24.0	2.5	23.2	1.5	22.0	ns
		OE to A; see Figure 4	-	280	-	280	-	280	-	280	ns
		OE to B; see Figure 4	-	220	-	220	-	220	-	220	ns
transition time	$t_{THL}, t_{TLH}$	A port	0.8	4.6	0.7	4.2	1.0	3.9	0.7	3.5	ns
		B port	1.0	4.9	0.7	3.9	0.7	3.3	0.6	2.9	ns
output skew	$t_{sk(o)}$	between channels <sup>[2]</sup>	-	0.8	-	0.7	-	0.6	-	0.6	ns
pulse width	$t_W$	data inputs	25	-	20	-	18	-	18	-	ns
data rate	$f_{data}$	-	-	40	-	50	-	55	-	55	Mbps
$V_{CC(A)}=2.5V\pm0.2V$											
propagation delay	$t_{PLH}, t_{PHL}$	A to B	-	-	1.1	13.6	1.0	12.1	0.9	11.0	ns
		B to A	-	-	1.0	12.7	0.6	11.2	0.3	10.0	ns
enable time	$t_{PZL}, t_{PZH}$	OE to A, B	-	-	-	1.0	-	1.0	-	1.0	us
disable time	$t_{PLZ}, t_{PHZ}$	OE to A; no external load <sup>[1]</sup>	-	-	2.5	13.2	2.5	13.2	2.5	13.2	ns
		OE to B; no external load <sup>[1]</sup>	-	-	2.0	18.7	2.8	17.6	1.2	16.5	ns
		OE to A; see Figure 4	-	-	-	220	-	220	-	220	ns
		OE to B; see Figure 4	-	-	-	220	-	220	-	220	ns



transition time	$t_{THL}, t_{TLH}$	A port	-	-	0.8	3.3	0.6	3.3	0.5	3.8	ns
		B port	-	-	0.6	3.5	0.7	3.3	0.6	3.0	ns
output skew time	$t_{sk(o)}$	between channels <sup>[2]</sup>	-	-	-	0.4	-	0.3	-	0.3	ns
pulse width	$t_W$	data inputs	-	-	14	-	13	-	13	-	ns
data rate	$f_{data}$	-	-	-	-	70	-	80	-	80	Mbps
<b><math>V_{CC(A)}=3.3V\pm 0.3V</math></b>											
propagation delay	$t_{PLH}, t_{PHL}$	A to B	-	-	-	-	0.9	9.9	0.8	9.0	ns
		B to A	-	-	-	-	0.5	9.3	0.2	8.0	ns
enable time	$t_{PZL}, t_{PZH}$	OE to A, B	-	-	-	-	-	1.0	-	1.0	us
disable time	$t_{PLZ}, t_{PHZ}$	OE to A; no external load <sup>[1]</sup>	-	-	-	-	2.1	14.1	2.0	13.1	ns
		OE to B; no external load <sup>[1]</sup>	-	-	-	-	1.0	13.1	1.7	12.1	ns
		OE to A; see Figure 4	-	-	-	-	-	220	-	220	ns
		OE to B; see Figure 4	-	-	-	-	-	220	-	220	ns
transition time	$t_{THL}, t_{TLH}$	A port	-	-	-	-	0.5	3.2	0.5	3.3	ns
		B port	-	-	-	-	0.7	3.3	0.6	2.9	ns
output skew time	$t_{sk(o)}$	between channels <sup>[2]</sup>	-	-	-	-	-	0.4	-	0.3	ns
pulse width	$t_W$	data inputs	-	-	-	-	10	-	10	-	ns
data rate	$f_{data}$	-	-	-	-	-	-	100	-	100	Mbps

Note:

[1] These values are guaranteed by design.

[2] Skew between any two outputs of the same package switching in the same direction.



### 3.3.7、Typical Power Dissipation Capacitance

( $T_{amb}=25^{\circ}\text{C}$ , voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions	$V_{CC(A)}$							Unit	
			1.2V	1.2V	1.5V	1.8V	2.5V	2.5V	3.3V		
			$V_{CC(B)}$								
			1.8V	5.0V	1.8V	1.8V	2.5V	5.0V	3.3V to 5.0V		
power dissipation capacitance	$C_{PD}$	outputs enabled; $OE=V_{CC(A)}$	A port: (direction A to B)	7.0	6.5	7.2	7.6	7.6	7.0	8.0	pF
			A port: (direction B to A)	9.6	10.0	9.8	10.1	10.5	10.3	10.8	pF
			B port: (direction A to B)	23.3	28.7	23.1	23.1	23.7	25.9	25.9	pF
			B port: (direction B to A)	17.8	25.5	17.1	16.8	17.4	21.0	20.5	pF
		outputs disabled; $OE=GND$	A port: (direction A to B)	0.2	0.2	0.2	0.3	0.3	0.3	0.3	pF
			A port: (direction B to A)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
			B port: (direction A to B)	0.01	0.02	0.01	0.01	0.01	0.01	0.01	pF
			B port: (direction B to A)	0.2	0.3	0.2	0.2	0.3	0.3	0.3	pF

Note:

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i\times N+\sum(C_L\times V_{CC}^2\times f_o)$  where:

$f_i$ =input frequency in MHz;  $f_o$ =output frequency in MHz;

$C_L$ =load capacitance in pF;  $V_{CC}$ =supply voltage in V;

$N$ =number of inputs switching;  $\sum(C_L\times V_{CC}^2\times f_o)$ =sum of the outputs.

[2]  $f_i=10\text{MHz}$ ;  $V_I=GND$  to  $V_{CC}$ ;  $t_r=t_f=1\text{ns}$ ;  $C_L=0\text{pF}$ ;  $R_L=\infty\Omega$ .

## 4、Testing Circuit

### 4.1、AC Testing Circuit

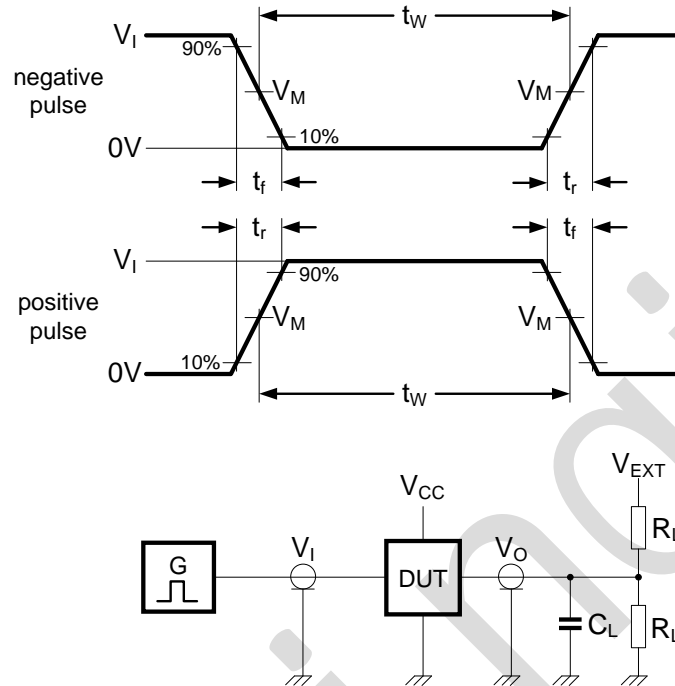


Figure 2. Test circuit for measuring switching times

All input pulses are supplied by generators having the following characteristics:

$PRR \leq 10\text{MHz}$ ;  $Z_0 = 50\Omega$ ;  $dV/dt \geq 1.0\text{V/ns}$ .

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$V_{EXT}$  = External voltage for measuring switching times.



## 4.2、AC Testing Waveforms

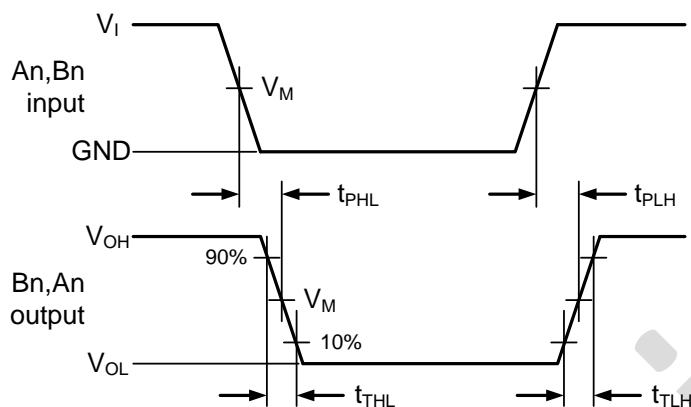


Figure 3. The data input (An, Bn) to data output (Bn, An) propagation delay times

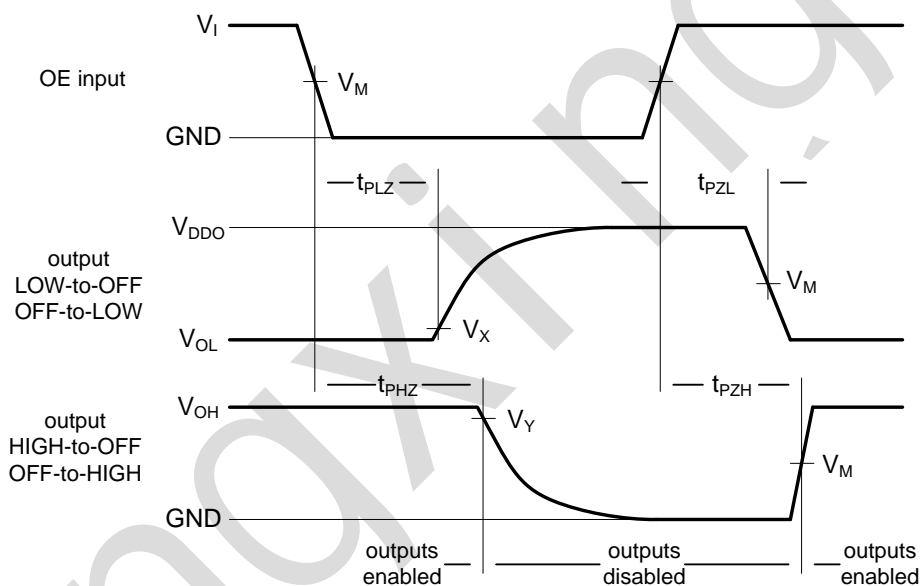


Figure 4. 3-state enable and disable times

## 4.3、Measurement Points

Supply voltage	Input	Output		
$V_{CCO}$	$V_M$	$V_M$	$V_X$	$V_Y$
1.2V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL}+0.1V$	$V_{OH}-0.1V$
$1.5V\pm 0.1V$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL}+0.1V$	$V_{OH}-0.1V$
$1.8V\pm 0.15V$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL}+0.15V$	$V_{OH}-0.15V$
$2.5V\pm 0.2V$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL}+0.15V$	$V_{OH}-0.15V$
$3.3V\pm 0.3V$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL}+0.3V$	$V_{OH}-0.3V$
$5.0V\pm 0.5V$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL}+0.3V$	$V_{OH}-0.3V$

Note:

[1]  $V_{CCI}$  is the supply voltage associated with the input.

[2]  $V_{CCO}$  is the supply voltage associated with the output.



灵星芯微 集成电路

#### 4.4. Test Data

Supply voltage		Input		Load		$V_{EXT}$		
$V_{CC(A)}$	$V_{CC(B)}$	$V_I$	$\Delta t/\Delta V$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
1.2V to 3.6V	1.65V to 5.5V	$V_{CCI}$	$\leq 1.0\text{ns/V}$	15pF	50k $\Omega$ , 1M $\Omega$	open	open	2 $V_{CCO}$

Note:

[1]  $V_{CCI}$  is the supply voltage associated with the input.

[2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements,  $R_L=1\text{M}\Omega$ . For measuring enable and disable times,  $R_L=50\text{K}\Omega$ .

[3]  $V_{CCO}$  is the supply voltage associated with the output.

## 5. Typical Application Circuit And Application Note

### 5.1. Applications

Voltage level-translation applications. The TXB010X can be used to interface between devices or systems operating at different supply voltages. See Figure 5 for a typical operating circuit using the TXB010X.

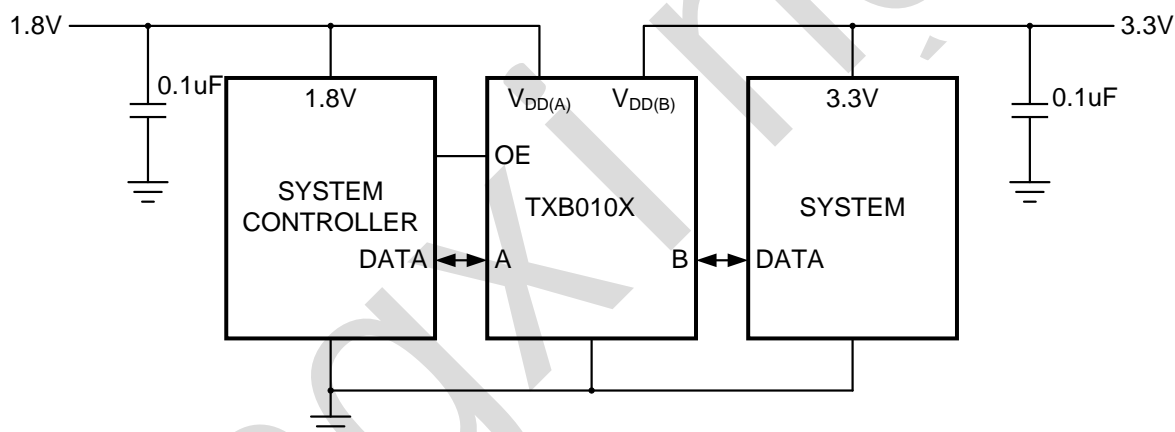


Figure 5. Typical operating circuit

### 5.2. Architecture

The architecture of the TXB010X is shown in Figure 6. The device does not require an extra input signal to control the direction of data flow from A to B or from B to A. In a static state, the output drivers of the TXB010X can maintain a defined output level, but the output architecture is designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing in the opposite direction. The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shots turn on the PMOS transistors (T1, T3) for a short duration, accelerating the low-to-high transition. Similarly, during a falling edge, the one shots turn on the NMOS transistors (T2, T4) for a short duration, accelerating the high-to-low transition. During output transitions the typical output impedance is 70 $\Omega$  at  $V_{CCO}=1.2\text{V}$  to 1.8V, 50  $\Omega$  at  $V_{CCO}=1.8\text{V}$  to 3.3V and 40 $\Omega$  at  $V_{CCO}=3.3\text{V}$  to 5.0V.

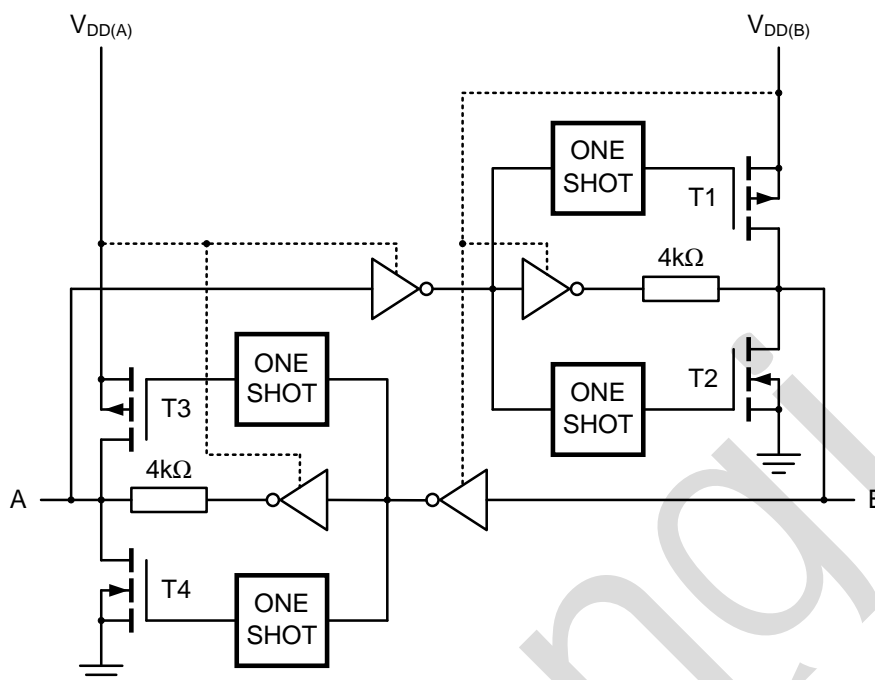
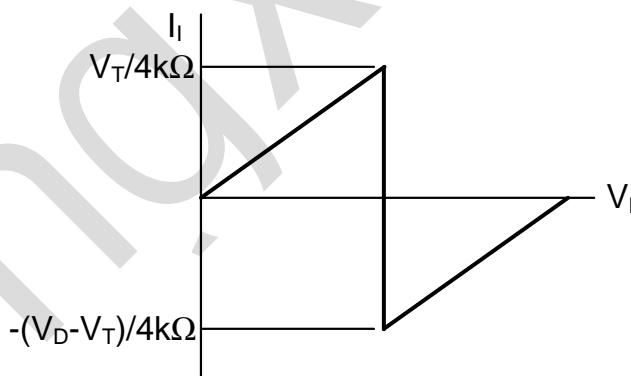


Figure 6. Architecture of TXB010X I/O cell (one channel)

### 5.3. Input Driver Requirements

For correct operation, the device driving the data I/Os of the TXB010X must have a minimum drive capability of  $\pm 2\text{mA}$ . See Figure 7 for a plot of typical input current versus input voltage.



$V_T$ : input threshold voltage of the TXB010X (typically  $V_{CC1}/2$ ).

$V_D$ : supply voltage of the external driver.

Figure 7. Typical input current versus input voltage graph





灵星芯微 精密控制

#### 5.4、Power Up

During operation  $V_{CC(A)}$  must never be higher than  $V_{CC(B)}$ , however during power-up  $V_{CC(A)} \geq V_{CC(B)}$  does not damage the device, so either power supply can be ramped up first. There is no special power-up sequencing required. The TXB010X includes circuitry that disables all output ports when either  $V_{CC(A)}$  or  $V_{CC(B)}$  is switched off.

#### 5.5、Enable And Disable

An output enable input (OE) is used to disable the device. Setting OE=LOW causes all I/Os to assume the high-impedance OFF-state. The disable time ( $t_{dis}$  with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time ( $t_{en}$ ) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor, the minimum value of the resistor is determined by the current-sourcing capability of the driver.

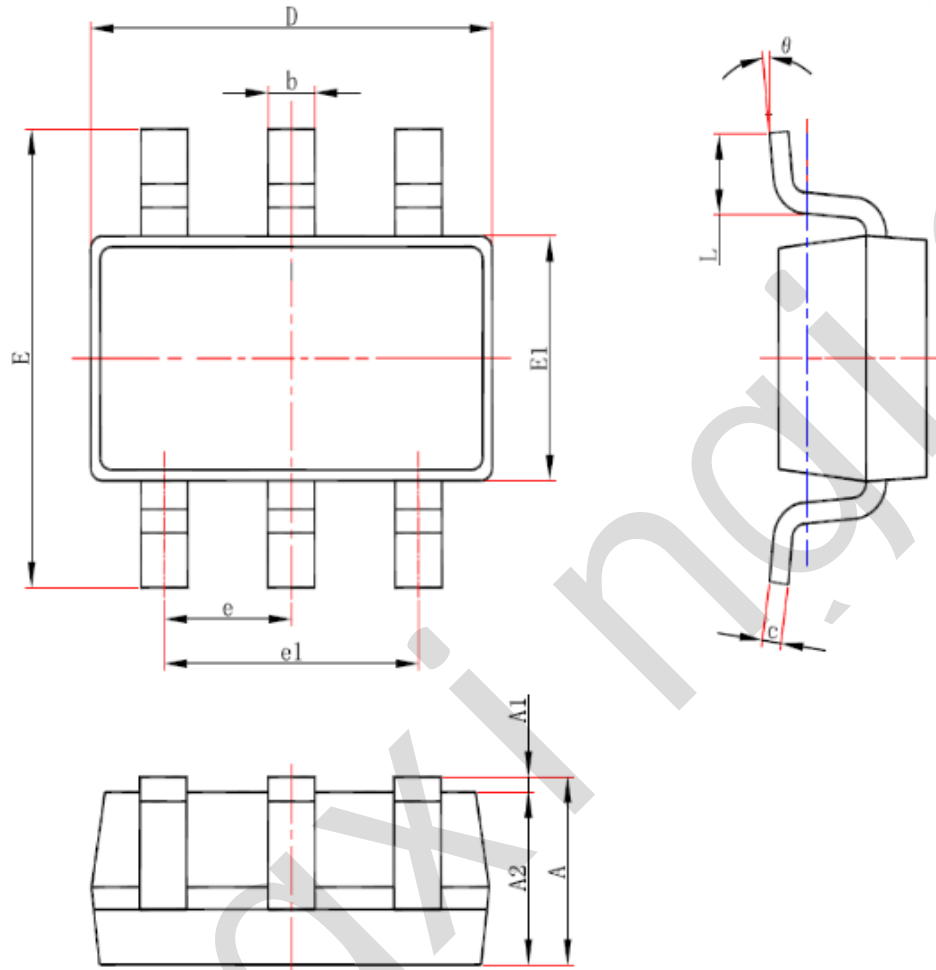
#### 5.6、Pull-up Or Pull-down Resistors On I/O Lines

As mentioned previously the TXB010X is designed with low static drive strength to drive capacitive loads of up to 70pF. To avoid output contention issues, any pull-up or pull-down resistors used must be kept higher than 50k $\Omega$ . For this reason the TXB010X is not recommended for use in open drain driver applications such as 1-Wire or I<sup>2</sup>C. For these applications, the TXS010X level translator is recommended.



## 6、Package Information

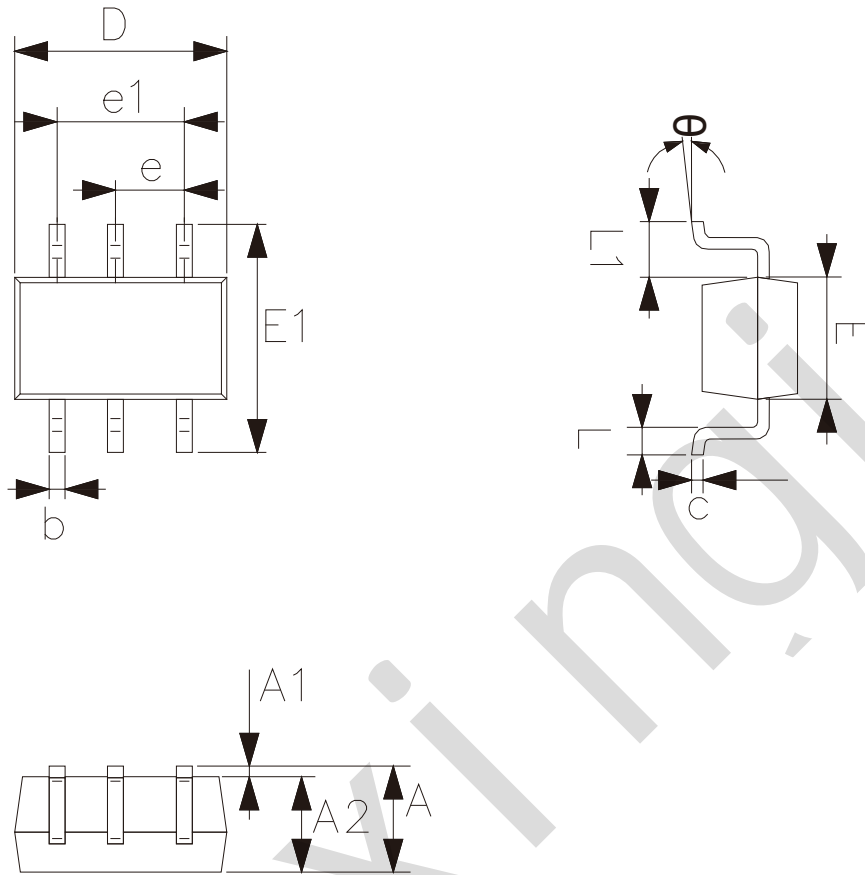
### 6.1、SOT23-6



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.25
A1	0.00	0.12
A2	1.00	1.20
b	0.30	0.50
c	0.10	0.20
D	2.82	3.02
E	2.60	3.00
E1	1.50	1.70
e	0.95	
e1	1.80	2.00
L	0.30	0.60
θ	0°	8°



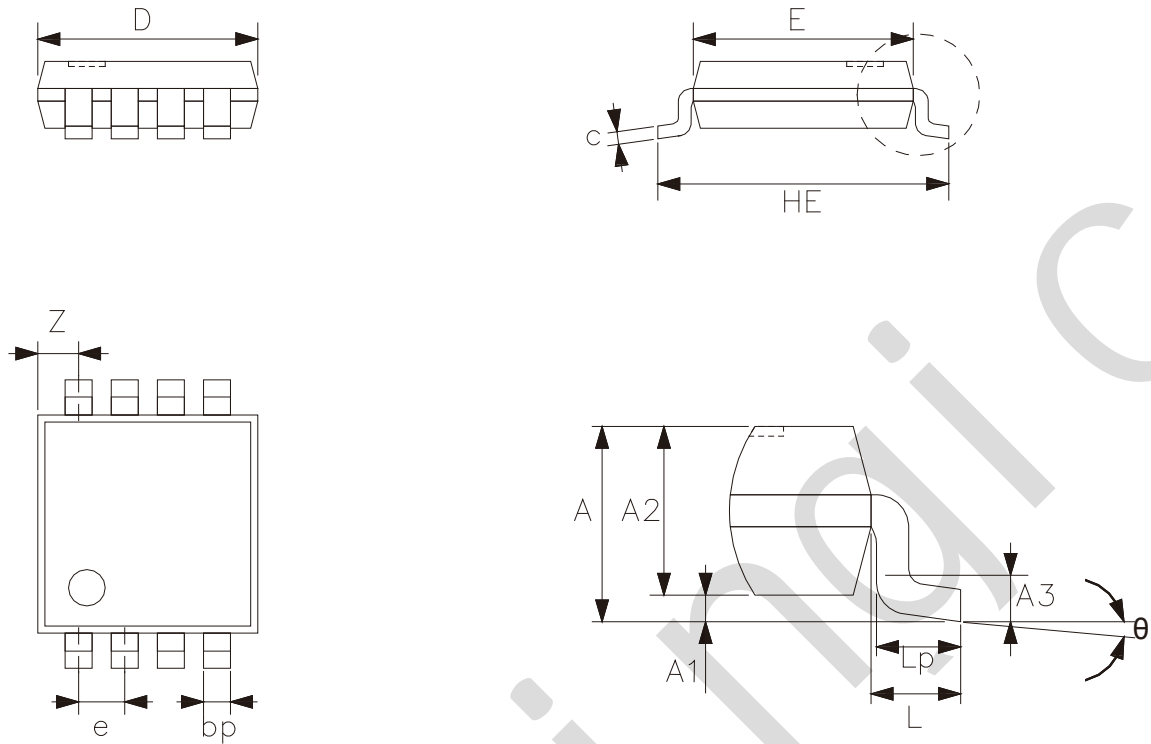
## 6.2、SOT363



Symbol	Dimensions (mm)	
	Min.	Max.
A	0.90	1.10
A1	0.00	0.10
A2	0.90	1.00
b	0.15	0.35
c	0.11	0.175
D	2.00	2.20
E1	2.15	2.45
E	1.15	1.35
e	0.65	
e1	1.20	1.40
L	0.26	0.46
L1	0.525	
$\theta$	0°	8°



### 6.3、TSSOP8

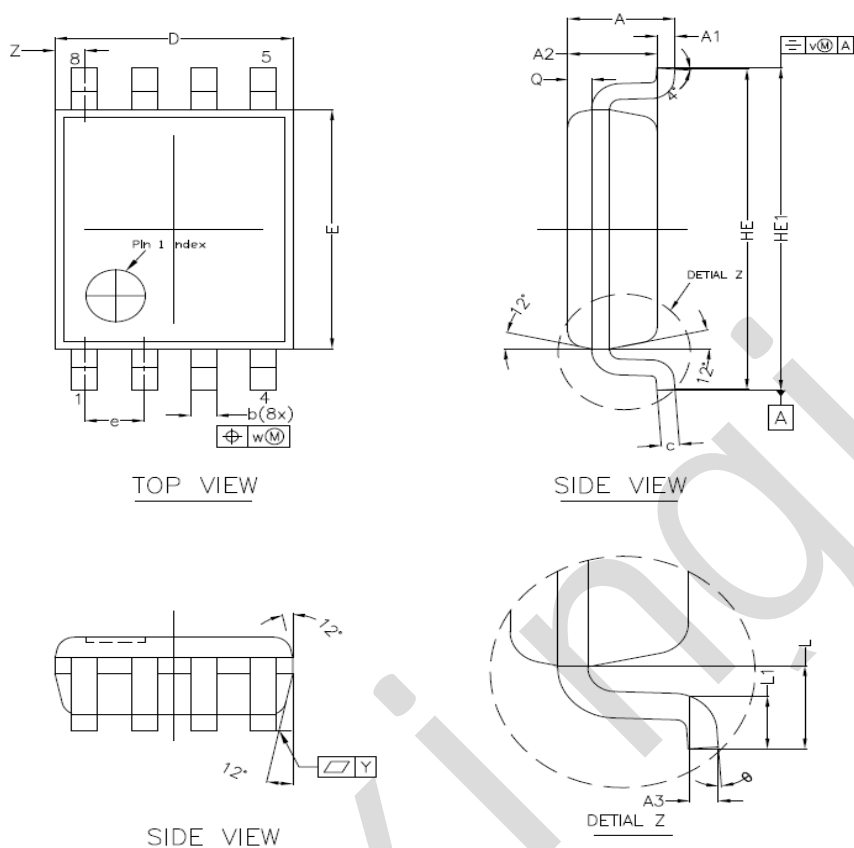


Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.10
A1	0	0.15
A2	0.75	0.95
A3	0.25	
bp	0.22	0.38
c	0.08	0.18
D	2.90	3.10
E	2.90	3.10
HE	3.90	4.10
L	0.50	
Lp	0.33	0.47
e	0.65	
Z	0.35	0.70
$\theta$	0°	8°



灵星芯微 精密制程

6.4. VSSOP8



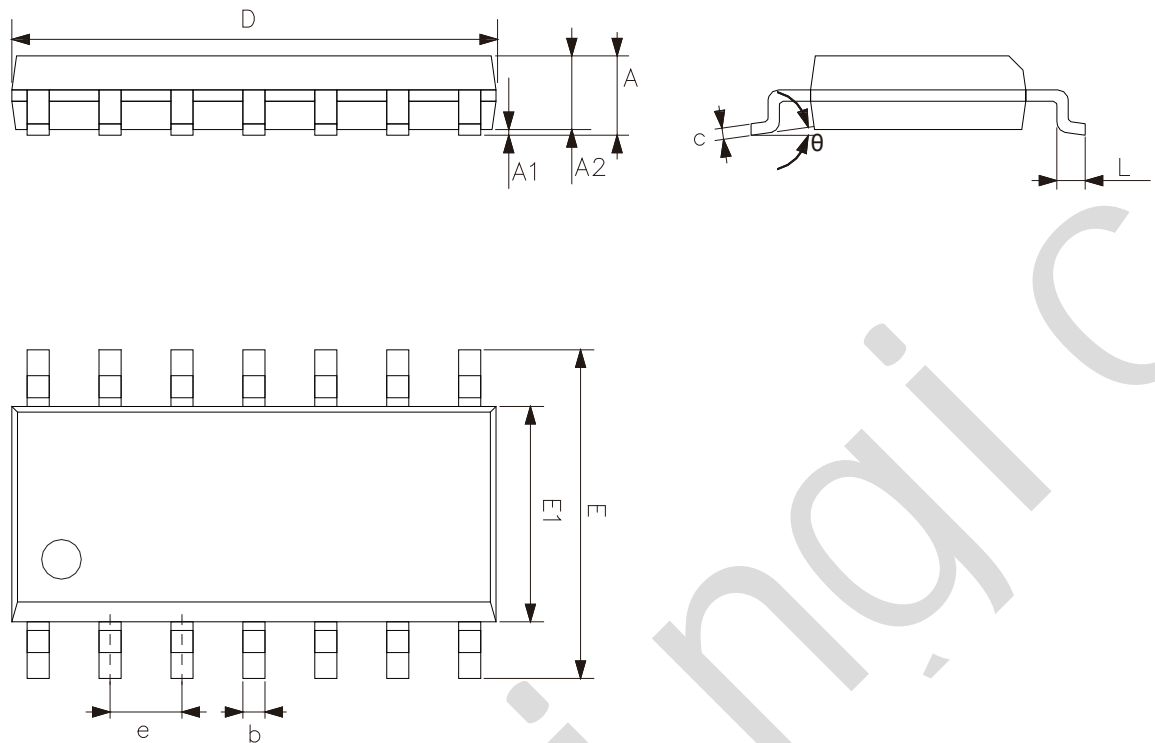
NOTES  
1.0 COP  
DIE ATTA  
2.0 D E

Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.00
A1	0.00	0.15
A2	0.60	0.85
A3	0.12	
Q	0.19	0.21
b	0.17	0.27
c	0.08	0.23
D	1.90	2.10
E	2.20	2.40
HE	3.00	3.20
HE1	3.00	3.40
e	0.50	
L	0.40	
L1	0.15	0.40
Y	0.10	
Z	0.10	0.40
$\theta$	0°	8°



灵星芯微 集成电路

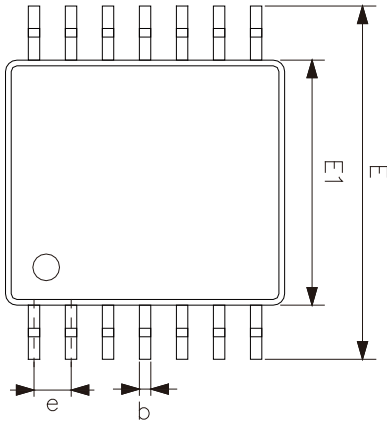
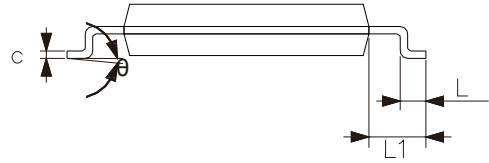
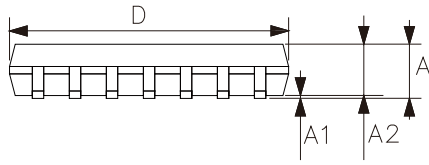
6.5、SOP14



Symbol	Dimensions (mm)	
	Min.	Max.
A	1.50	1.75
A1	0.05	0.25
A2	1.30	-
b	0.33	0.50
c	0.19	0.25
D	8.43	8.76
E	5.80	6.25
E1	3.75	4.00
e	1.27	
L	0.40	0.89
θ	0°	8°



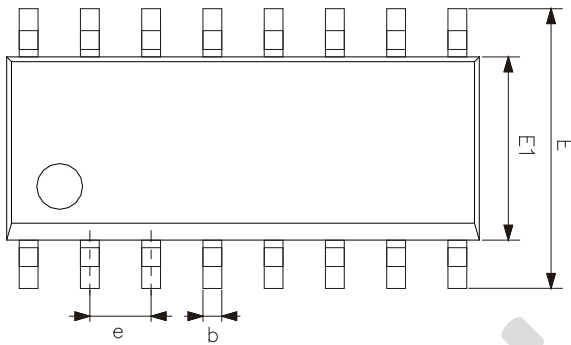
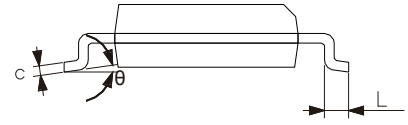
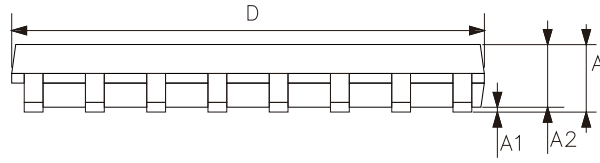
### 6.6. TSSOP14



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
L1	1.00	
$\theta$	0°	8°



### 6.7、SOP16

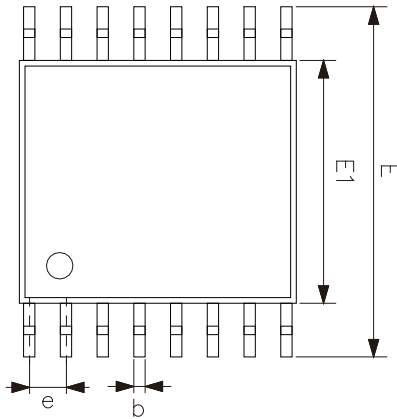
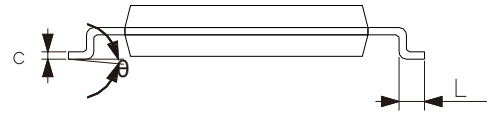
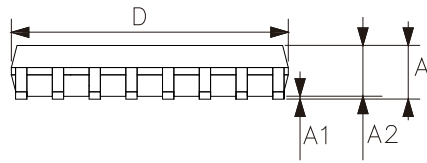


Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
$\theta$	0°	8°





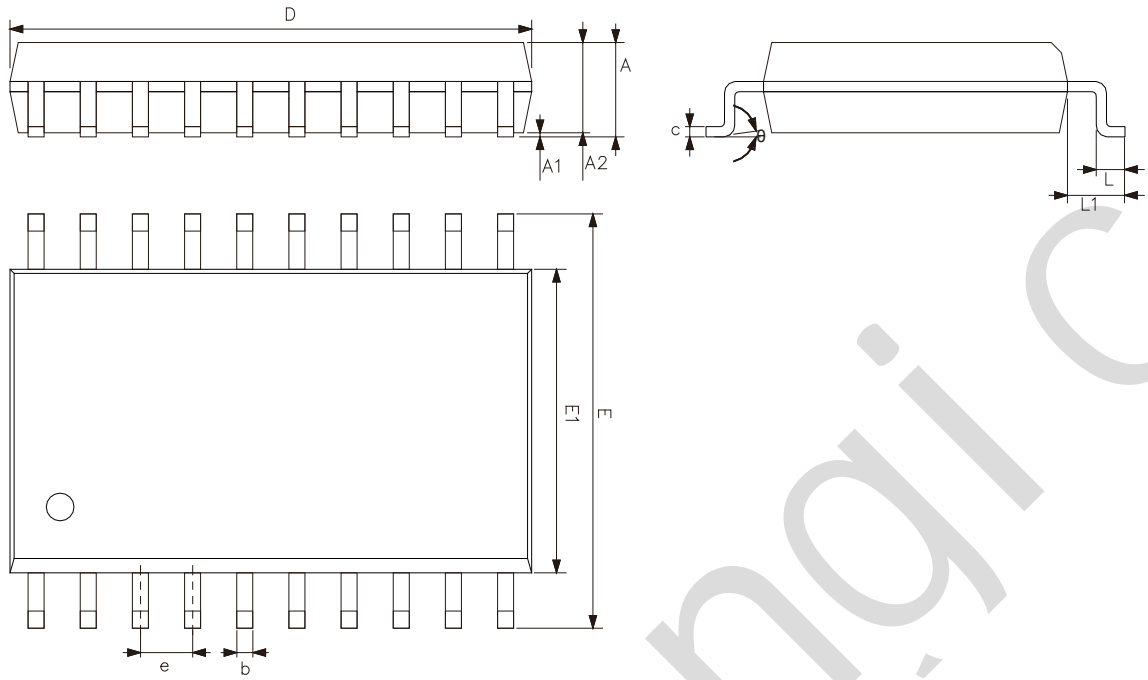
### 6.8、TSSOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
$\theta$	0°	8°



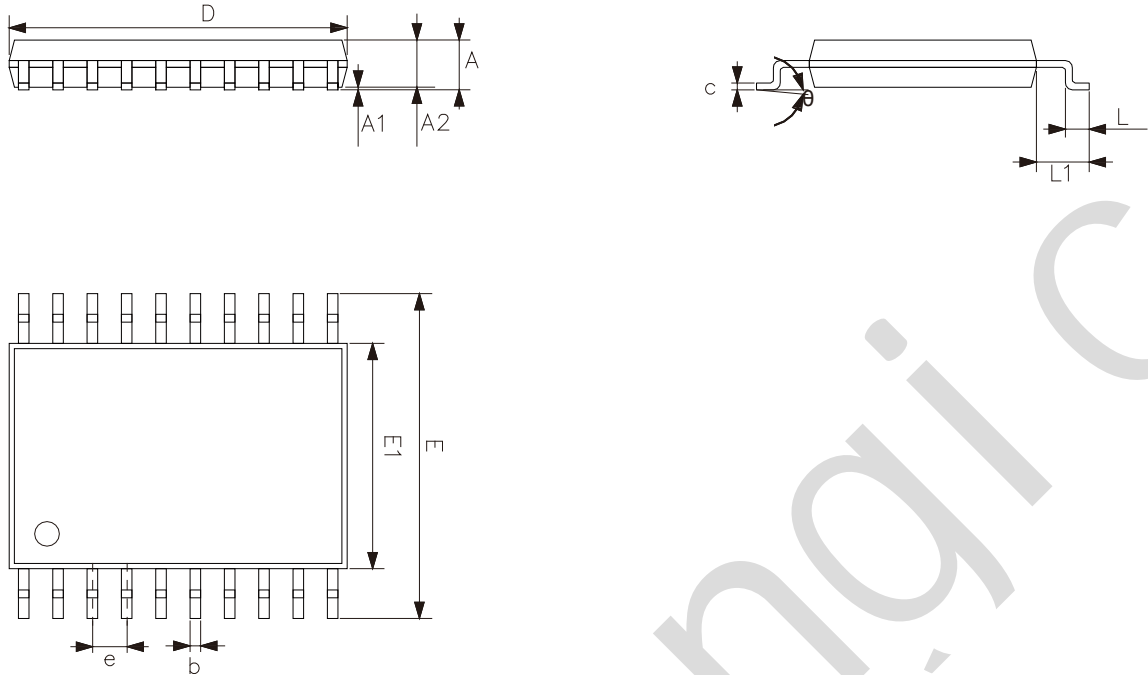
### 6.9、SOP20



Symbol	Dimensions (mm)	
	Min.	Max.
A	2.47	2.65
A1	0.05	0.30
A2	2.20	2.44
b	0.35	0.50
c	0.15	0.30
D	12.54	12.94
E	10.00	10.60
E1	7.30	7.70
e	1.27	
L	0.40	1.05
L1	1.30	1.50
$\theta$	0°	8°



### 6.10、TSSOP20



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
L1	1.00	
$\theta$	0°	8°



## 7、Statements And Notes

### 7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

### 7.2、Notes

We Recommend you to read this chapter carefully before using this product.

The information in this chapter is provided for reference only and Lingxing disclaims any express or implied warranties, including but not limited to applicability, special application or non-infringement of third party rights.

This product is not suitable for critical equipment such as life-saving, life-sustaining or safety equipment. It is also not suitable for applications that may result in personal injury, death, or serious property or environmental damage due to product malfunction or failure. Lingxing will not be liable for any damages incurred by the customers at their own risk for such applications.

The customer is responsible for conducting all necessary tests Lingxing's application to avoid failure in the application or the application of the customer's third party users. Lingxing does not accept any liability.

The Company reserves the right to change or improve the information published in this chapter at any time. The information in this chapter are subject to change without notice. We recommend the customer to consult our sales staff before purchasing.

Please obtain related materials form Lingxing's regular channels and we are not responsible for its content if it is provided by sources other than our company.

In case of any conflict between the Chinese and English version, the version is subject to the Chinese one.