TXS010X （LX)
X-Bit Bidirectional Level-Shifting, Voltage-Level Translator

Product Specification

Specification Revision History：

Version	Date	Description
2021-04-A1	2021-04	New
2023-02-A2	2023-02	Modify the content
2023-05-A3	2023-05	Update the package information
2023-11-A4	2023-11	Update the package information

1、General Description

The TXS010X is a X-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 1-bit input-output ports (A and B), one output enable input (OE) and two supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). $V_{CC(A)}$ can be supplied at any voltage between 1.65V and 3.6V. $V_{CC(B)}$ can be supplied at any voltage between 2.3V and 5.5V. This flexibility makes the device suitable for translating between any of the voltage nodes (1.8V, 2.5V, 3.3V and 5.0V). Pins A and OE are referenced to $V_{CC(A)}$ and pin B is referenced to $V_{CC(B)}$. A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

Features:

- Wide supply voltage range:
  $V_{CC(A)}$: 1.65V to 3.6V
  $V_{CC(B)}$: 2.3V to 5.5V
- Maximum data rates:
  Push-pull: 50 Mbps
  Open-drain: 2 Mbps
- I_{OFF} circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5V
- Specified from -40 to +105℃
- Package:
  TXS0101: SOT23-6/SOT363
  TXS0102: TSSOP8/VSSOP8
  TXS0104: SOP14/TSSOP14
  TXS0108: TSSOP20

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
TXS0102DCT (LX)	TSSOP8	DAXX	100 PCS/tube	200 tube/box	20000 PCS/box	Dimensions of plastic enclosure: 3.0mm×3.0mm Pin spacing: 0.65mm
TXS0104ED (LX)	SOP14	TXS0104	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 1.27mm
TXS0104EP (LX)	TSSOP14	TXS0104	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm
TXS0108EP (LX)	TSSOP20	TXS0108	70 PCS/tube	200 tube/box	14000 PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing: 0.65mm

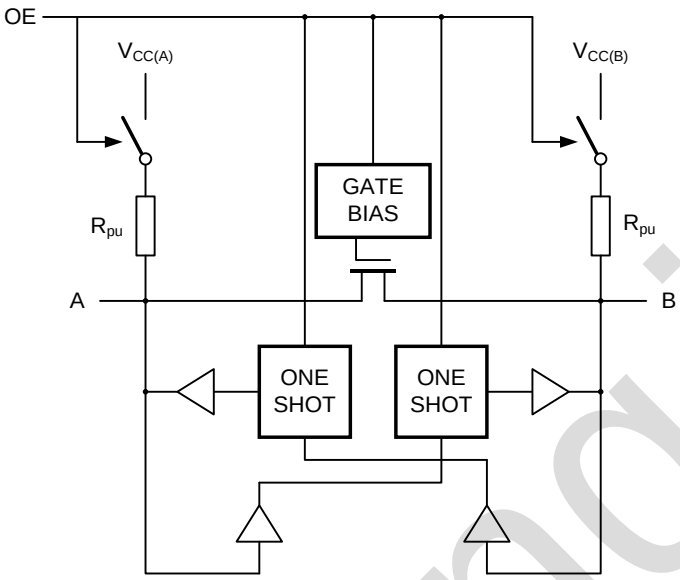
Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
TXS0101DB (LX)	SOT23-6	CZXX	3000 PCS/reel	30000 PCS/box	Dimensions of plastic enclosure: 2.9mm × 1.6mm Pin spacing: 0.95mm
TXS0101DC (LX)	SOT363	CZXX	3000 PCS/reel	30000 PCS/box	Dimensions of plastic enclosure: 2.1mm ×1.3mm Pin spacing: 0.65mm
TXS0102DCT (LX)	TSSOP8	DAXX	3000 PCS/reel	3000 PCS/box	Dimensions of plastic enclosure: 3.0mm ×3.0mm Pin spacing: 0.65mm
TXS0102DCU (LX)	VSSOP8	DAXX	3000 PCS/reel	3000 PCS/box	Dimensions of plastic enclosure: 2.0mm ×2.3mm Pin spacing: 0.50mm
TXS0104EDR (LX)	SOP14	TXS0104	2500 PCS/reel	5000 PCS/box	Dimensions of plastic enclosure: 8.7mm ×3.9mm Pin spacing: 1.27mm
TXS0104EP (LX)	TSSOP14	TXS0104	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm ×4.4mm Pin spacing: 0.65mm
TXS0108EP (LX)	TSSOP20	TXS0108	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 6.5mm ×4.4mm Pin spacing: 0.65mm

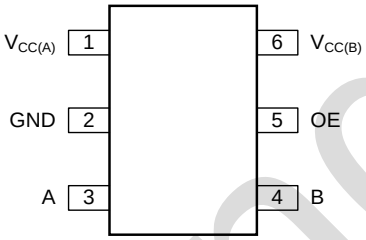
Note 1: “XX” refers to variable content, meaning year and package batch serial number.
Note 2: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

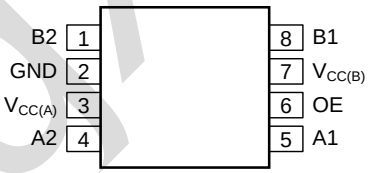
2.1、Block Diagram



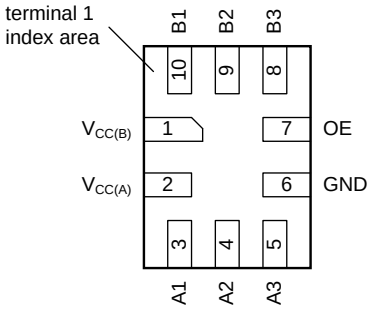
2.2、Pin Configurations



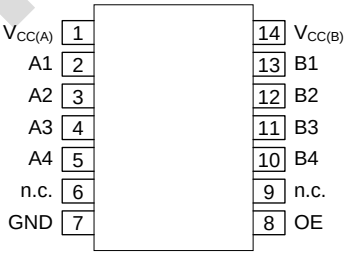
SOT23-6/SOT363



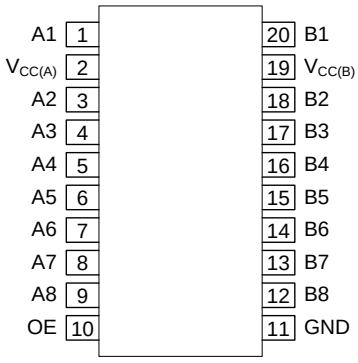
TSSOP8/VSSOP8



QFN10



SOP14/TSSOP14



TSSOP20

2.3、Pin Description

2.3.1、SOT23-6/SOT363

Pin No.	Pin Name	Description
1	$V_{CC(A)}$	supply voltage A
2	GND	ground (0V)
3	A	data input or output (referenced to $V_{CC(A)}$)
4	B	data input or output (referenced to $V_{CC(B)}$)
5	OE	output enable input (active HIGH; referenced to $V_{CC(A)}$)
6	$V_{CC(B)}$	supply voltage B

2.3.2、TSSOP8/VSSOP8

Pin No.	Pin Name	Description
1	B2	data input or output (referenced to $V_{CC(B)}$)
2	GND	ground (0V)
3	$V_{CC(A)}$	supply voltage A
4	A2	data input or output (referenced to $V_{CC(A)}$)
5	A1	data input or output (referenced to $V_{CC(A)}$)
6	OE	output enable input (active HIGH; referenced to $V_{CC(A)}$)
7	$V_{CC(B)}$	supply voltage B
8	B1	data input or output (referenced to $V_{CC(B)}$)

2.3.3、QFN10

Pin No.	Pin Name	Description
1	$V_{CC(B)}$	supply voltage B
2	$V_{CC(A)}$	supply voltage A
3	A1	data input or output (referenced to $V_{CC(A)}$)
4	A2	data input or output (referenced to $V_{CC(A)}$)
5	A3	data input or output (referenced to $V_{CC(A)}$)
6	GND	ground (0V)
7	OE	output enable input (active HIGH; referenced to $V_{CC(A)}$)
8	B3	data input or output (referenced to $V_{CC(B)}$)
9	B2	data input or output (referenced to $V_{CC(B)}$)
10	B1	data input or output (referenced to $V_{CC(B)}$)

2.3.4、SOP14/TSSOP14

Pin No.	Pin Name	Description
1	$V_{CC(A)}$	supply voltage A
2	A1	data input or output (referenced to $V_{CC(A)}$)
3	A2	data input or output (referenced to $V_{CC(A)}$)
4	A3	data input or output (referenced to $V_{CC(A)}$)
5	A4	data input or output (referenced to $V_{CC(A)}$)
6	n.c.	not connected
7	GND	ground (0V)

8	OE	output enable input (active HIGH; referenced to $V_{CC(A)}$)
9	n.c.	not connected
10	B4	data input or output (referenced to $V_{CC(B)}$)
11	B3	data input or output (referenced to $V_{CC(B)}$)
12	B2	data input or output (referenced to $V_{CC(B)}$)
13	B1	data input or output (referenced to $V_{CC(B)}$)
14	$V_{CC(B)}$	supply voltage B

2.3.5、TSSOP20

Pin No.	Pin Name	Description
1	A1	data input or output (referenced to $V_{CC(A)}$)
2	$V_{CC(A)}$	supply voltage A
3	A2	data input or output (referenced to $V_{CC(A)}$)
4	A3	data input or output (referenced to $V_{CC(A)}$)
5	A4	data input or output (referenced to $V_{CC(A)}$)
6	A5	data input or output (referenced to $V_{CC(A)}$)
7	A6	data input or output (referenced to $V_{CC(A)}$)
8	A7	data input or output (referenced to $V_{CC(A)}$)
9	A8	data input or output (referenced to $V_{CC(A)}$)
10	OE	output enable input (active HIGH; referenced to $V_{CC(A)}$)
11	GND	ground (0V)
12	B8	data input or output (referenced to $V_{CC(B)}$)
13	B7	data input or output (referenced to $V_{CC(B)}$)
14	B6	data input or output (referenced to $V_{CC(B)}$)
15	B5	data input or output (referenced to $V_{CC(B)}$)
16	B4	data input or output (referenced to $V_{CC(B)}$)
17	B3	data input or output (referenced to $V_{CC(B)}$)
18	B2	data input or output (referenced to $V_{CC(B)}$)
19	$V_{CC(B)}$	supply voltage B
20	B1	data input or output (referenced to $V_{CC(B)}$)

2.4、Function table

Supply voltage		Input	Input/output	
$V_{CC(A)}$	$V_{CC(B)}$	OE	A	B
1.65V to 3.6V	2.3V to 5.5V	L	Z	Z
1.65V to 3.6V	2.3V to 5.5V	H	input or output	output or input
GND	2.3V to 5.5V	X	Z	Z
1.65V to 3.6V	GND	X	Z	Z

Note:

[1] H=HIGH voltage level; L=LOW voltage level; X=don’t care; Z=high-impedance OFF-state.

[2] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, All voltage referenced to GND, unless otherwise specified)

Characteristic	Symbol	Conditions	Min.	Max.	Unit
supply voltage A	$V_{CC(A)}$	-	-0.5	+6.5	V
supply voltage B	$V_{CC(B)}$	-	-0.5	+6.5	V
input voltage	V_I	OE[1]	-0.5	+6.5	V
		A, B port; Power-down or 3-state mode[1]	-0.5	+6.5	V
		A, B port; Active mode[1][2][3]	-0.5	V_{CCI}+0.5	V
output voltage	V_O	A, B port; Power-down or 3-state mode[1]	-0.5	+6.5	V
		A, B port; Active mode[1][3][4]	-0.5	V_{CCO}+0.5	V
input clamping current	I_{IK}	V_I<0V	-50	-	mA
output clamping current	I_{OK}	V_O<0V	-50	-	mA
output current	I_O	V_O=0V to V_{CCO}[4]	-	±50	mA
supply current	I_{CC}	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
ground current	I_{GND}	-	-100	-	mA
storage temperature	T_{stg}	-	-65	+150	℃
total power dissipation	P_{tot}	-	-	500	mW
soldering temperature	T_L	10s	260		℃

Note:

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output.

[3] V_{CCI}+0.5V or V_{CCO}+0.5V should not exceed 6.5V.

[4] V_{CCO} is the supply voltage associated with the output.

3.2、Recommended operating conditions

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage A	$V_{CC(A)}$	-		1.65	3.6	V
supply voltage B	$V_{CC(B)}$	-		2.3	5.5	V
input voltage	V_I	OE		0	5.5	V
		Power-down or 3-state mode	A port	0	3.6	V
			B port	0	5.5	V
		Active mode	A, B port	0	V_{CCI}	V
output voltage	V_O	Power-down or 3-state mode	A port	0	3.6	V
			B port	0	5.5	V
		Active mode	A, B port	0	V_{CCO}	V
ambient temperature	T_{amb}	-		-40	+105	℃
input transition rise and fall rate	Δt/ΔV	A or B port; push-pull driving	$V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	-	10	ns/V
		OE input	$V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	-	10	ns/V

Note:

[1] The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.

[2] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

[3] V_{CCI} is the supply voltage associated with the input.

[4] V_{CCO} is the supply voltage associated with the output.

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
LOW-level output voltage	V_{OL}	A port; V_I≤0.15V; $V_{CC(B)}$=1.65V to 5.5V; $V_{CC(A)}$=1.65V; I_O=-135uA		-	0.25	-	V
input leakage current	I_I	OE input; V_I=0V to 3.6V; $V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V		-	-	±1	uA
OFF-state output current	I_{OZ}	A or B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V		-	-	±1	uA
power-off leakage current	I_{OFF}	A port; V_I or V_O=0V to 3.6V; $V_{CC(A)}$=0V; $V_{CC(B)}$=0V to 5.5V		-	-	±1	uA
		B port; V_I or V_O=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=0V to 3.6V		-	-	±1	uA
input capacitance	C_I	OE input; $V_{CC(A)}$=3.3V; $V_{CC(B)}$=3.3V		-	2.6	-	pF
input/output capacitance	$C_{I/O}$	A port; $V_{CC(A)}$=3.3V; $V_{CC(B)}$=3.3V	enabled	-	9	-	pF
			disabled	-	5.2	-	pF
		B port; $V_{CC(A)}$=3.3V; $V_{CC(B)}$=3.3V	enabled	-	10.5	-	pF
			disabled	-	9	-	pF
supply current	$I_{CC(A)}$	$V_{CC(A)}$=1.8V	$V_{CC(B)}$=2.5V	-	0.1	-	uA
			$V_{CC(B)}$=3.3V	-	0.1	-	uA
			$V_{CC(B)}$=5.0V	-	0.1	-	uA
		$V_{CC(A)}$=2.5V	$V_{CC(B)}$=2.5V	-	0.1	-	uA
			$V_{CC(B)}$=3.3V	-	0.1	-	uA
			$V_{CC(B)}$=5.0V	-	0.1	-	uA
		$V_{CC(A)}$=3.3V	$V_{CC(B)}$=2.5V	-	-	-	uA
			$V_{CC(B)}$=3.3V	-	0.1	-	uA
			$V_{CC(B)}$=5.0V	-	0.1	-	uA
	$I_{CC(B)}$	$V_{CC(A)}$=1.8V	$V_{CC(B)}$=2.5V	-	0.5	-	uA
			$V_{CC(B)}$=3.3V	-	1.5	-	uA
			$V_{CC(B)}$=5.0V	-	4.6	-	uA
		$V_{CC(A)}$=2.5V	$V_{CC(B)}$=2.5V	-	0.1	-	uA
			$V_{CC(B)}$=3.3V	-	0.8	-	uA
			$V_{CC(B)}$=5.0V	-	3.8	-	uA
		$V_{CC(A)}$=3.3V	$V_{CC(B)}$=2.5V	-	-	-	uA

			$V_{CC(B)}$=3.3V	-	0.1	-	uA
			$V_{CC(B)}$=5.0V	-	2.8	-	uA

Note:

[1] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

[2] V_{CCO} is the supply voltage associated with the output.

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	A port	$V_{CC(A)}$=1.65V to 1.95V; $V_{CC(B)}$=2.3V to 5.5V	$V_{CC(A)}$-0.2	-	-	V
			$V_{CC(A)}$=2.3V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	$V_{CC(A)}$-0.4	-	-	V
		B port	$V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	$V_{CC(B)}$-0.4	-	-	V
		OE input	$V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	0.65$V_{CC(A)}$	-	-	V
LOW-level input voltage	V_{IL}	A or B port	$V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	-	-	0.15	V
		OE input	$V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	-	-	0.35$V_{CC(A)}$	V
HIGH-level output voltage	V_{OH}	A port; I_O=-20uA; V_I≥$V_{CC(B)}$-0.4V	$V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	0.67$V_{CC(A)}$	-	-	V
		B port; I_O=-20uA; V_I≥$V_{CC(A)}$-0.2V	$V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	0.67$V_{CC(B)}$	-	-	V
LOW-level output voltage	V_{OL}	A port; V_I≤0.15V; $V_{CC(B)}$=1.65V to 5.5V	$V_{CC(A)}$=1.65V; I_O=-220uA	-	-	0.4	V
			$V_{CC(A)}$=2.3V; I_O=-300uA	-	-	0.4	V
			$V_{CC(A)}$=3.0V; I_O=-400uA	-	-	0.55	V
		B port; V_I≤0.15V; $V_{CC(A)}$=1.65V to 3.6V	$V_{CC(B)}$=1.65V; I_O=-220uA	-	-	0.4	V
			$V_{CC(B)}$=2.3V; I_O=-300uA	-	-	0.4	V
			$V_{CC(B)}$=3.0V; I_O=-400uA	-	-	0.55	V
			$V_{CC(B)}$=4.5V; I_O=-620uA	-	-	0.55	V
input leakage current	I_I	OE input; V_I=0V to 3.6V; $V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V		-	-	±2	uA
OFF-state output current	I_{OZ}	A or B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V		-	-	±2	uA
power-off leakage current	I_{OFF}	A port; V_I or V_O=0V to 3.6V; $V_{CC(A)}$=0V; $V_{CC(B)}$=0V to 5.5V		-	-	±2	uA
		B port; V_I or V_O=0V to 3.6V; $V_{CC(B)}$=0V; $V_{CC(A)}$=0V to 5.5V		-	-	±2	uA
supply current	I_{CC}	OE=0V or $V_{CC(A)}$; An, Bn open					
		$I_{CC(A)}$	$V_{CC(A)}$=1.65V; $V_{CC(B)}$=1.65V to 5.5V	-5	-	0.5	uA

			$V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	-2	-	1.2	uA
			$V_{CC(A)}$=3.6V; $V_{CC(B)}$=0V	-	-	1.0	uA
			$V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V	-1	-	-	uA
		$I_{CC(B)}$	$V_{CC(A)}$=1.65V; $V_{CC(B)}$=1.65V to 5.5V	-	-	22	uA
			$V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	-	-	20	uA
			$V_{CC(A)}$=3.6V; $V_{CC(B)}$=0V	-1	-	-	uA
			$V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V	-	-	2	uA
		$I_{CC(A)}+I_{CC(B)}$	$V_{CC(A)}$=1.65V; $V_{CC(B)}$=1.65V to 5.5V	-	-	17	uA
			$V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	-	-	20	uA

Note:

[1] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

[2] V_{CCO} is the supply voltage associated with the output.

3.3.3、DC Characteristics 3

(T_{amb}=-40℃ to +105℃, voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	A port	$V_{CC(A)}$=1.65V to 1.95V; $V_{CC(B)}$=2.3V to 5.5V	$V_{CC(A)}$-0.2	-	-	V
			$V_{CC(A)}$=2.3V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	$V_{CC(A)}$-0.4	-	-	V
		B port	$V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	$V_{CC(B)}$-0.4	-	-	V
		OE input	$V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	0.65$V_{CC(A)}$	-	-	V
LOW-level input voltage	V_{IL}	A or B port	$V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	-	-	0.15	V
		OE input	$V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	-	-	0.35$V_{CC(A)}$	V
HIGH-level output voltage	V_{OH}	A port; I_O=-20uA; V_I≥$V_{CC(B)}$-0.4V	$V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	0.67$V_{CC(A)}$	-	-	V
		B port; I_O=-20uA; V_I≥$V_{CC(A)}$-0.2V	$V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	0.67$V_{CC(B)}$	-	-	V
LOW-level output voltage	V_{OL}	A port; V_I≤0.15V; $V_{CC(B)}$=1.65V to 5.5V	$V_{CC(A)}$=1.65V; I_O=-220uA	-	-	0.4	V
			$V_{CC(A)}$=2.3V; I_O=-300uA	-	-	0.4	V
			$V_{CC(A)}$=3.0V; I_O=-400uA	-	-	0.55	V
		B port; V_I≤0.15V; $V_{CC(A)}$=1.65V to 3.6V	$V_{CC(B)}$=1.65V; I_O=-220uA	-	-	0.4	V
			$V_{CC(B)}$=2.3V; I_O=-300uA	-	-	0.4	V
			$V_{CC(B)}$=3.0V; I_O=-400uA	-	-	0.55	V
			$V_{CC(B)}$=4.5V; I_O=-620uA	-	-	0.55	V

input leakage current	I_I	OE input; V_I=0V to 3.6V; $V_{CC(A)}$=1.65V to 1.95V; $V_{CC(B)}$=2.3V to 5.5V		-	-	±12	uA
OFF-state output current	I_{OZ}	A or B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=1.65V to 1.95V; $V_{CC(B)}$=2.3V to 5.5V		-	-	±12	uA
power-off leakage current	I_{OFF}	A port; V_I or V_O=0V to 3.6V; $V_{CC(A)}$=0V; $V_{CC(B)}$=0V to 5.5V		-	-	±12	uA
		B port; V_I or V_O=0V to 3.6V; $V_{CC(B)}$=0V; $V_{CC(A)}$=0V to 5.5V		-	-	±12	uA
supply current	I_{CC}	OE=0V or $V_{CC(A)}$; An, Bn open					
		$I_{CC(A)}$	$V_{CC(A)}$=1.65V; $V_{CC(B)}$=1.65V to 5.5V	-5	-	1	uA
			$V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	-2	-	2	uA
			$V_{CC(A)}$=3.6V; $V_{CC(B)}$=0V	-	-	2	uA
			$V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V	-1	-	-	uA
		$I_{CC(B)}$	$V_{CC(A)}$=1.65V; $V_{CC(B)}$=1.65V to 5.5V	-	-	60	uA
			$V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	-	-	20	uA
			$V_{CC(A)}$=3.6V; $V_{CC(B)}$=0V	-1	-	-	uA
			$V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V	-	-	12	uA
		$I_{CC(A)}+I_{CC(B)}$	$V_{CC(A)}$=1.65V; $V_{CC(B)}$=1.65V to 5.5V	-	-	65	uA
			$V_{CC(A)}$=1.65V to 3.6V; $V_{CC(B)}$=2.3V to 5.5V	-	-	20	uA

Note:

[1] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

[2] V_{CCO} is the supply voltage associated with the output.

3.3.4、AC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions	$V_{CC(B)}$				Unit
			1.8V± 0.15V	2.5V± 0.2V	3.3V± 0.3V	5.0V± 0.5V	
HIGH to LOW propagation delay	t_{PHL}	A to B	6.5	5.9	5.7	5.5	ns
LOW to HIGH propagation delay	t_{PLH}	A to B	7.1	6.3	6.2	6.6	ns
HIGH to LOW propagation delay	t_{PHL}	B to A	6.2	5.4	5.1	5	ns
LOW to HIGH propagation delay	t_{PLH}	B to A	5.6	4.1	3.6	3.2	ns
enable time	t_{en}	OE to A; B[1]	200	200	200	200	ns
disable time	t_{dis}	OE to A; no external load[1][2]	12	12	12	12	ns
		OE to B; no external load[2]	12	12	12	12	ns
		OE to A; see Figure 3	90	90	90	90	ns
		OE to B; see Figure 3	95	75	100	75	ns
LOW to HIGH output transition time	t_{TLH}	A port	6.5	5.2	4.8	4.4	ns
		B port	6.6	4.3	2.1	1.5	ns
HIGH to LOW output transition time	t_{THL}	A port	5.8	4.8	4.3	3.8	ns
		B port	3.6	2.2	1.8	1.5	ns
output skew time	$t_{sk(o)}$	between channels[3]	1	1	1	1	ns
pulse width	t_W	data inputs	20	16.7	16.7	16.7	ns
data rate	f_{data}	-	50	60	60	60	Mbps

Note:

[1] t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[2] These values are guaranteed by design.

[3] Skew between any two outputs of the same package switching in the same direction.

3.3.5、AC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions	$V_{CC(B)}$								Unit
			1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$V_{CC(A)}$=1.8V±0.15V											
HIGH to LOW propagation delay	t_{PHL}	A to B	-	9.7	-	7.3	-	6.5	-	5.9	ns
LOW to HIGH propagation delay	t_{PLH}	A to B	-	11.3	-	8.4	-	7.4	-	6.5	ns
HIGH to LOW propagation delay	t_{PHL}	B to A	-	9.8	-	8.0	-	7.4	-	7.0	ns
LOW to HIGH propagation delay	t_{PLH}	B to A	-	10.2	-	7.0	-	5.8	-	5.0	ns
enable time	t_{en}	OE to A; B[1]	-	200	-	200	-	200	-	200	ns
disable time	t_{dis}	OE to A; no external load[1][2]	-	13	-	13	-	13	-	13	ns
		OE to B; no external load[2]	-	16	-	13	-	13	-	13	ns
		OE to A; see Figure 3	-	140	-	140	-	140	-	145	ns
		OE to B; see Figure 3	-	165	-	125	-	175	-	125	ns
LOW to HIGH output transition time	t_{TLH}	A port	2.2	11.9	2.0	8.6	1.9	7.8	1.9	7.2	ns
		B port	2.8	12.2	1.8	7.7	1.2	5.3	0.7	2.9	ns
HIGH to LOW output transition time	t_{THL}	A port	1.8	8.8	1.3	6.6	0.9	5.7	0.6	4.9	ns
		B port	1.3	8.3	1.0	5.4	0.9	3.9	0.7	3.0	ns
output skew	$t_{sk(o)}$	between channels[3]	-	1	-	1	-	1	-	1	ns
pulse width	t_W	data inputs	22.2	-	16.7	-	16.7	-	16.7	-	ns
data rate	f_{data}	-	-	45	-	60	-	60	-	60	Mbps
$V_{CC(A)}$=2.5V±0.2V											
HIGH to LOW propagation delay	t_{PHL}	A to B	-	-	-	6.2	-	5.3	-	4.7	ns
LOW to HIGH propagation delay	t_{PLH}	A to B	-	-	-	6.8	-	5.9	-	5.2	ns
HIGH to LOW propagation delay	t_{PHL}	B to A	-	-	-	5.9	-	4.8	-	4.2	ns

LOW to HIGH propagation delay	t_{PLH}	B to A	-	-	-	6.2	-	4.6	-	3.6	ns
enable time	t_{en}	OE to A; B[1]	-	-	-	200	-	200	-	200	ns
disable time	t_{dis}	OE to A; no external load[1][2]	-	-	-	9	-	9	-	9	ns
		OE to B; no external load[2]	-	-	-	11	-	9	-	9	ns
		OE to A	-	-	-	105	-	105	-	105	ns
		OE to B	-	-	-	125	-	175	-	120	ns
LOW to HIGH output transition time	t_{TLH}	A port	-	-	1.7	7.3	1.7	6.4	1.8	5.8	ns
		B port	-	-	1.8	7.3	1.3	5.4	0.8	3.3	ns
HIGH to LOW output transition time	t_{THL}	A port	-	-	1.3	5.7	0.8	4.7	0.6	3.8	ns
		B port	-	-	1.1	5.4	0.9	4.1	0.7	3.0	ns
output skew time	$t_{sk(o)}$	between channels[3]	-	-	-	1	-	1.2	-	1	ns
pulse width	t_W	data inputs	-	-	14	-	11	-	11	-	ns
data rate	f_{data}	-	-	-	-	70	-	90	-	90	Mbps
$V_{CC(A)}$=3.3V ±0.3V											
HIGH to LOW propagation delay	t_{PHL}	A to B	-	-	-	-	-	4.9	-	4.2	ns
LOW to HIGH propagation delay	t_{PLH}	A to B	-	-	-	-	-	5.2	-	4.6	ns
HIGH to LOW propagation delay	t_{PHL}	B to A	-	-	-	-	-	4.7	-	3.8	ns
LOW to HIGH propagation delay	t_{PLH}	B to A	-	-	-	-	-	4.7	-	4.3	ns
enable time	t_{en}	OE to A; B[1]	-	-	-	-	-	200	-	200	ns
disable time	t_{dis}	OE to A; no external load[1][2]	-	-	-	-	-	8	-	8	ns
		OE to B; no external load[2]	-	-	-	-	-	8	-	8	ns
		OE to A	-	-	-	-	-	150	-	150	ns
		OE to B	-	-	-	-	-	170	-	120	ns
LOW to HIGH output transition time	t_{TLH}	A port	-	-	-	-	1.6	5.7	1.8	5.0	ns
		B port	-	-	-	-	1.5	5.4	0.9	3.9	ns
HIGH to LOW output transition time	t_{THL}	A port	-	-	-	-	1.0	4.5	0.6	3.5	ns
		B port	-	-	-	-	1.0	4.2	0.8	3.1	ns

output skew time	$t_{sk(o)}$	between channels[3]	-	-	-	-	-	1	-	1	ns
pulse width	t_W	data inputs	-	-	-	-	11	-	9	-	ns
data rate	f_{data}	-	-	-	-	-	-	90	-	110	Mbps

Note:

[1] t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[2] These values are guaranteed by design.

[3] Skew between any two outputs of the same package switching in the same direction.

3.3.6、AC Characteristics 3

(T_{amb}=-40℃ to +105℃, voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	**Symbol**	**Conditions**	**$V_{CC(B)}$**								**Unit**
			1.8V±0.15V		**2.5V±0.2V**		**3.3V±0.3V**		**5.0V±0.5V**		
			Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
$V_{CC(A)}$=1.8V±0.15V											
HIGH to LOW propagation delay	t_{PHL}	A to B	-	12.1	-	9.1	-	8.1	-	7.4	ns
LOW to HIGH propagation delay	t_{PLH}	A to B	-	14.1	-	10.5	-	9.3	-	8.1	ns
HIGH to LOW propagation delay	t_{PHL}	B to A	-	12.3	-	10.0	-	9.3	-	8.8	ns
LOW to HIGH propagation delay	t_{PLH}	B to A	-	12.8	-	8.8	-	7.3	-	6.3	ns
enable time	t_{en}	OE to A; B[1]	-	200	-	200	-	200	-	200	ns
disable time	t_{dis}	OE to A; no external load[1][2]	-	14	-	14	-	14	-	14	ns
		OE to B; no external load[2]	-	17	-	14	-	14	-	14	ns
		OE to A; see Figure 3	-	140	-	140	-	140	-	145	ns
		OE to B; see Figure 3	-	165	-	125	-	175	-	125	ns
LOW to HIGH output transition time	t_{TLH}	A port	2.2	14.9	2.0	10.8	1.9	9.8	1.9	9.0	ns
		B port	2.8	15.3	1.8	9.6	1.2	6.6	0.7	3.6	ns
HIGH to LOW output transition time	t_{THL}	A port	1.8	11.0	1.3	8.3	0.9	7.1	0.6	6.1	ns
		B port	1.3	10.4	1.0	6.8	0.9	4.9	0.7	3.8	ns
output skew	$t_{sk(o)}$	between channels[3]	-	1.1	-	1.1	-	1.1	-	1.1	ns
pulse width	t_W	data inputs	25	-	20	-	20	-	20	-	ns
data rate	f_{data}	-	-	40	-	50	-	50	-	50	Mbps
$V_{CC(A)}$=2.5V±0.2V											

HIGH to LOW propagation delay	t_{PHL}	A to B	-	-	-	7.8	-	6.6	-	5.9	ns
LOW to HIGH propagation delay	t_{PLH}	A to B	-	-	-	8.5	-	7.4	-	6.5	ns
HIGH to LOW propagation delay	t_{PHL}	B to A	-	-	-	7.4	-	6.0	-	5.3	ns
LOW to HIGH propagation delay	t_{PLH}	B to A	-	-	-	7.8	-	5.8	-	4.5	ns
enable time	t_{en}	OE to A; B[1]	-	-	-	200	-	200	-	200	ns
disable time	t_{dis}	OE to A; no external load[1][2]	-	-	-	10	-	10	-	10	ns
		OE to B; no external load[2]	-	-	-	12	-	10	-	10	ns
		OE to A	-	-	-	105	-	105	-	105	ns
		OE to B	-	-	-	125	-	175	-	120	ns
LOW to HIGH output transition time	t_{TLH}	A port	-	-	1.7	9.1	1.7	8.0	1.8	7.3	ns
		B port	-	-	1.8	9.1	1.3	6.8	0.9	4.1	ns
HIGH to LOW output transition time	t_{THL}	A port	-	-	1.3	7.1	0.8	5.9	0.6	4.8	ns
		B port	-	-	1.1	6.8	0.9	5.1	0.7	3.8	ns
output skew time	$t_{sk(o)}$	between channels[3]	-	-	-	1.1	-	1.3	-	1.1	ns
pulse width	t_W	data inputs	-	-	16.7	-	12.5	-	12.5	-	ns
data rate	f_{data}	-	-	-	-	60	-	80	-	80	Mbps
$V_{CC(A)}$=3.3V±0.3V											
HIGH to LOW propagation delay	t_{PHL}	A to B	-	-	-	-	-	6.1	-	5.3	ns
LOW to HIGH propagation delay	t_{PLH}	A to B	-	-	-	-	-	6.5	-	5.8	ns
HIGH to LOW propagation delay	t_{PHL}	B to A	-	-	-	-	-	5.9	-	4.8	ns
LOW to HIGH propagation delay	t_{PLH}	B to A	-	-	-	-	-	5.9	-	5.4	ns
enable time	t_{en}	OE to A; B[1]	-	-	-	-	-	200	-	200	ns
disable time	t_{dis}	OE to A; no external load[1][2]	-	-	-	-	-	9	-	9	ns
		OE to B; no external load[2]	-	-	-	-	-	9	-	9	ns

		OE to A	-	-	-	-	-	150	-	150	ns
		OE to B	-	-	-	-	-	170	-	120	ns
LOW to HIGH output transition time	t_{TLH}	A port	-	-	-	-	1.6	7.1	1.8	6.3	ns
		B port	-	-	-	-	1.5	6.8	0.9	4.9	ns
HIGH to LOW output transition time	t_{THL}	A port	-	-	-	-	1.0	5.6	0.7	4.4	ns
		B port	-	-	-	-	1.0	5.3	0.8	3.9	ns
output skew time	$t_{sk(o)}$	between channels[3]	-	-	-	-	-	1.1	-	1.1	ns
pulse width	t_W	data inputs	-	-	-	-	13	-	10	-	ns
data rate	f_{data}	-	-	-	-	-	-	80	-	100	Mbps

Note:

[1] t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[2] These values are guaranteed by design.

[3] Skew between any two outputs of the same package switching in the same direction.

4、Testing Circuit

4.1、AC Testing Circuit

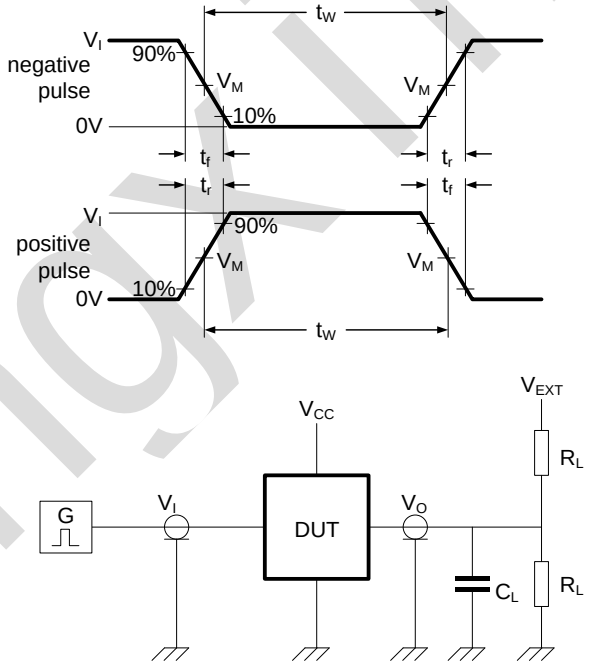


Figure 1. Test circuit for measuring switching times

All input pulses are supplied by generators having the following characteristics: PRR≤10MHz; Z_O=50Ω; dV/dt≥1.0V/ns.

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

V_{EXT}=External voltage for measuring switching times.

4.2、AC Testing Waveforms

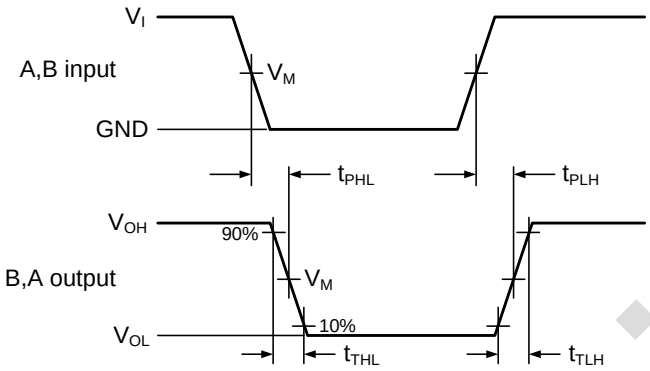


Figure 2. The data input (A, B) to data output (B, A) propagation delay times

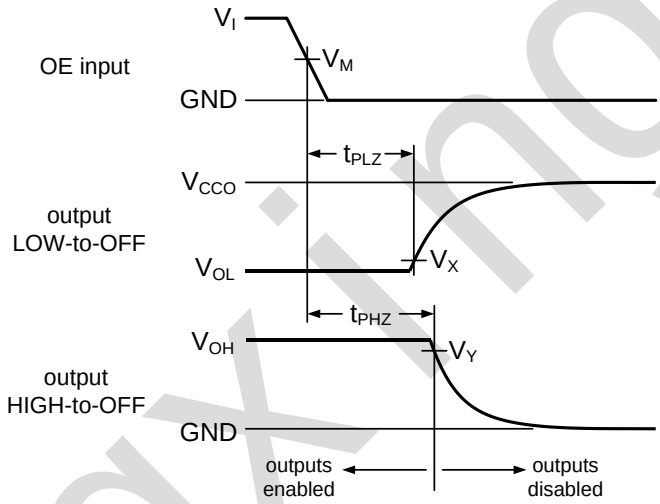
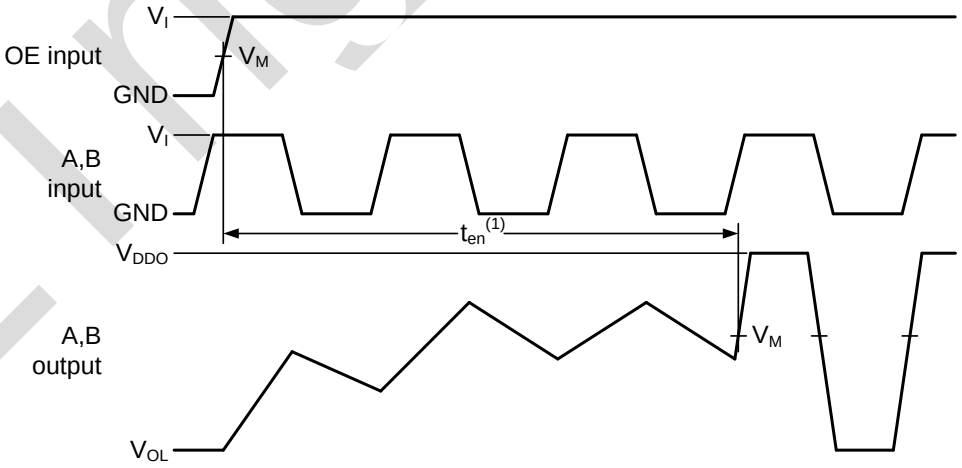


Figure 3. Disable times



(1) The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. See also Section 5.6.

Figure 4. Enable times

4.3、Measurement Points

Supply voltage	Input	Output		
V_{CCO}	V_M	V_M	V_X	V_Y
1.8V±0.15V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.15V	V_{OH}-0.15V
2.5V±0.2V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.15V	V_{OH}-0.15V
3.3V±0.3V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.3V	V_{OH}-0.3V
5.0V±0.5V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.3V	V_{OH}-0.3V

Note:

[1] V_{CCI} is the supply voltage associated with the input.

[2] V_{CCO} is the supply voltage associated with the output.

4.4、Test Data

Supply voltage		Input		Load		V_{EXT}		
$V_{CC(A)}$	$V_{CC(B)}$	V_I	$\Delta t/\Delta V$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65V to 3.6V	2.3V to 5.5V	V_{CCI}	≤1.0ns/V	15pF	50kΩ, 1MΩ	open	open	$2V_{CCO}$

Note:

[1] V_{CCI} is the supply voltage associated with the input.

[2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R_L=1MΩ. For measuring enable and disable times, R_L=50KΩ.

[3] V_{CCO} is the supply voltage associated with the output.

5、Typical Application Circuit And Application Note

5.1、Voltage Level-translation Applications

The TXS010X can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device is primarily targeted at I^2C or 1-wire which use open-drain drivers, it may also be used in applications where push-pull drivers are connected to the ports, however the TXB010X may be more suitable.

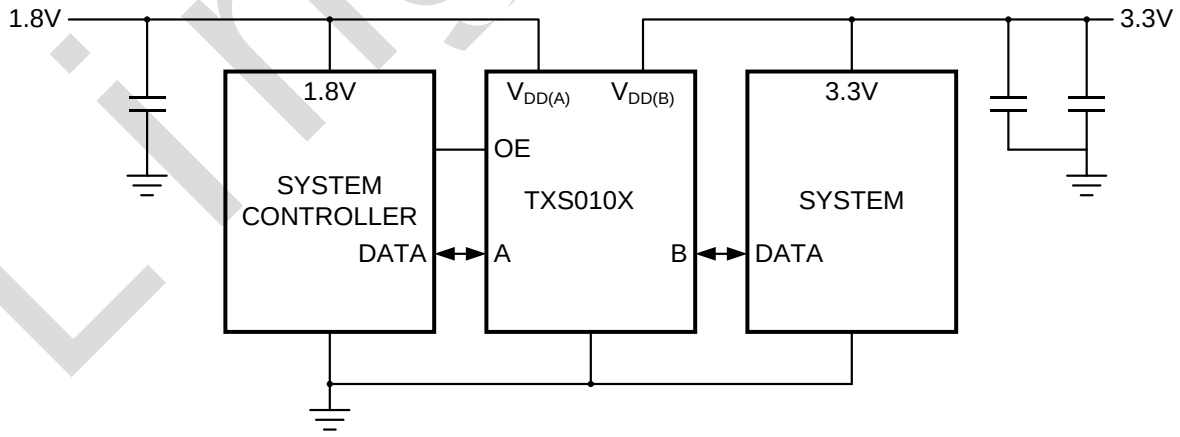


Figure 5. Typical operating circuit

5.2、Architecture

The architecture of the TXS010X is shown in Figure 6. The device does not require an extra input signal to control the direction of data flow from A to B or B to A.

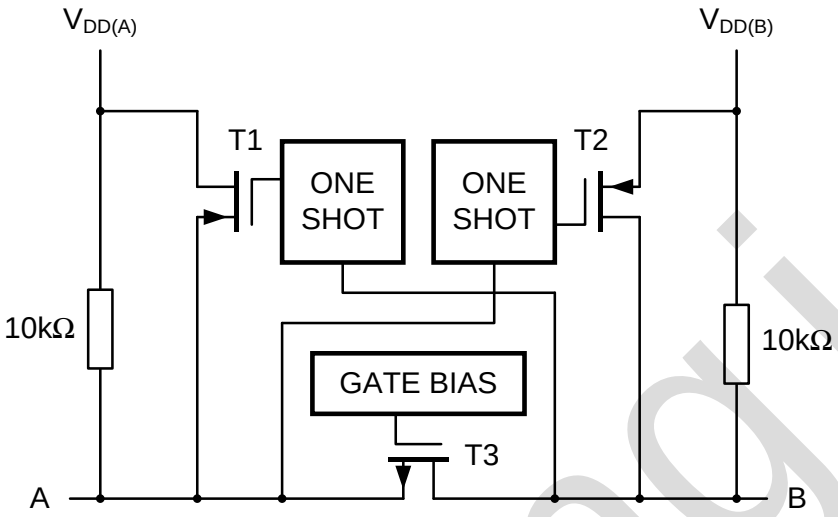


Figure 6. Architecture of TXS010X I/O cell (one channel)

The TXS010X is a "switch" type voltage translator, it employs two key circuits to enable voltage translation:

1. A pass-gate transistor (N-channel) that ties the ports together.
2. An output edge-rate accelerator that detects and accelerates rising edges on the I/O pins.

The gate bias voltage of the pass gate transistor (T3) is set at approximately one threshold voltage above the V_{CC} level of the low-voltage side. During a LOW-to-HIGH transition the output one-shot accelerates the output transition by switching on the PMOS transistors (T1, T2) bypassing the 10KΩ pull-up resistors and increasing current drive capability. The one-shot is activated once the input transition reaches approximately $V_{CCI}/2$; it is de-activated approximately 50ns after the output reaches $V_{CCO}/2$. During the acceleration time the driver output resistance is between approximately 50Ω and 70Ω. To avoid signal contention and minimize dynamic I_{DD}, the user should wait for the one-shot circuit to turn-off before applying a signal in the opposite direction. Pull-up resistors are included in the device for DC current sourcing capability.

5.3、Input Driver Requirements

As the TXS010X is a switch type translator, properties of the input driver directly effect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system; the max data rate, HIGH-to-LOW output transition time (t_{THL}) and propagation delay (t_{PHL}) are dependent upon the output impedance and edge-rate of the external driver. The limits provided for these parameters in the datasheet assume a driver with output impedance below 50Ω is used.

5.4、Output Load Considerations

The maximum lumped capacitive load that can be driven is dependant upon the one-shot pulse duration. In cases with very heavy capacitive loading there is a risk that the output will not reach the positive rail within the one-shot pulse duration. To avoid excessive capacitive loading and to ensure correct triggering of the one-shot it's recommended to use short trace lengths and low capacitance connectors on TXS010X PCB layouts. To ensure low impedance termination and avoid output signal oscillations and one-shot re-triggering, the length of the PCB trace should be such that the round trip delay of any reflection is within the one-shot pulse duration (approximately 50ns).

5.5、Power Up

During operation $V_{CC(A)}$ must never be higher than $V_{CC(B)}$, however during power-up $V_{CC(A)} \geq V_{CC(B)}$ does not damage the device, so either power supply can be ramped up first. There is no special power-up sequencing required. The TXS010X includes circuitry that disables all output ports when either $V_{CC(A)}$or $V_{CC(B)}$ is switched off.

5.6、Enable And Disable

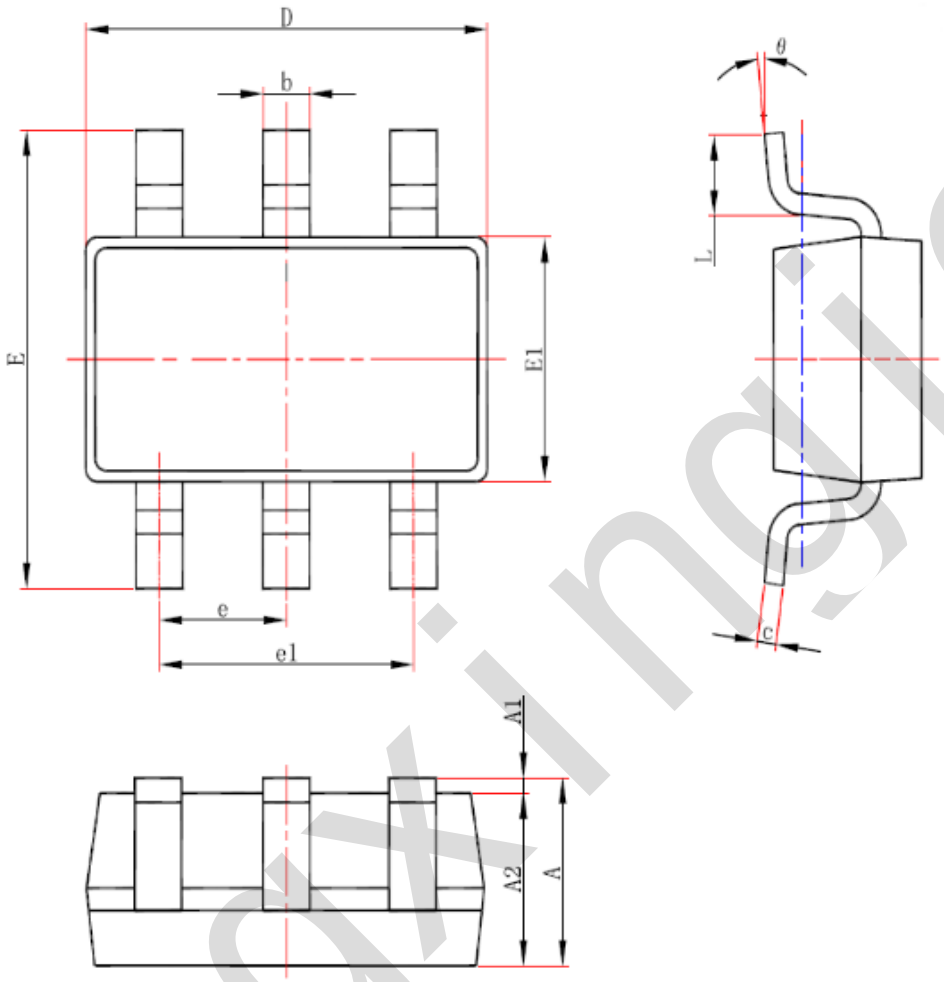
An output enable input (OE) is used to disable the device. Setting OE=LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor, the minimum value of the resistor is determined by the current-sourcing capability of the driver.

5.7、Pull-up Or Pull-down Resistors On I/O Lines

The TXS010X has the pull-up resistors dynamically change value based on whether a low or a high is being passed through the I/O line. Each A-port I/O has a pull-up resistor (R_{PUA}) to V_{CCA} and each B-port I/O has a pull-up resistor (R_{PUB}) to V_{CCB}. R_{PUA} and R_{PUB} have a value of 40kΩ when the output is driving LOW. R_{PUA} and R_{PUB} have a value of 4kΩ when the output is driving HIGH. R_{PUA} and R_{PUB} are disabled when OE=LOW. This feature provides lower static power consumption (when the I/Os are passing a LOW) and supports lower V_{OL} values for the same size pass-gate transistor and helps improve simultaneous switching performance.

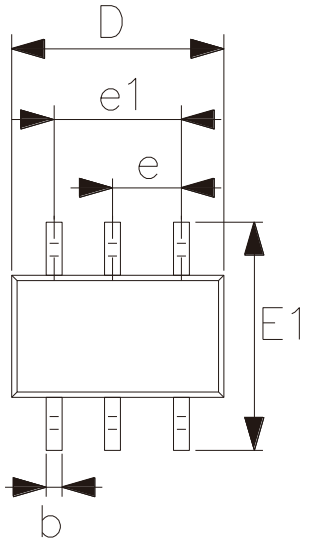
6、Package Information

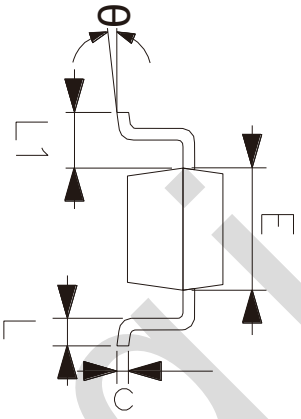
6.1、SOT23-6

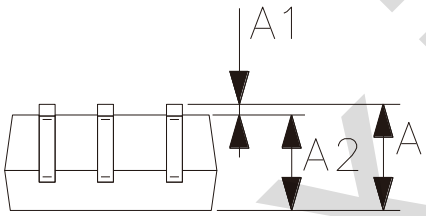


Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.25
A1	0.00	0.12
A2	1.00	1.20
b	0.30	0.50
c	0.10	0.20
D	2.82	3.02
E	2.60	3.00
E1	1.50	1.70
e	0.95	
e1	1.80	2.00
L	0.30	0.60
θ	0°	8°

6.2、SOT-363

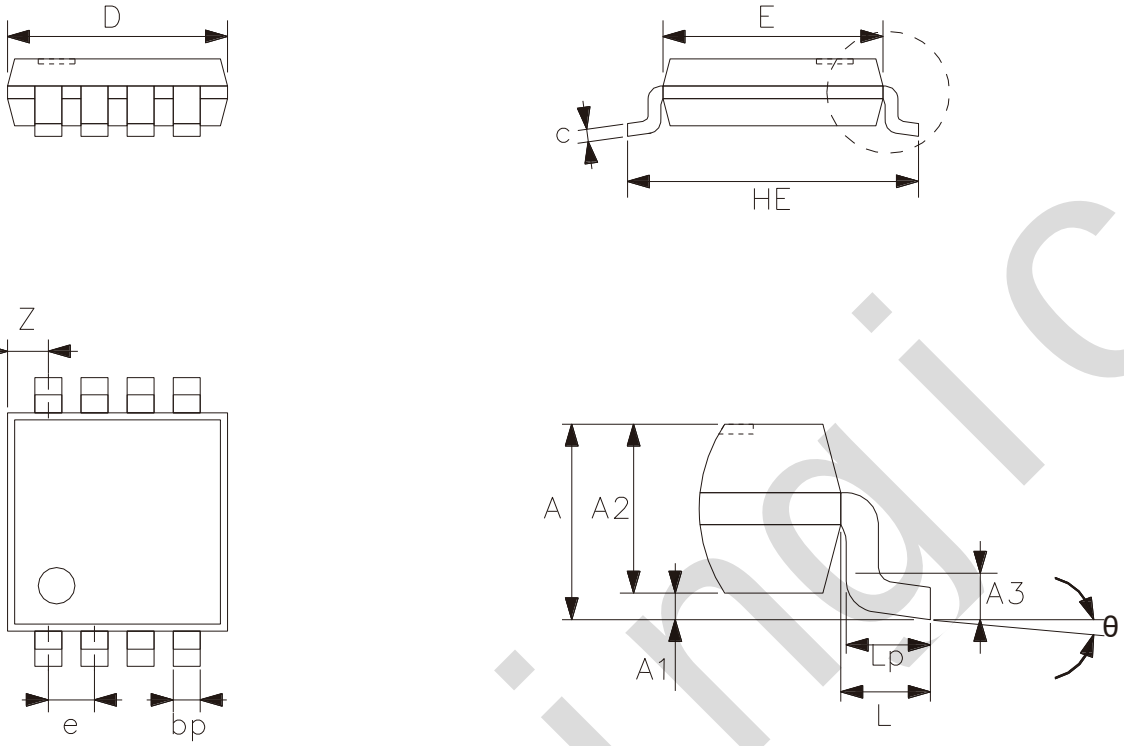






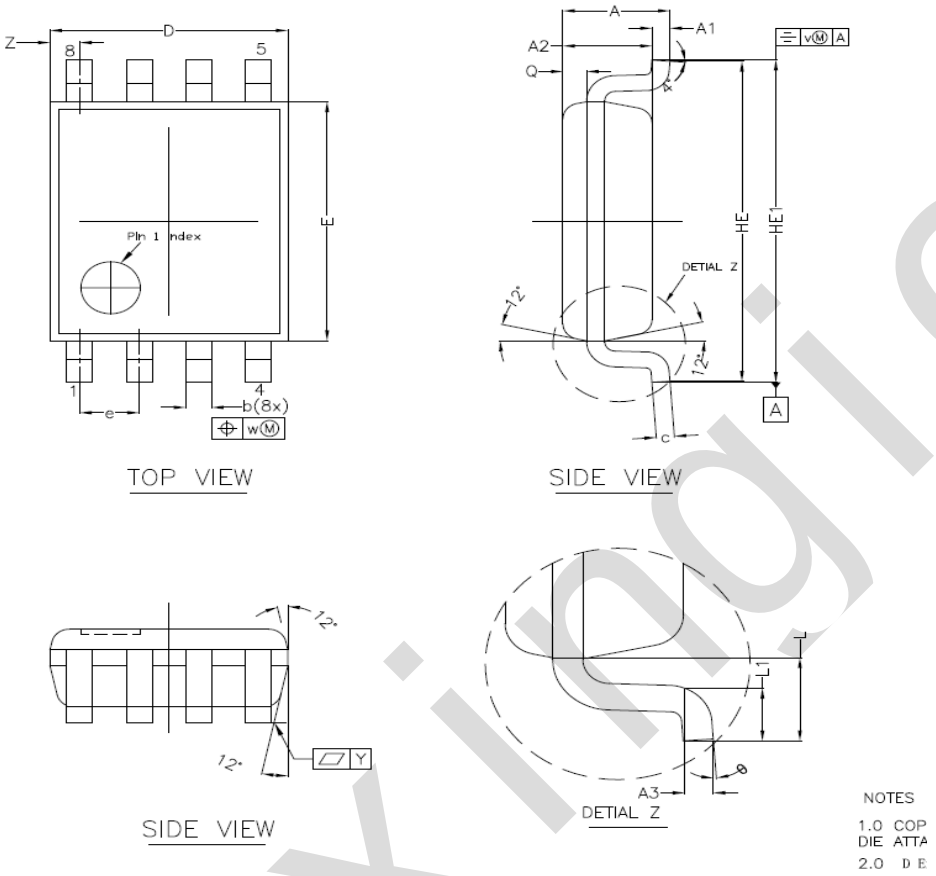
Symbol	Dimensions (mm)	
	Min.	Max.
A	0.90	1.10
A1	0.00	0.10
A2	0.90	1.00
b	0.15	0.35
c	0.11	0.175
D	2.00	2.20
E1	2.15	2.45
E	1.15	1.35
e	0.65	
e1	1.20	1.40
L	0.26	0.46
L1	0.525	
θ	0°	8°

6.3、TSSOP8



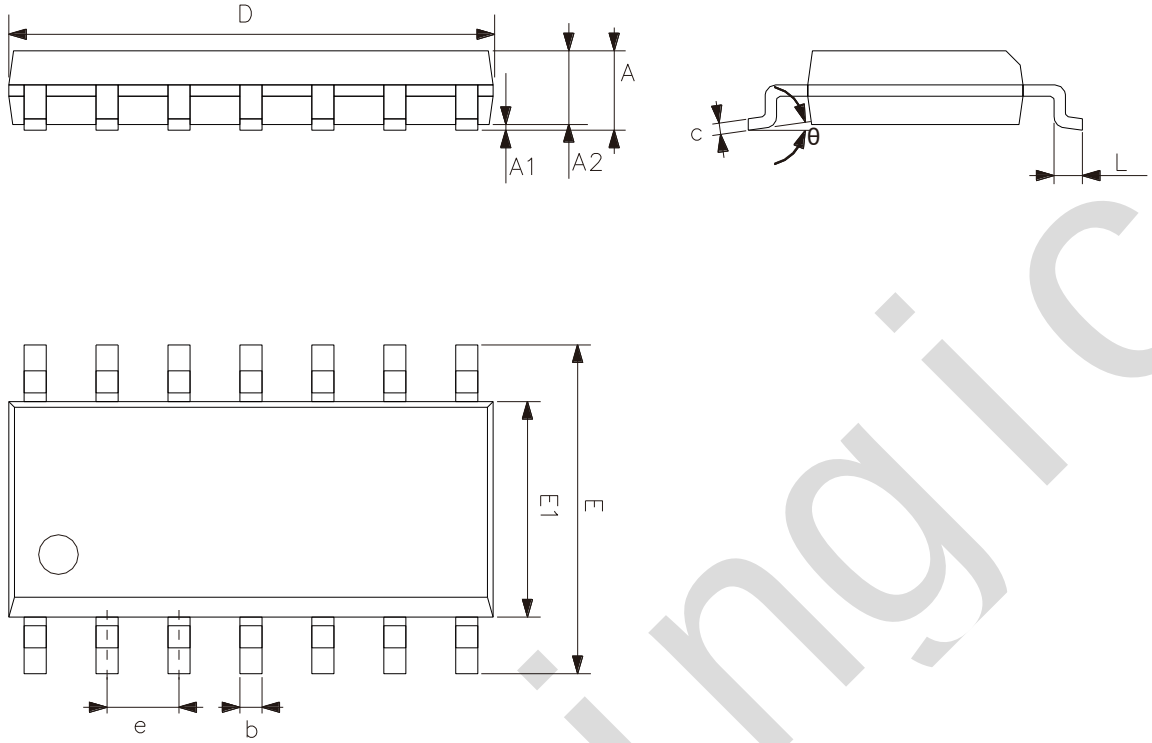
Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.10
A1	0	0.15
A2	0.75	0.95
A3	0.25	
bp	0.22	0.38
c	0.08	0.18
D	2.90	3.10
E	2.90	3.10
HE	3.90	4.10
L	0.50	
Lp	0.33	0.47
e	0.65	
Z	0.35	0.70
θ	0°	8°

6.4、VSSOP8



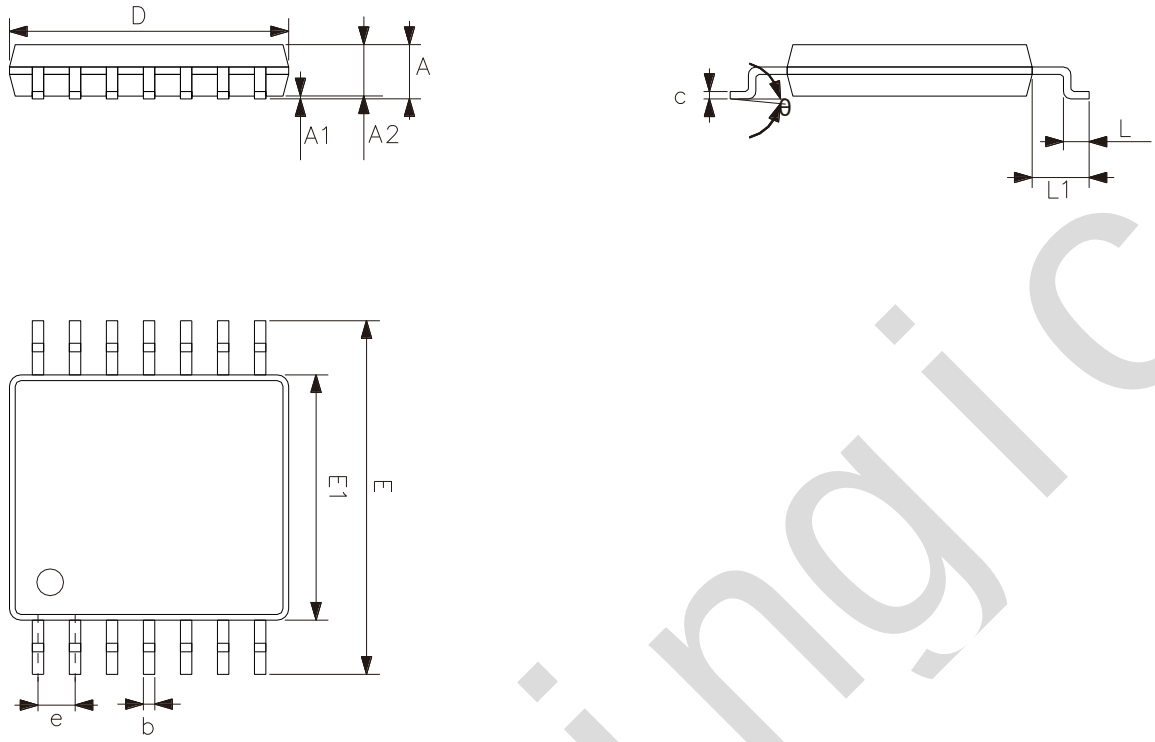
Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.00
A1	0.00	0.15
A2	0.60	0.85
A3	0.12	
Q	0.19	0.21
b	0.17	0.27
c	0.08	0.23
D	1.90	2.10
E	2.20	2.40
HE	3.00	3.20
HE1	3.00	3.40
e	0.50	
L	0.40	
L1	0.15	0.40
Y	0.10	
Z	0.10	0.40
θ	0 °	8 °

6.5、SOP14



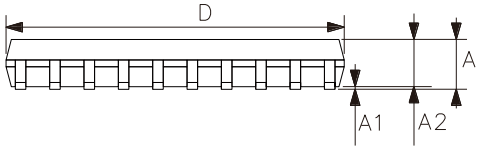
Symbol	Dimensions (mm)	
	Min.	Max.
A	1.50	1.75
A1	0.05	0.25
A2	1.30	-
b	0.33	0.50
c	0.19	0.25
D	8.43	8.76
E	5.80	6.25
E1	3.75	4.00
e	1.27	
L	0.40	0.89
θ	0 °	8 °

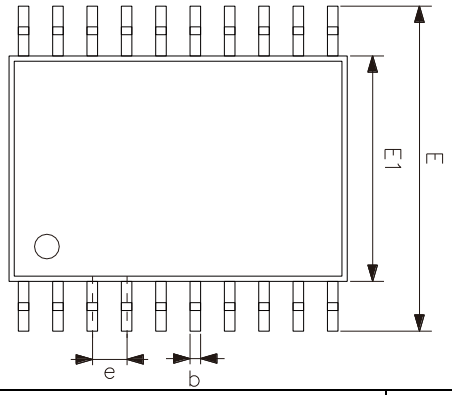
6.6、TSSOP14



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
L1	1.00	
θ	0°	8°

6.7、TSSOP20





Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
L1	1.00	
θ	0°	8°

7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notes

Recommended carefully reading this information before the use of this product；

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