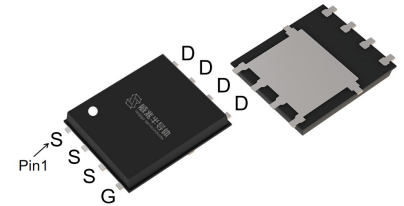


Features

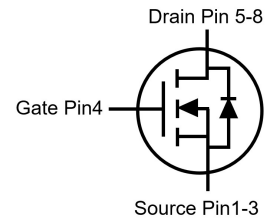
- Enhancement mode
- Very low on-resistance
- 100% Avalanche Tested, 100% Rg Tested

V_{DS}	40	V
$R_{DS(on),TYP@ V_{GS}=10V}$	4.8	mΩ
$R_{DS(on),TYP@ V_{GS}=4.5V}$	6.1	mΩ
I_D (Wire bond Limited)	33	A

PDFN5x6



Part ID	Package Type	Marking	Packing
VS4698AP	PDFN5x6	4698AP	3000pcs/Reel



Maximum ratings, at $T_A=25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		40	V
V_{GS}	Gate-Source voltage		± 20	V
I_S	Diode continuous forward current	$T_C = 25^\circ\text{C}$	29	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Wire bond limited)	$T_C = 25^\circ\text{C}$	33	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Wire bond limited)	$T_C = 100^\circ\text{C}$	33	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	228	A
I_{DSM}	Continuous drain current @ $V_{GS}=10V$	$T_A = 25^\circ\text{C}$	16	A
		$T_A = 70^\circ\text{C}$	13	A
E_{AS}	Avalanche energy, single pulsed ②		210	mJ
P_D	Maximum power dissipation ③	$T_C = 25^\circ\text{C}$	35	W
		$T_C = 100^\circ\text{C}$	14	W
P_{DSM}	Maximum power dissipation ④	$T_A = 25^\circ\text{C}$	2.6	W
		$T_A = 70^\circ\text{C}$	1.7	W
$T_{STG,TJ}$	Storage and Junction Temperature Range		-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ⑤	3	3.6	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ⑥	40	48	$^\circ\text{C/W}$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T _j = 25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	40	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current(T _j =25°C)	V _{DS} =40V,V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C)⑦	V _{DS} =40V,V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V,V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =250μA	1.1	1.6	2.2	V
R _{DS(on)}	Drain-Source On-State Resistance ⑧	V _{GS} =10V, I _D =20A	--	4.8	6.2	mΩ
		T _j =100°C ⑦	--	6.1	--	mΩ
R _{DS(on)}	Drain-Source On-State Resistance ⑧	V _{GS} =4.5V, I _D =15A	--	6.1	7.9	mΩ
Dynamic Electrical Characteristics @ T _j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance ⑦	V _{DS} =20V,V _{GS} =0V, f=1MHz	--	2860	--	pF
C _{oss}	Output Capacitance ⑦		--	245	--	pF
C _{rss}	Reverse Transfer Capacitance ⑦		--	195	--	pF
R _g	Gate Resistance	f=1MHz	--	0.8	--	Ω
Q _g (10V)	Total Gate Charge ⑦	V _{DS} =20V,I _D =20A, V _{GS} =10V	--	54	--	nC
Q _g (4.5V)	Total Gate Charge ⑦		--	27	--	nC
Q _{gs}	Gate-Source Charge ⑦		--	7.6	--	nC
Q _{gd}	Gate-Drain Charge ⑦		--	11	--	nC
Switching Characteristics ⑦						
T _d (on)	Turn-on Delay Time	V _{DD} =20V, I _D =20A, R _G =3Ω, V _{GS} =10V	--	9.2	--	ns
T _r	Turn-on Rise Time		--	45	--	ns
T _d (off)	Turn-Off Delay Time		--	38	--	ns
T _f	Turn-Off Fall Time		--	23	--	ns
Source- Drain Diode Characteristics@ T _j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =20A,V _{GS} =0V	--	0.8	1.2	V
T _{rr}	Reverse Recovery Time ⑦	I _{sd} =20A, V _{GS} =0V di/dt=100A/μs	--	14	28	ns
Q _{rr}	Reverse Recovery Charge ⑦		--	7	14	nC

NOTE:

- ① Single pulse; pulse width $\leq 100\mu s$.
- ② EAS of 210mJ is based on starting $T_j = 25^\circ\text{C}$, $L = 0.5\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 29A$, $V_{GS} = 10V$; 100% FT tested at $L = 0.5\text{mH}$, $I_{AS} = 16A$.
- ③ The power dissipation P_d is based on $T_j(\text{max})$, using junction-to-case thermal resistance $R_{\theta JC}$.
- ④ The power dissipation P_{dsm} is based on $T_j(\text{max})$, using junction-to-ambient thermal resistance $R_{\theta JA}$.
- ⑤ These tests are performed respectively with the device mounted on a 1 in2 pad and a minimum pad of 2oz. Copper FR-4 board in a still air environment with $T_A=25^\circ\text{C}$, using Transient Dual Interface method to acquire $R_{\theta JC}$.
- ⑥ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.
- ⑦ Guaranteed by design, not subject to production testing.
- ⑧ Pulse width $\leq 380\mu s$; duty cycle $\leq 2\%$.

Typical Characteristics

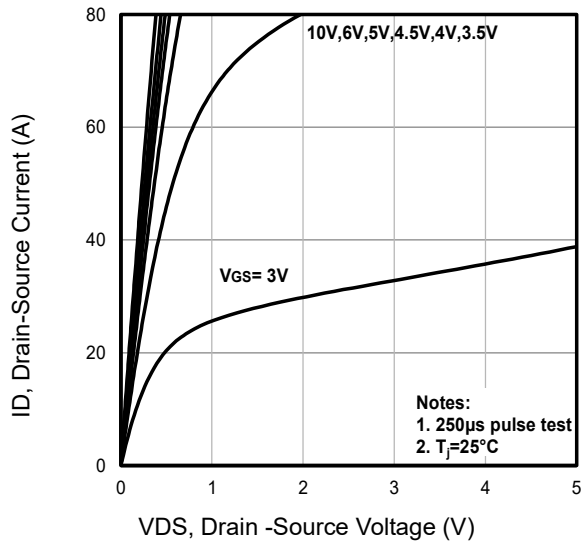


Fig1. Typical Output Characteristics

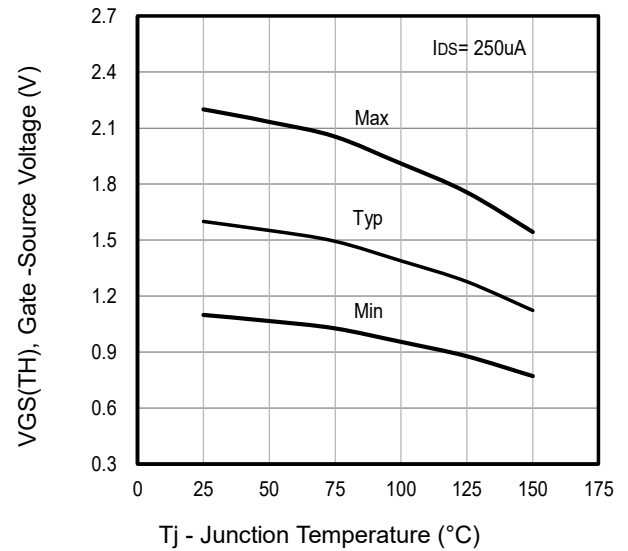


Fig2. Typical $V_{GS(TH)}$ Gate-Source Voltage Vs. T_J

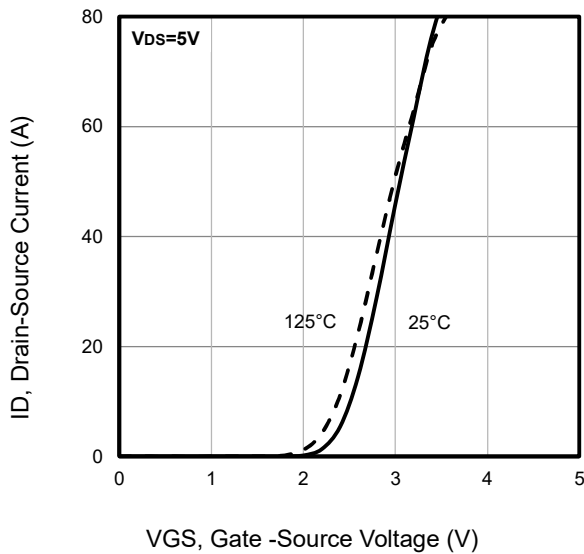


Fig3. Typical Transfer Characteristics

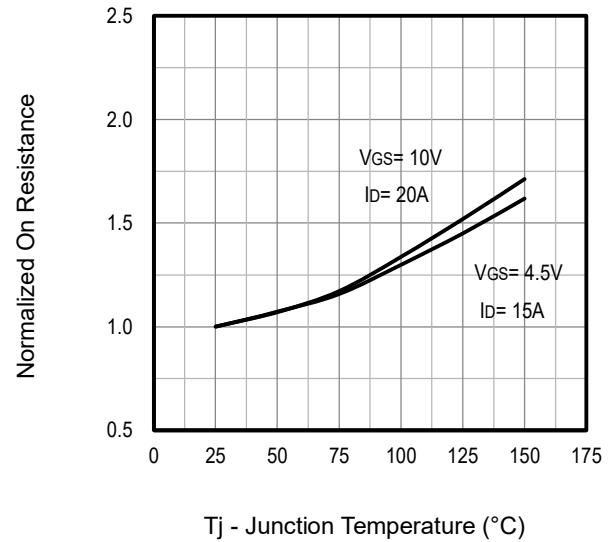


Fig4. Typical Normalized On-Resistance Vs. T_J

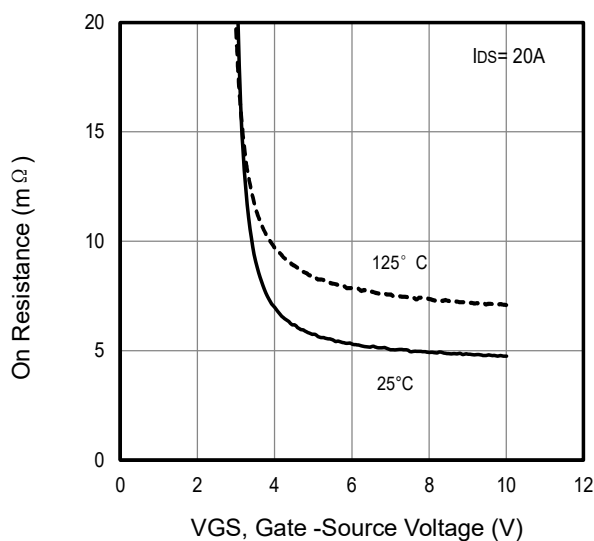


Fig5. Typical On Resistance Vs Gate-Source Voltage

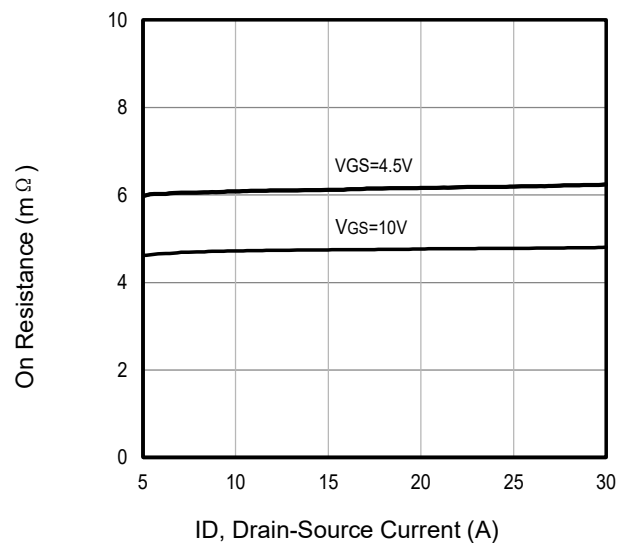


Fig6. Typical On Resistance Vs Drain Current

Typical Characteristics

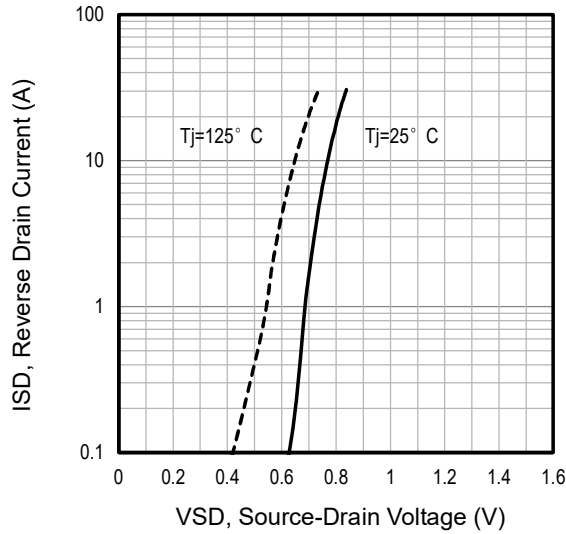


Fig7. Typical Source-Drain Diode Forward Voltage

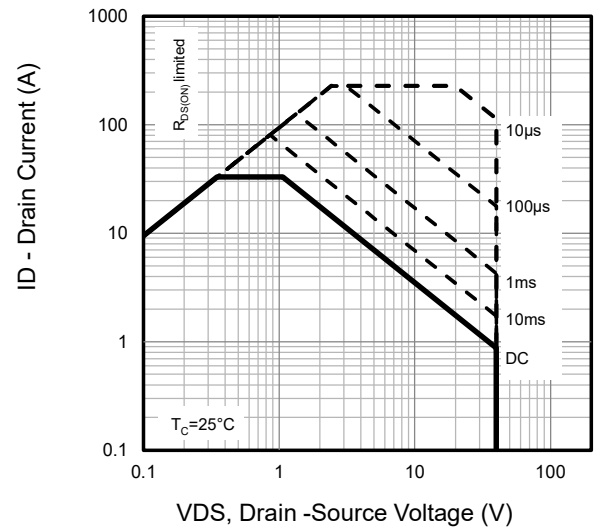


Fig8. Maximum Safe Operating Area

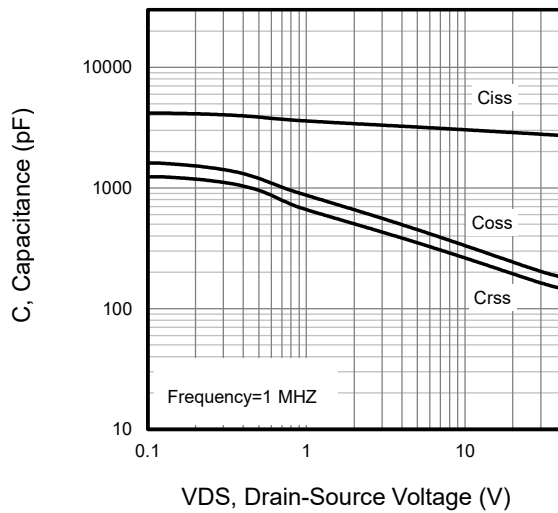


Fig9. Typical Capacitance Vs. Drain-Source Voltage

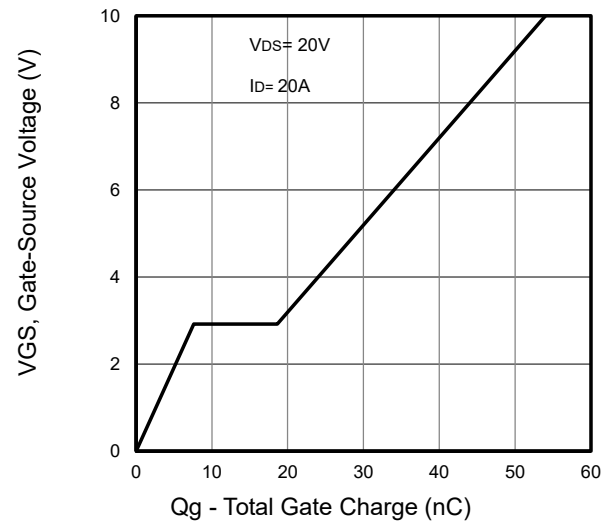


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

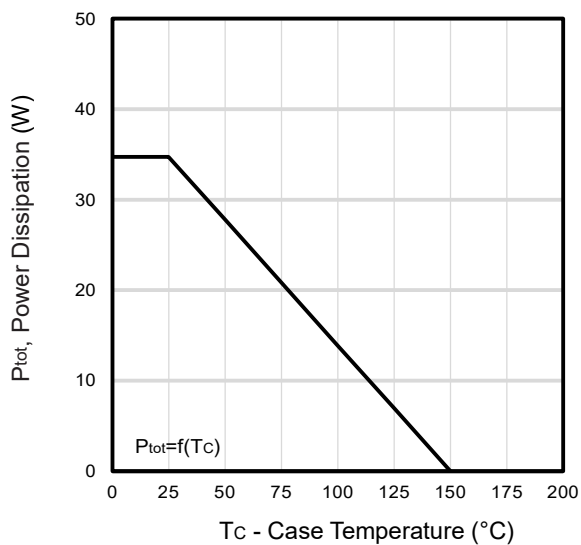


Fig11. Power Dissipation Vs. Case Temperature

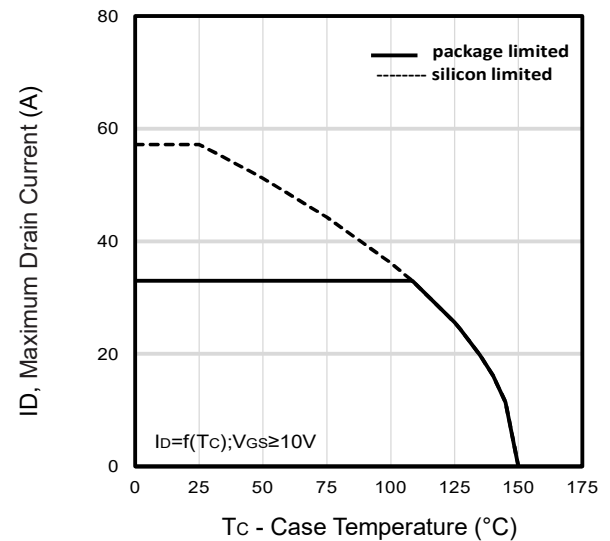


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

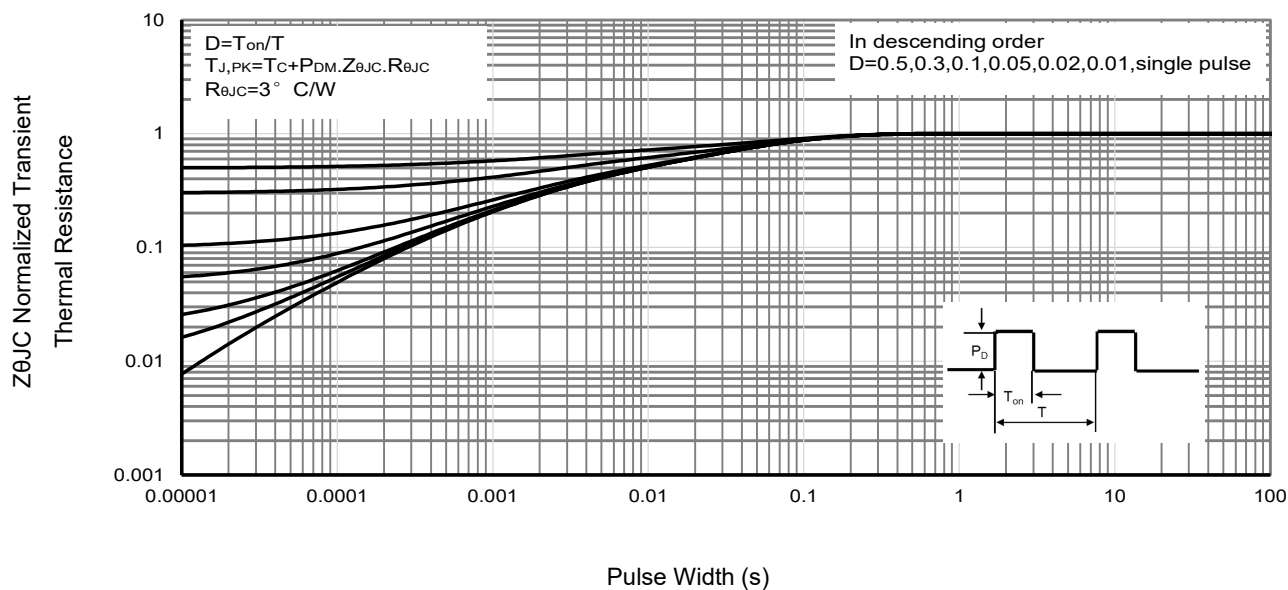


Fig13 . Normalized Maximum Transient Thermal Impedance

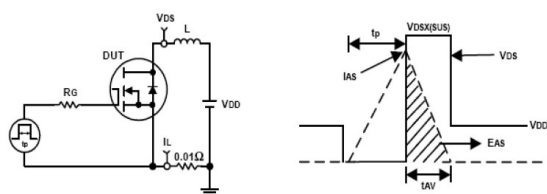


Fig14. Unclamped Inductive Test Circuit and waveforms

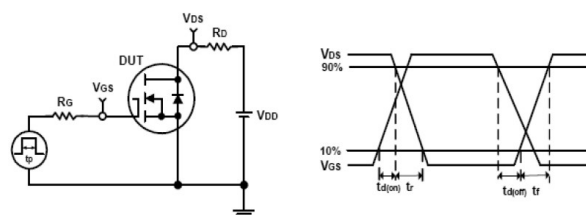
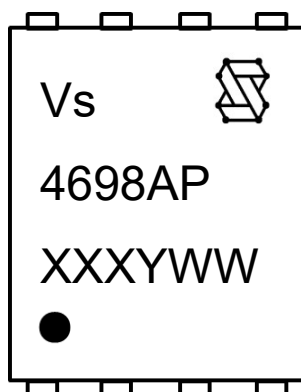


Fig15. Switching Time Test Circuit and waveforms

Marking Information



1st line: Vergiga Code (Vs) , Vergiga Logo

2nd line: Part Number (4698AP)

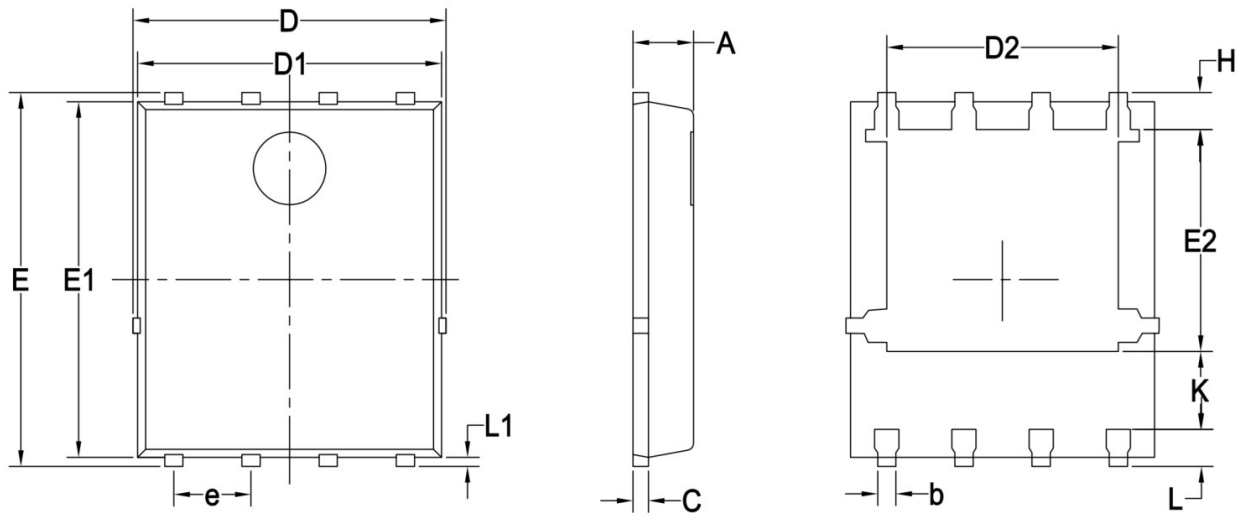
3rd line: Date code (XXXYWW)

XXX: Wafer Lot Number Code, code changed with Lot Number

Y: Year Code, refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

PDFN5x6 Package Outline Data


Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	0.90	1.00	1.10
b	0.30	0.40	0.50
C	0.20	0.25	0.30
D	5.15 BSC		
D1	5.00 BSC		
D2	3.76	3.81	3.86
e	1.27 BSC		
E	6.15 BSC		
E1	5.80	5.85	5.90
E2	3.45	3.65	3.85
H	0.51	0.61	0.71
K	1.10	--	--
L	0.51	0.61	0.71
L1	0.08	0.15	0.23

Notes:

- 1.Refer to JEDEC MO-240 variation AA.
- 2.Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
- 3.Dimensions "D1" and "E1" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

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