

## Automotive-grade N-channel 40 V, 2.5 mΩ typ., 80 A STripFET™ F7 Power MOSFET in a DPAK package

Datasheet - production data

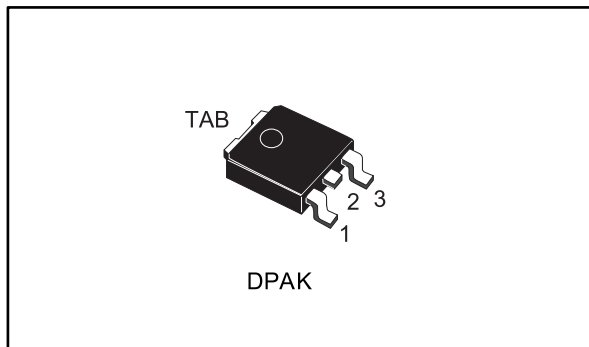
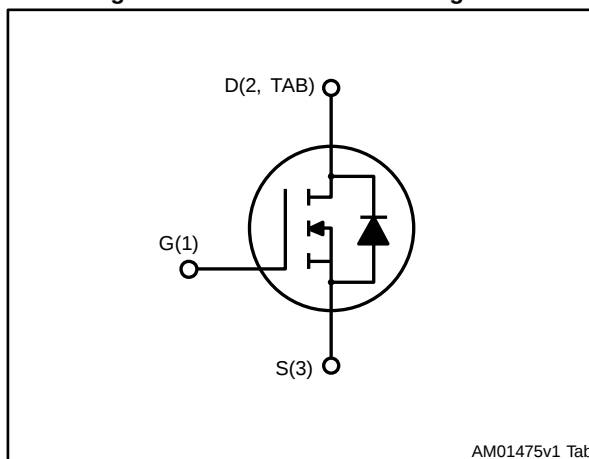


Figure 1: Internal schematic diagram



### Features

| Order code   | V <sub>DS</sub> | R <sub>DS(on)</sub> max. | I <sub>D</sub> | P <sub>TOT</sub> |
|--------------|-----------------|--------------------------|----------------|------------------|
| STD134N4F7AG | 40 V            | 3.5 mΩ                   | 80 A           | 134 W            |

- AEC-Q101 qualified
- Among the lowest R<sub>DS(on)</sub> on the market
- Excellent FoM (figure of merit)
- Low C<sub>rss</sub>/C<sub>iss</sub> ratio for EMI immunity
- High avalanche ruggedness



### Applications

- Switching applications

### Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

| Order code   | Marking | Package | Packing       |
|--------------|---------|---------|---------------|
| STD134N4F7AG | 134N4F7 | DPAK    | Tape and reel |

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## Contents

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol         | Parameter                                                              | Value      | Unit               |
|----------------|------------------------------------------------------------------------|------------|--------------------|
| $V_{DS}$       | Drain-source voltage                                                   | 40         | V                  |
| $V_{GS}$       | Gate-source voltage                                                    | $\pm 20$   | V                  |
| $I_D^{(1)}$    | Drain current (continuous) at $T_{case} = 25\text{ }^{\circ}\text{C}$  | 80         | A                  |
|                | Drain current (continuous) at $T_{case} = 100\text{ }^{\circ}\text{C}$ | 80         |                    |
| $I_{DM}^{(2)}$ | Drain current (pulsed)                                                 | 320        | A                  |
| $P_{TOT}$      | Total dissipation at $T_{case} = 25\text{ }^{\circ}\text{C}$           | 134        | W                  |
| $E_{AS}^{(3)}$ | Single pulse avalanche energy                                          | 325        | mJ                 |
| $T_{stg}$      | Storage temperature range                                              | -55 to 175 | $^{\circ}\text{C}$ |
| $T_J$          | Operating junction temperature range                                   |            |                    |

**Notes:**<sup>(1)</sup>Current is limited by package<sup>(2)</sup>Pulse width is limited by safe operating area<sup>(3)</sup>Starting  $T_J = 25\text{ }^{\circ}\text{C}$ ,  $I_D = 40\text{ A}$ ,  $V_{DD} = 20\text{ V}$ 

Table 3: Thermal data

| Symbol              | Parameter                        | Value | Unit                 |
|---------------------|----------------------------------|-------|----------------------|
| $R_{thj-case}$      | Thermal resistance junction-case | 1.12  | $^{\circ}\text{C/W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb  | 50    |                      |

**Notes:**<sup>(1)</sup>When mounted on a 1-inch<sup>2</sup> FR-4, 2 Oz copper board.

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified)

Table 4: Static

| Symbol                      | Parameter                         | Test conditions                                                                                                         | Min. | Typ. | Max.      | Unit          |
|-----------------------------|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------|------|------|-----------|---------------|
| $V_{(\text{BR})\text{DSS}}$ | Drain-source breakdown voltage    | $V_{\text{GS}} = 0\text{ V}$ , $I_{\text{D}} = 250\text{ }\mu\text{A}$                                                  | 40   |      |           | V             |
| $I_{\text{DSS}}$            | Zero gate voltage drain current   | $V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 40\text{ V}$                                                            |      |      | 1         | $\mu\text{A}$ |
|                             |                                   | $V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 40\text{ V}$ ,<br>$T_{\text{case}} = 125\text{ }^{\circ}\text{C}^{(1)}$ |      |      | 100       |               |
| $I_{\text{GSS}}$            | Gate-body leakage current         | $V_{\text{DS}} = 0\text{ V}$ , $V_{\text{GS}} = \pm 20\text{ V}$                                                        |      |      | $\pm 100$ | nA            |
| $V_{\text{GS(th)}}$         | Gate threshold voltage            | $V_{\text{DS}} = V_{\text{GS}}$ , $I_{\text{D}} = 250\text{ }\mu\text{A}$                                               | 2    |      | 4         | V             |
| $R_{\text{DS(on)}}$         | Static drain-source on-resistance | $V_{\text{GS}} = 10\text{ V}$ , $I_{\text{D}} = 40\text{ A}$                                                            |      | 2.5  | 3.5       | m $\Omega$    |

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

Table 5: Dynamic

| Symbol           | Parameter                    | Test conditions                                                                                                                                                              | Min. | Typ. | Max. | Unit |
|------------------|------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $C_{\text{iss}}$ | Input capacitance            | $V_{\text{DS}} = 25\text{ V}$ , $f = 1\text{ MHz}$ ,<br>$V_{\text{GS}} = 0\text{ V}$                                                                                         | -    | 2790 | -    | pF   |
| $C_{\text{oss}}$ | Output capacitance           |                                                                                                                                                                              | -    | 890  | -    |      |
| $C_{\text{rss}}$ | Reverse transfer capacitance |                                                                                                                                                                              | -    | 60   | -    |      |
| $Q_{\text{g}}$   | Total gate charge            | $V_{\text{DD}} = 20\text{ V}$ , $I_{\text{D}} = 80\text{ A}$ ,<br>$V_{\text{GS}} = 10\text{ V}$<br>(see <a href="#">Figure 14: "Test circuit for gate charge behavior"</a> ) | -    | 41   | -    | nC   |
| $Q_{\text{gs}}$  | Gate-source charge           |                                                                                                                                                                              | -    | 15   | -    |      |
| $Q_{\text{gd}}$  | Gate-drain charge            |                                                                                                                                                                              | -    | 11   | -    |      |

Table 6: Switching times

| Symbol              | Parameter           | Test conditions                                                                                                                                                                                                                                                                      | Min. | Typ. | Max. | Unit |
|---------------------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{\text{d(on)}}$  | Turn-on delay time  | $V_{\text{DD}} = 20\text{ V}$ , $I_{\text{D}} = 40\text{ A}$ ,<br>$R_{\text{G}} = 4.7\text{ }\Omega$ , $V_{\text{GS}} = 10\text{ V}$<br>(see <a href="#">Figure 13: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 18: "Switching time waveform"</a> ) | -    | 18   | -    | ns   |
| $t_{\text{r}}$      | Rise time           |                                                                                                                                                                                                                                                                                      | -    | 17.5 | -    |      |
| $t_{\text{d(off)}}$ | Turn-off delay time |                                                                                                                                                                                                                                                                                      | -    | 26   | -    |      |
| $t_{\text{f}}$      | Fall time           |                                                                                                                                                                                                                                                                                      | -    | 13   | -    |      |

Table 7: Source-drain diode

| Symbol          | Parameter                     | Test conditions                                                                                                                                                                                   | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $I_{SD}^{(1)}$  | Source-drain current          |                                                                                                                                                                                                   | -    |      | 80   | A    |
| $I_{SDM}^{(2)}$ | Source-drain current (pulsed) |                                                                                                                                                                                                   | -    |      | 320  | A    |
| $V_{SD}^{(2)}$  | Forward on voltage            | $V_{GS} = 0\text{ V}$ , $I_{SD} = 80\text{ A}$                                                                                                                                                    | -    |      | 1.2  | V    |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 80\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 32\text{ V}$<br>(see <a href="#">Figure 15: "Test circuit for inductive load switching and diode recovery times"</a> ) | -    | 37   |      | ns   |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                   | -    | 28.5 |      | nC   |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                   | -    | 1.5  |      | A    |

**Notes:**<sup>(1)</sup>Current is limited by package<sup>(2)</sup>Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

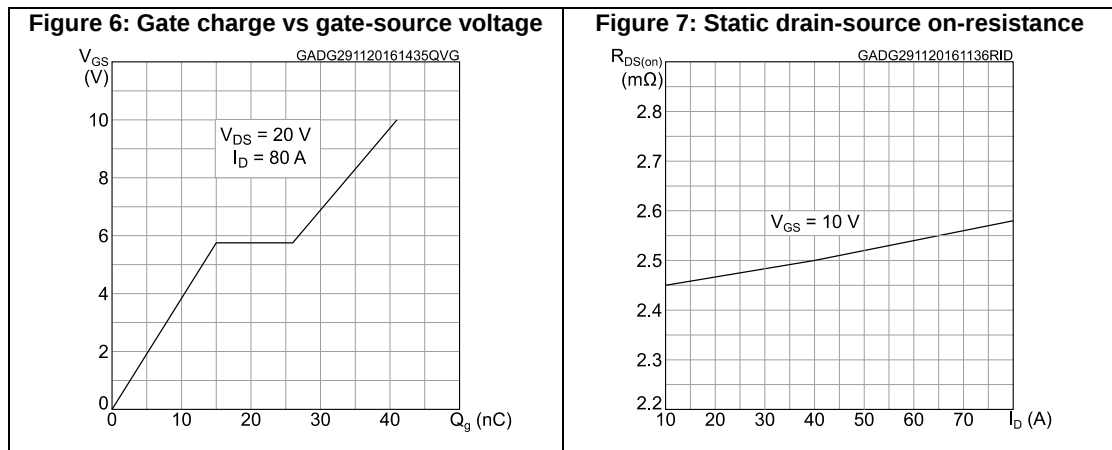
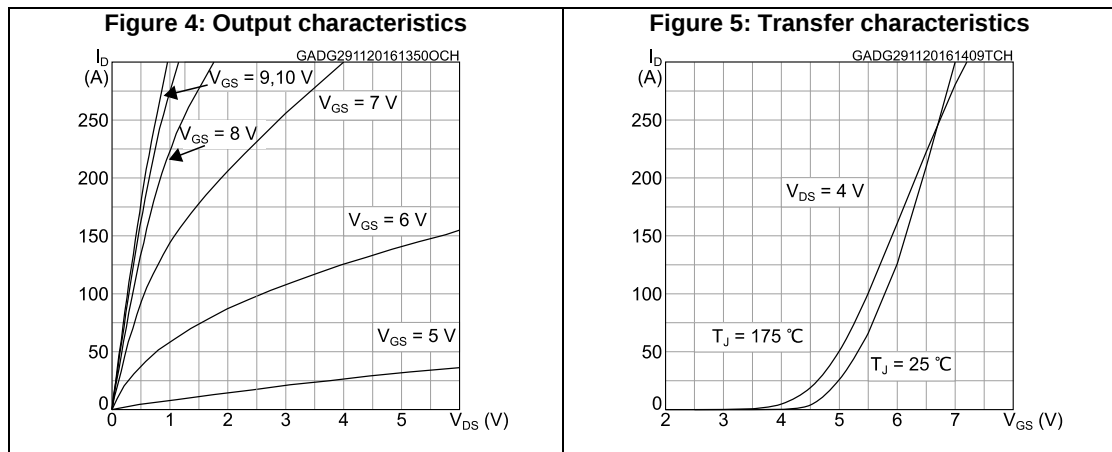
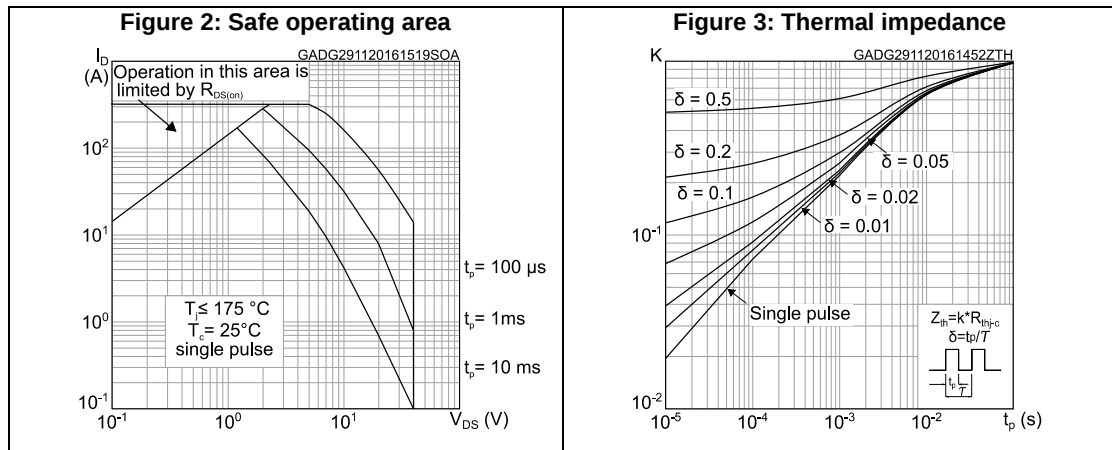


Figure 8: Capacitance variations

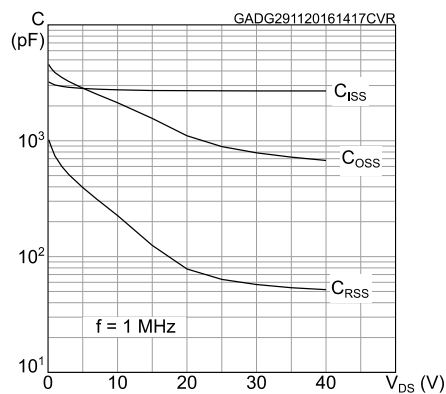


Figure 9: Normalized gate threshold voltage vs temperature



Figure 10: Normalized on-resistance vs temperature

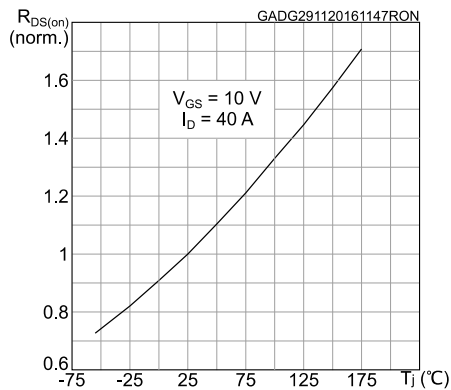
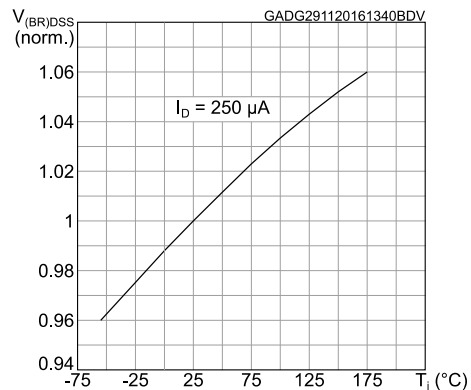
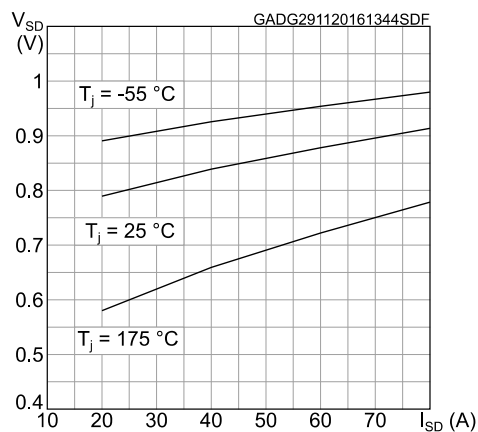
Figure 11: Normalized  $V_{(BR)DSS}$  vs temperature

Figure 12: Source-drain diode forward characteristics



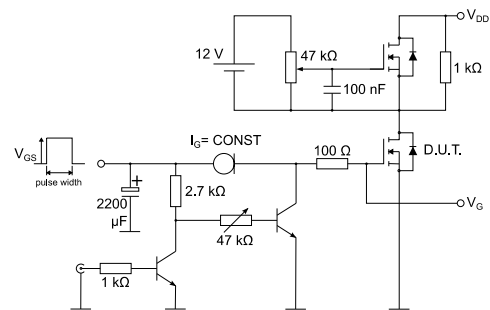
### 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**



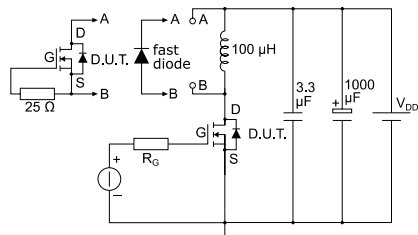
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**Figure 14: Test circuit for gate charge behavior**



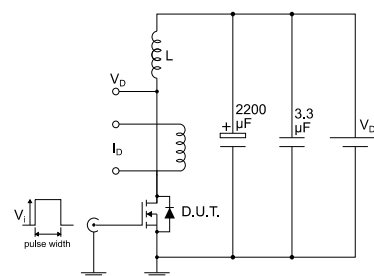
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**Figure 15: Test circuit for inductive load switching and diode recovery times**



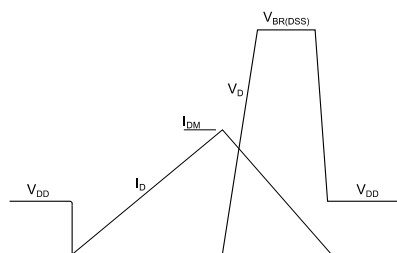
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**Figure 16: Unclamped inductive load test circuit**



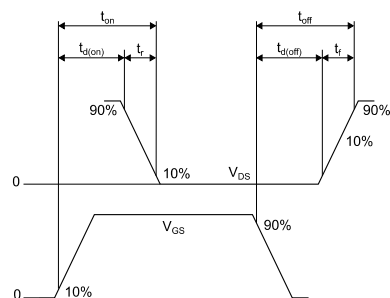
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**Figure 17: Unclamped inductive waveform**



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**Figure 18: Switching time waveform**



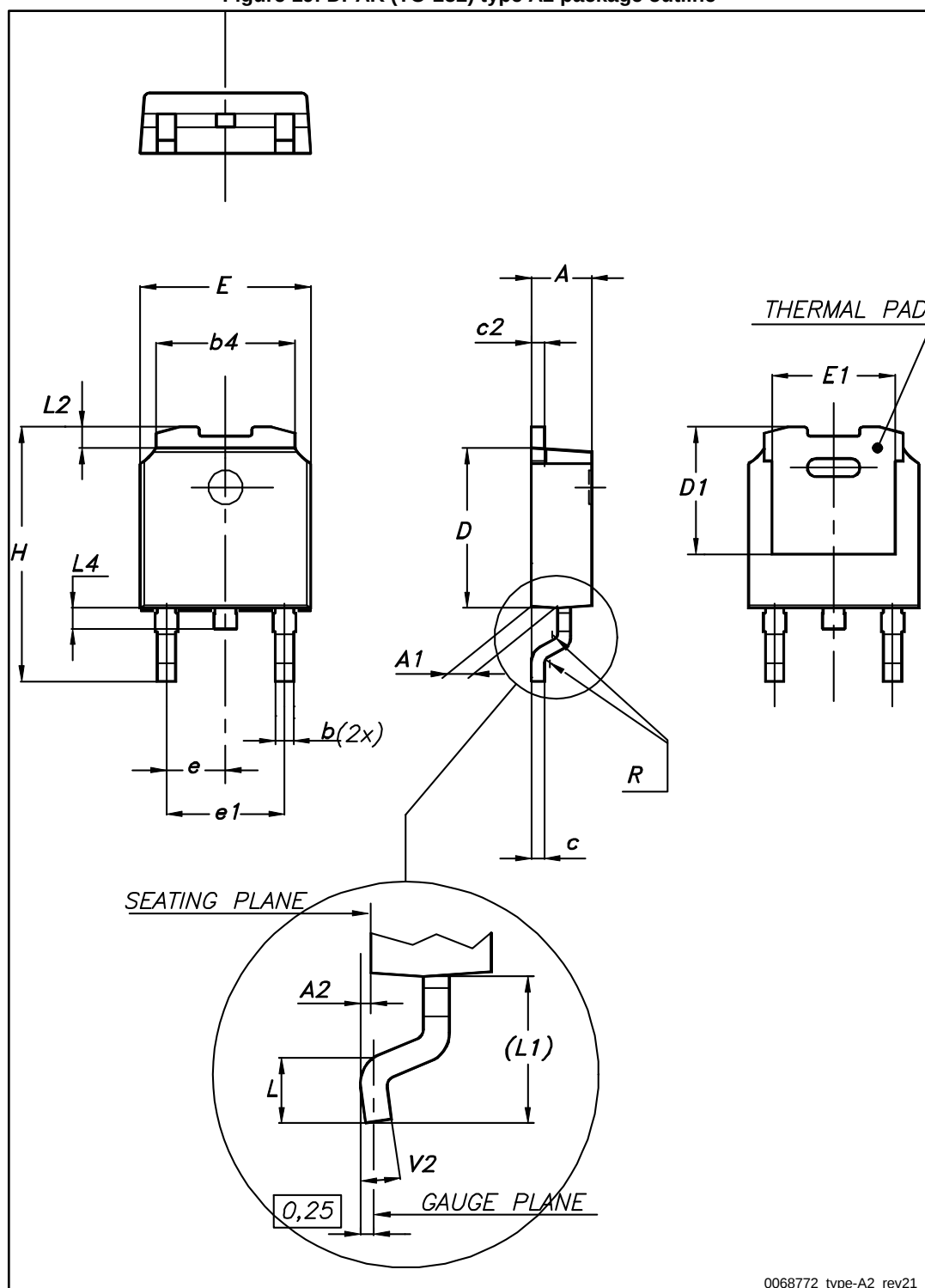
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## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **[www.st.com](http://www.st.com)**. ECOPACK® is an ST trademark.

## 4.1 DPAK (TO-252) type A2 package information

Figure 19: DPAK (TO-252) type A2 package outline

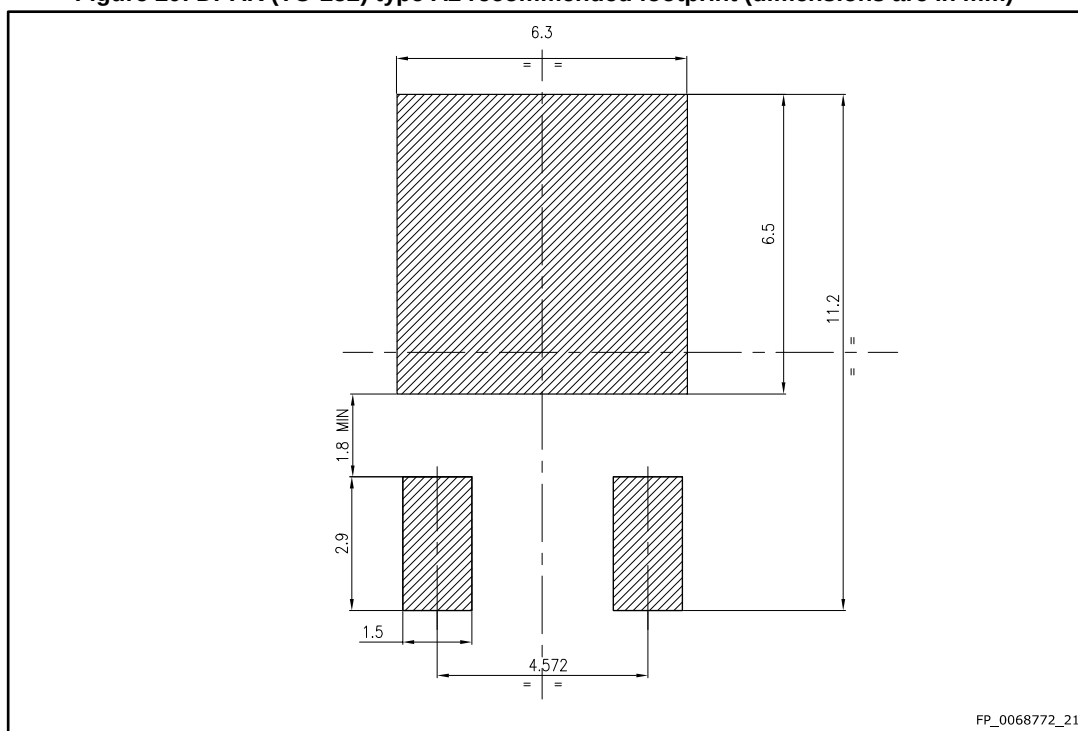


0068772\_type-A2\_rev21

Table 8: DPAK (TO-252) type A2 mechanical data

| Dim. | mm   |      |       |
|------|------|------|-------|
|      | Min. | Typ. | Max.  |
| A    | 2.20 |      | 2.40  |
| A1   | 0.90 |      | 1.10  |
| A2   | 0.03 |      | 0.23  |
| b    | 0.64 |      | 0.90  |
| b4   | 5.20 |      | 5.40  |
| c    | 0.45 |      | 0.60  |
| c2   | 0.48 |      | 0.60  |
| D    | 6.00 |      | 6.20  |
| D1   | 4.95 | 5.10 | 5.25  |
| E    | 6.40 |      | 6.60  |
| E1   | 5.10 | 5.20 | 5.30  |
| e    | 2.16 | 2.28 | 2.40  |
| e1   | 4.40 |      | 4.60  |
| H    | 9.35 |      | 10.10 |
| L    | 1.00 |      | 1.50  |
| L1   | 2.60 | 2.80 | 3.00  |
| L2   | 0.65 | 0.80 | 0.95  |
| L4   | 0.60 |      | 1.00  |
| R    |      | 0.20 |       |
| V2   | 0°   |      | 8°    |

**Figure 20: DPAK (TO-252) type A2 recommended footprint (dimensions are in mm)**



## 4.2 DPAK (TO-252) packing information

Figure 21: DPAK (TO-252) tape outline

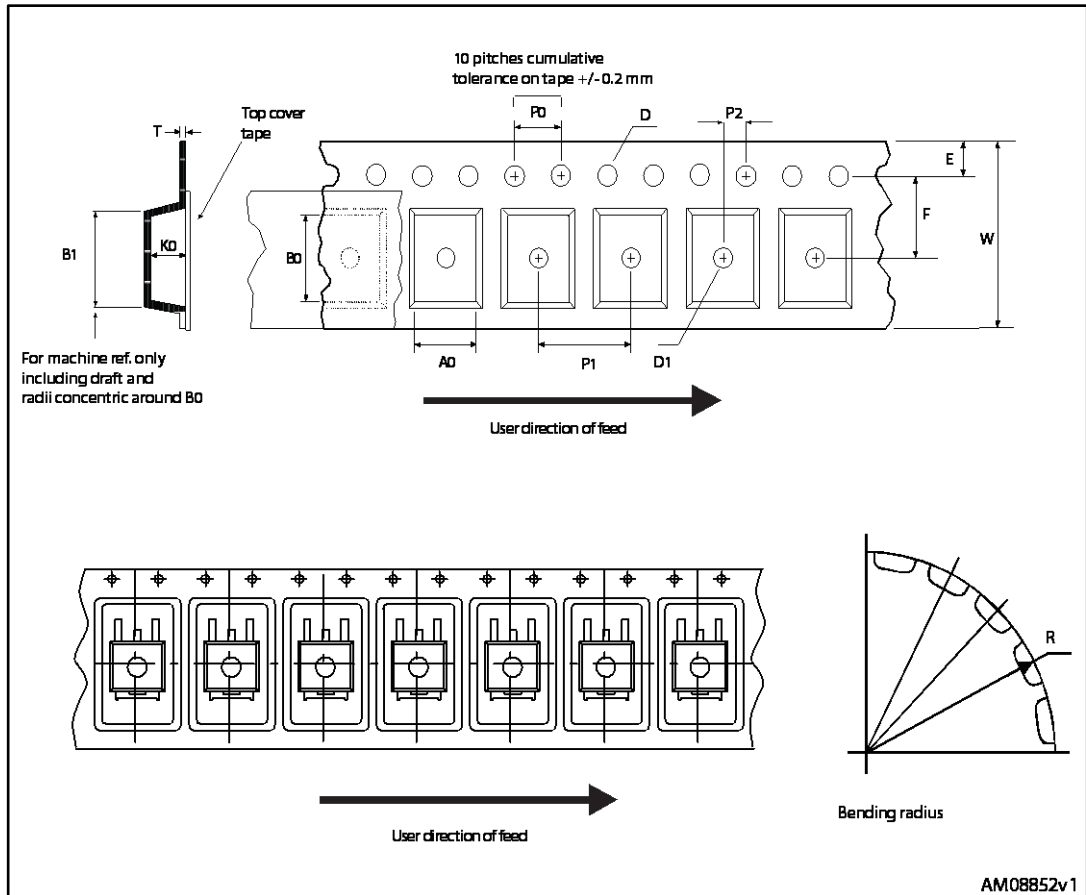


Figure 22: DPAK (TO-252) reel outline

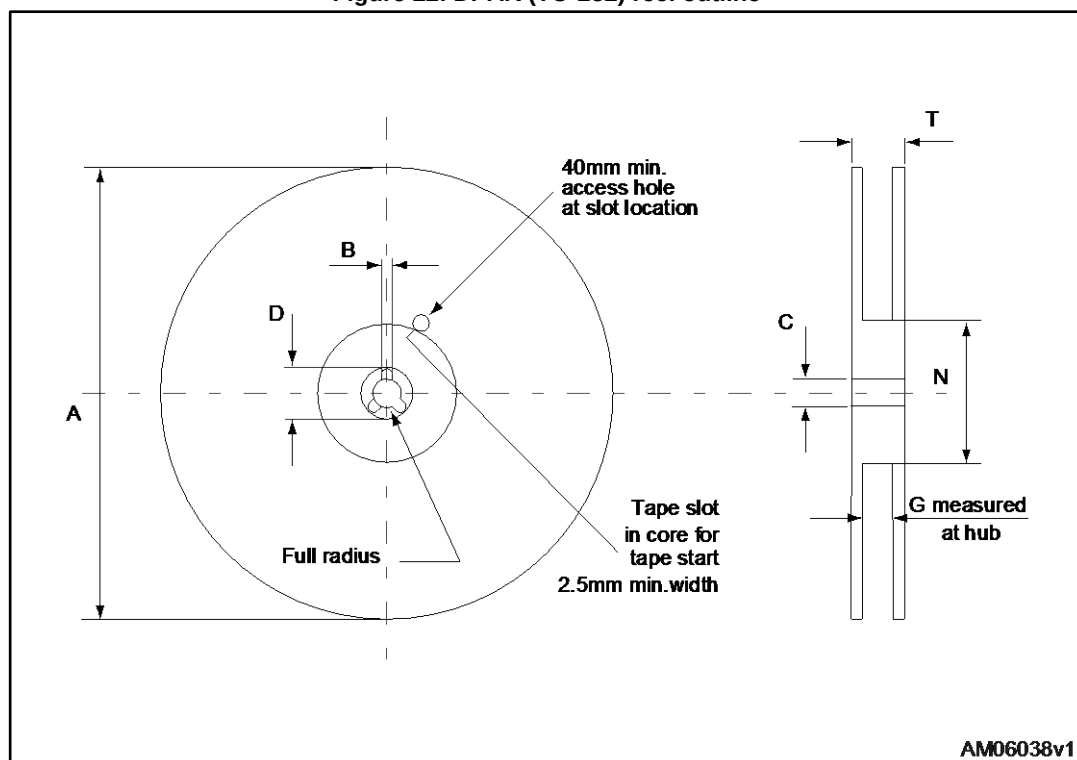


Table 9: DPAK (TO-252) tape and reel mechanical data

| Tape |      |      | Reel      |      |      |
|------|------|------|-----------|------|------|
| Dim. | mm   |      | Dim.      | mm   |      |
|      | Min. | Max. |           | Min. | Max. |
| A0   | 6.8  | 7    | A         |      | 330  |
| B0   | 10.4 | 10.6 | B         | 1.5  |      |
| B1   |      | 12.1 | C         | 12.8 | 13.2 |
| D    | 1.5  | 1.6  | D         | 20.2 |      |
| D1   | 1.5  |      | G         | 16.4 | 18.4 |
| E    | 1.65 | 1.85 | N         | 50   |      |
| F    | 7.4  | 7.6  | T         |      | 22.4 |
| K0   | 2.55 | 2.75 |           |      |      |
| P0   | 3.9  | 4.1  | Base qty. |      | 2500 |
| P1   | 7.9  | 8.1  | Bulk qty. |      | 2500 |
| P2   | 1.9  | 2.1  |           |      |      |
| R    | 40   |      |           |      |      |
| T    | 0.25 | 0.35 |           |      |      |
| W    | 15.7 | 16.3 |           |      |      |

## 5 Revision history

Table 10: Document revision history

| Date        | Revision | Changes       |
|-------------|----------|---------------|
| 05-Dec-2016 | 1        | First release |

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