MDC97476

1MSPS, 12-BIT ADC
SOT-23-6 标准封装

概述

MDC97476 是 MPS 公司新上市的一款工业级 12-bit ADC，与业界同等功能的 12-bit ADC 管脚兼容，具有 1MSPS 采样率，电源功耗低，外形尺寸紧凑，适合于在工业自动化控制过程中，对多通道分布式模拟输入信号实现高达 1MHz 的同步数据采样，实现自动控制系统的闭环控制，如工业级大功率伺服电机的自动控制，对无人值守铁塔/机房的运行参数实现 7x24 小时连续采样与环境参数的控制.

MDC97476 采用单一电源供电，电源电压 3.0-3.6V。为简化外围电路，ADC 内部参考电源与 VDD 共用同一电源。数字接口使用简化 3 线 SPI 串行接口总线协议与外部控制器如 MCU/FPGA 主板联接。
工作温度范围：-40°C 至 +85°C。

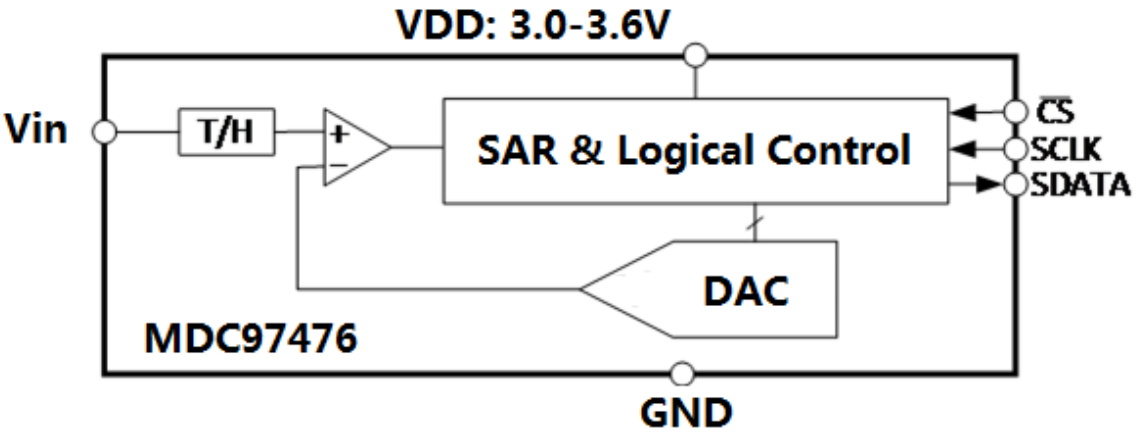
产品特点

- 单通道 12-bit ADC
- 最高采样率 1MSPS
- 典型 SNR=71dB, THD=82dB
- 典型 DNL/INL: +/-0.5 LSB
- 3.0-3.6V 单电源供电
- 兼容 3 线 SPI 标准接口
- SOT-23-6 标准封装

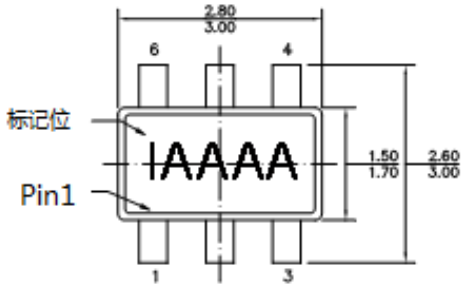
应用场景

- 工业自动化仪表及控制系统
- 数字化采样系统
- 医疗仪器
- 移动通信终端
- 便携式仪表
- 电池供电设备中的信号采集

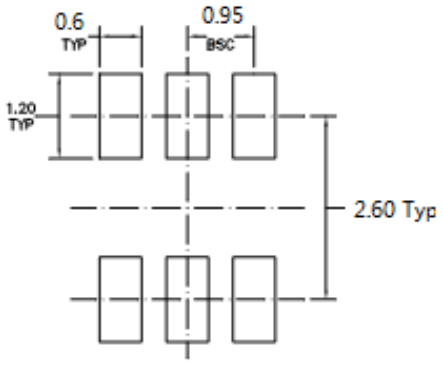
功能框图



外形封装尺寸图



俯视图



推荐焊盘图　　单位:毫米

管脚功能表

脚位号	名称	I/O	功能描述
1	VDD	电源	电源及 ADC 参考电压，电压范围：3.0 V 至 3.6 V
2	GND	参考地	参考地，电源地
3	VIN	模拟输入	模拟输入信号，范围：0 至 VDD
4	SCLK	数字输入	SPI 时钟输入
5	SDATA	数字输出	转换数字化数据输出，数据编码格式请参考 MPS 官网数据手册
6	$\overline{CS}$	数字输入	片选控制信号. $\overline{CS}$ 的下降沿开始 ADC 转换过程

推荐工作参数

供电电压 (VDD) ..... 3.0V to 3.6V
模拟输入信号 (VIN)..... 0V to VDD
数字输入(SCLK, SDATA, $\overline{CS}$)..... 0V to VDD
工作温度 (TA) ..... -40°C to +85°C

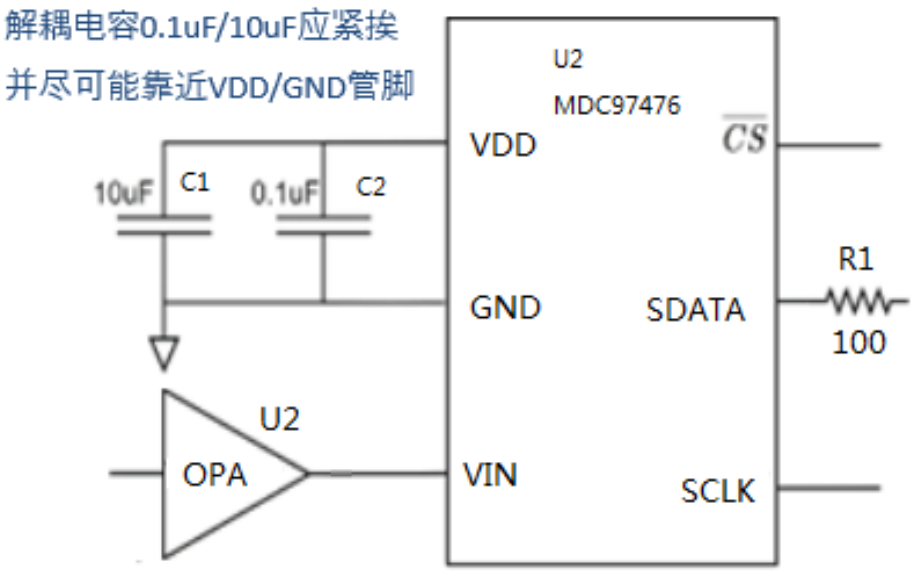
注: 如果 VDD 电压超过 4.0V 可能会造成器件永久性功能失效.

选型订购指南

型号	包装方式	温度范围	电源电压
MDC97476GJ-P	剪带袋装	-40°C to +85°C	3.0V 至 3.6V
MDC97476GJ-Z	178mm 整盘	-40°C to +85°C	3.0V 至 3.6V

典型应用图

MDC97476 的典型应用图如下，为了减少电源纹波 VDD 对 ADC 转换精度的影响，需要在 PCB 上靠近 ADC 的 VDD 与 GND 的两个 Pin 脚上，加上两个去耦电容 C1, C2. 如果串行数据输出脚 SDATA 离上位控制器(MCU 或 FPGA)的输入脚距离大于 5 厘米，建议在 SDATA 输出脚上串联一个 50-200 的电阻，以减少该输出信号的变形失真。如果输入到 VIN 模拟信号范围不在 0-3.6V 的范围内，推荐在 VIN 输入端加入一级运放构成的模拟信号缓冲器 U2，来匹配调整模拟输入信号范围.



技术支持

如果使用中有任何疑问，请以如下方式联络我们:

电子邮件..... Forest.Jie@monolithicpower.com
微信号 .....Forest-ADC
手机号码.....13240142807
MDC97476 最新数据手册网址.....
https://www.monolithicpower.com/en/products/mdc97476.html

亦可参考后附英文手册，了解该ADC详细技术参数.

MDC97476

1 MSPS, 12-Bit ADC in 6-Lead TSOT-23

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MDC97476 is 12-bit, high speed, low power, successive approximation analog-to-digital converters (ADCs). The parts operate from a single 3 V to 3.6 V power supply with a conversion rate up to 1 MSPS.

The MDC97476 uses a three–wire SPI compatible serial digital interface for chip control and data output. The sampling rate is determined by the serial clock, and the conversion process and data acquisition are controlled by a chip select pin.

The MDC97476 uses the power supply as its reference, and power consumption is as low as 4.9mW at 1 MSPS conversion rate with a 3.3 V power supply. The parts are available in a 6-pin TSOT-23 package, with an operating temperature range of –40°C to +85°C.

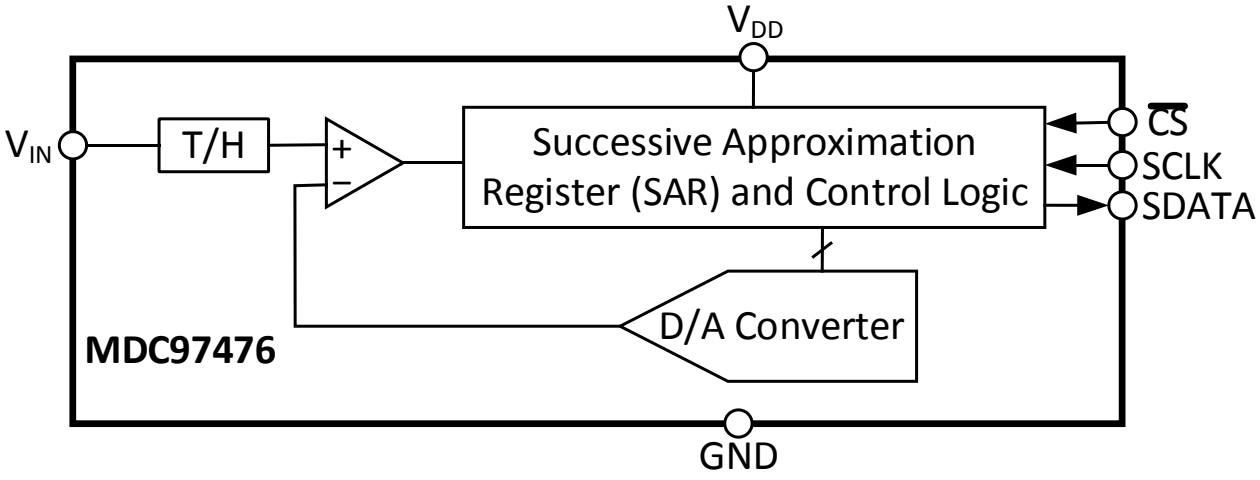
FEATURES

- 12-Bit SAR analog-to-digital converter
- Conversion rate up to 1 MSPS
- Single 3.0 V to 3.6 V Power Supply
- Low power: 4.9 mW at 1 MSPS with 3.3 V supplies
- 71 dB SNR at 117 kHz input frequency
- Reference derived from power supply
- SPI-compatible serial interface
- 6-pin TSOT-23 package

APPLICATIONS

- Battery-powered systems
- Medical instruments
- Instrumentation and control systems
- Portable Systems
- Data acquisition systems
- Mobile Communications

BLOCK DIAGRAM

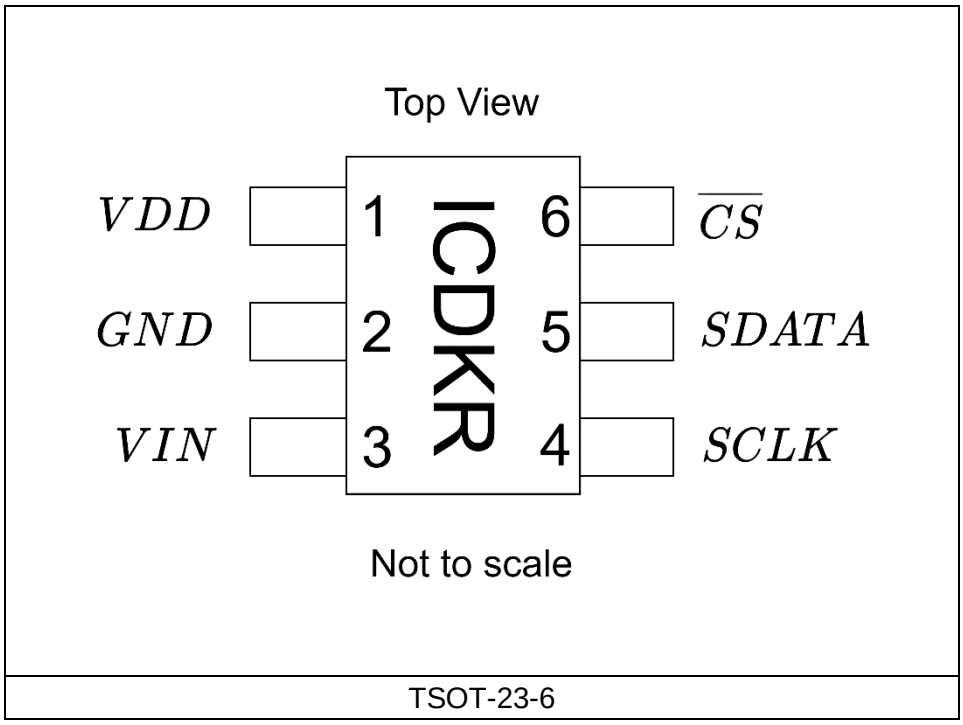


ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MDC97476GJ	TSOT-23-6	*CDKR*	1

* For Tape & Reel, add suffix -Z (e.g. MDC97476GJ-Z)

PACKAGE REFERENCE



TSOT-23-6

PIN FUNCTIONS

Pin #	Name	I/O	Description
1	VDD	power	Positive power supply pin. Voltage range 3 V to 3.6 V
2	GND	ground	Ground pin
3	VIN	input	Analog input pin and the range is from 0 to VDD.
4	SCLK	input	Digital clock input.
5	SDATA	output	Digital data output. The bit serial stream is clocked out at falling edge of SCLK.
6	$\overline{CS}$	input	Chip selection. The falling edge of $\overline{CS}$ starts the conversion.

Absolute Maximum Ratings (1)

VDD to GND .....-0.3 V to +4 V
VIN to GND.....-0.3 V to VDD+0.3 V
SCLK to GND .....-0.3 V to VDD+0.3 V
$\overline{CS}$ to GND .....-0.3 V to VDD+0.3 V
SDATA to GND .....-0.3 V to VDD+0.3 V
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....3.5k V
Charged device model (CDM) ..... 250 V

Recommended Operating Conditions(2)

VDD .....+3 V to +3.6 V
Digital input pins ..... 0V to VDD V
Operating Junction Temp. (T_A)... -40°C to +85°C

Thermal Resistance (3) θ_{JA} θ_{JC}

6-pin TSOT-23 ..... 143 ..... 76 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS - MDC97476

VDD = 3.3 V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Dynamic Characteristics						
Signal to Noise Ratio	SNR	f_{IN} = 117 kHz		71		dB
Signal to (Noise & Distortion) Ratio	SINAD	f_{IN} = 117 kHz		71		dB
Total Harmonic Distortion	THD	f_{IN} = 117 kHz		-82		dB
Spurious Free Dynamic Range	SFDR	f_{IN} = 117 kHz		85		dB
Static Characteristics						
Integral Nonlinearity	INL			±0.5		LSB
Differential Nonlinearity	DNL			±0.5		LSB
Gain Error	GE			70		LSB
Offset error	V_{OFF}			6		LSB
Analog Input						
Input voltage range	V_{IN}			0 to VDD		V
DC leakage current	I_L				1	uA
Input capacitance	C_{IN_A}			14		pF
Digital Input						
Input high voltage	V_{INH}			2		V
Input Low Voltage	V_{INL}			1		V
Input current	I_{IN}				1	uA
Input capacitance	C_{IN_D}			2		pF
Digital Output						
Output high voltage	V_{OH}	I_{load} = 1mA		3.2		V
Output Low Voltage	V_{OL}	I_{load} = 1mA		0.1		V
Floating output capacitance	C_{OUT}			2		pF
Floating output current	I_{OL}				10	uA
POWER SUPPLY CHARACTERISTICS						
Power supply voltage	V_{DD}			3.3		V
Static normal mode current	I_{DDS}			0.9		mA
Operation normal mode current	I_{DDOP}			1.5		mA
Sleep mode current	I_{SD}	SCLK off		25		uA
	I_{SD}	SCLK on		200		uA
Operational normal mode power consumption	P_{OP}			4.9		mW
Sleep power consumption	P_{SD}	SCLK off		83		uW
		SCLK on		660		uW
AC ELECTRICAL CHARACTERISTICS						
Clock frequency	F_{SCLK}				20	MHz
SCLK duty cycle			40%		60%	

Throughput rate	F_{SAMPLE}				1	MHz

TIMING CHARACTERISTICS

VDD = 3.3 V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
SCLK period	t_{SCLK}		50			ns
Conversion time	t_{on}			16 × t_{SCLK}		
Quiet time	t_{quiet}		50			ns
Minimum $\overline{CS}$ pulse width	t_1		10			ns
$\overline{CS}$ to SCLK setup time	t_2		10			ns
Delay from CS until SDATA TRI-STATE disabled	t_3				20	ns
Data access time after SCLK falling edge	t_4				40	ns
SCLK low pulse width	t_5		0.4 × t_{SCLK}			ns
SCLK high pulse width	t_6		0.4 × t_{SCLK}			ns
SCLK to data valid hold time	t_7		5			ns
SCLK falling edge to SDATA tri-state	t_8		5			ns
wake-up time from sleep mode	t_{wakeup}			50		µs
power up wait time	t_{puwait}		200			µs
wait time before normal operation after power up	$t_{clkwait}$			200 × t_{SCLK}		µs

Note #1: for t_{SCLK}, t_{on}, t_{quiet} and t_{1-8}, refer to Figure 2.

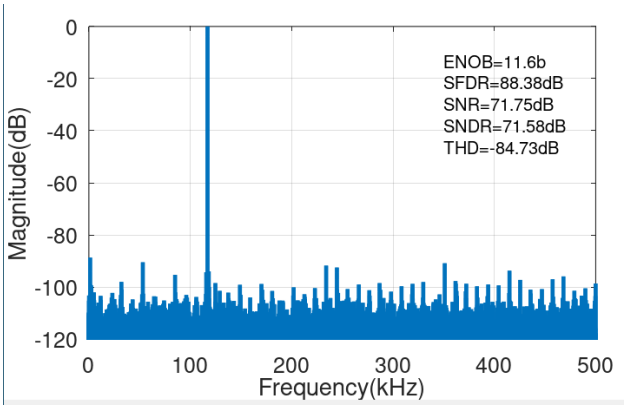
Note #2: for t_{puwait} and $t_{clkwait}$, refer to Figure 12.

TYPICAL CHARACTERISTICS – MDC97476

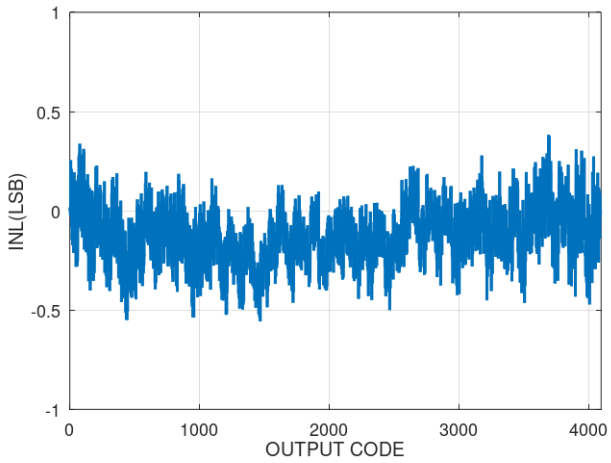
VDD = 3.3 V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS, T_A = 25°C, unless otherwise noted

Dynamic Performance

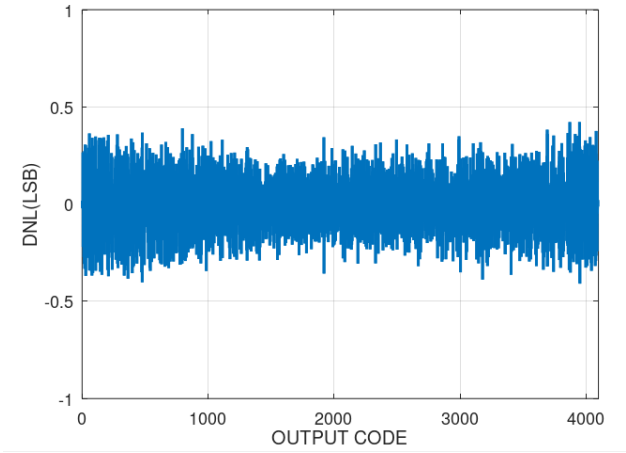
f_{IN} = 117kHz



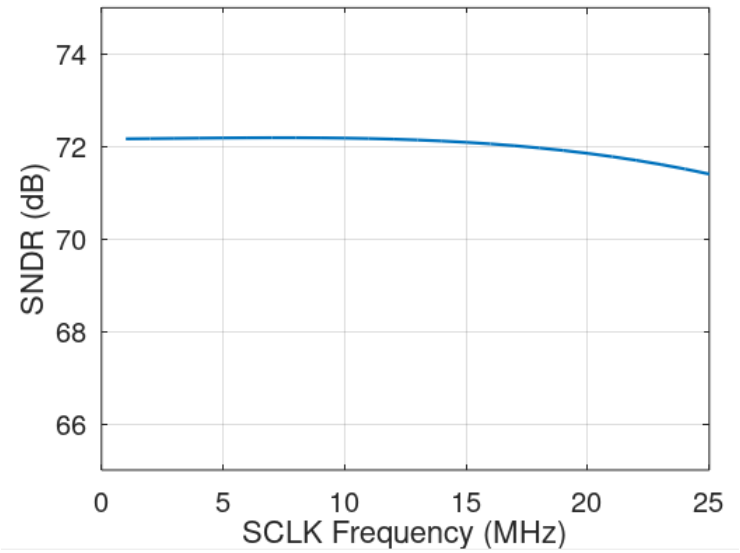
INL



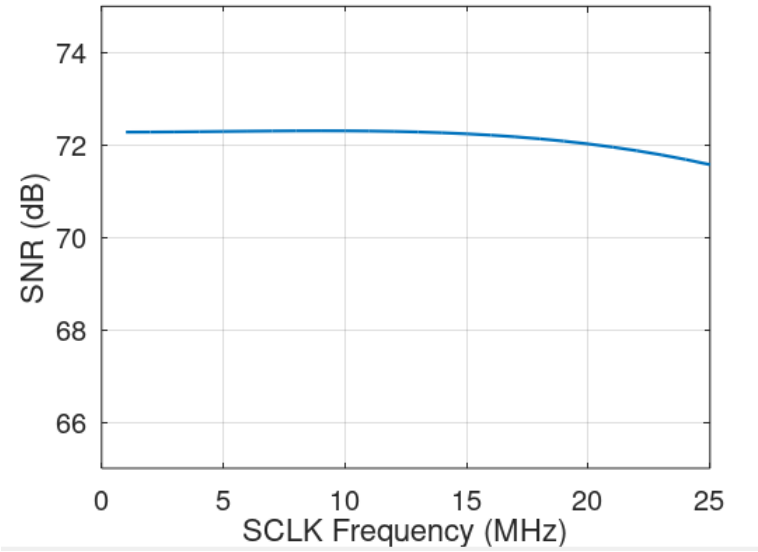
DNL



SNDR vs SCLK frequency



SNR vs SCLK frequency



FUNCTIONAL BLOCK DIAGRAM

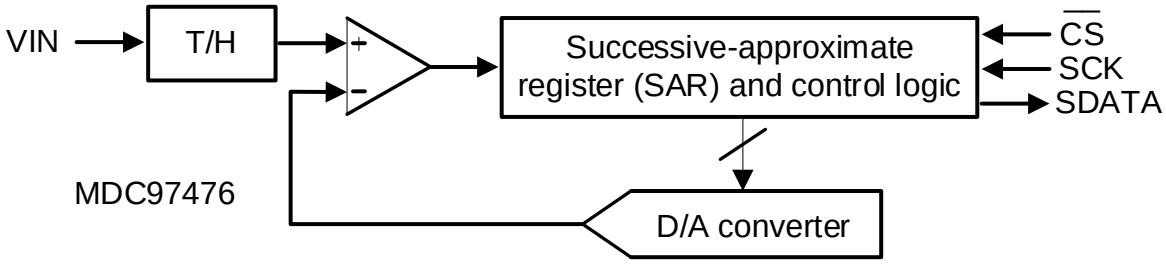


Figure 1: Functional Block Diagram

OPERATION

The MDC97476 is 12-bit, fast, micropower, single-supply successive-approximation analog-to-digital converters (ADCs). Operating from a single 3.3V supply, the MDC97476 is capable of throughput rates of 1 MSPS with a 20 MHz input clock.

Each MDC97476 provides an on-chip, track-and-hold ADC and a serial interface in a tiny 6-lead TSOT-23 package. The serial clock input accesses data from the part and provides the clock source for the SAR. The analog input range is 0 V to VDD. There is no on-chip reference, and no external reference is required for the ADC. The reference for the MDC97476 is derived from the power supply and thus provides the widest dynamic input range.

As shown in **Figure 1**, there are 4 I/O pins. VIN is the analog input signal pin. $\overline{CS}$ is chip select, which indicates the starting of conversion process. SCLK is input clock, which controls the timing of serial data. SDATA is the serial data output pin, which outputs the conversion result.

The falling edge of $\overline{CS}$ indicates the end of signal tracking phase and the start of conversion process. Meanwhile, SDATA will come out of tri-state and goes to logic low.

At the 13th rising edge of SCLK after $\overline{CS}$ goes to low, the ADC transfers from hold phase to track phase. The SDATA pin goes into tri-state either at the 16th falling edge of SCLK after $\overline{CS}$ goes to low, or at the rising edge of $\overline{CS}$ .After SDATA outputs all data and goes back to tri-state, the ADC must wait a quiet time t_{QUIET} before starting a new conversion, i.e., the next falling edge of $\overline{CS}$ must be longer than quiet time t_{QUIET}, see **Figure 2**.

To read a complete sample from the MDC97476, $\overline{CS}$ must keep low along with at least 16 SCLK cycles. The SDATA are clocked out on falling edges of SCLK. SDATA on MDC97476 outputs 4 leading zeroes first, then followed by 12 data bits (order: MSB first). After the data bits, MDC97476 SDATA goes into tri-state. Please be noted, the falling edge of $\overline{CS}$ shall only happen when $SCLK$ is logic high. The detailed timing diagrams are shown in **Figure 2**.

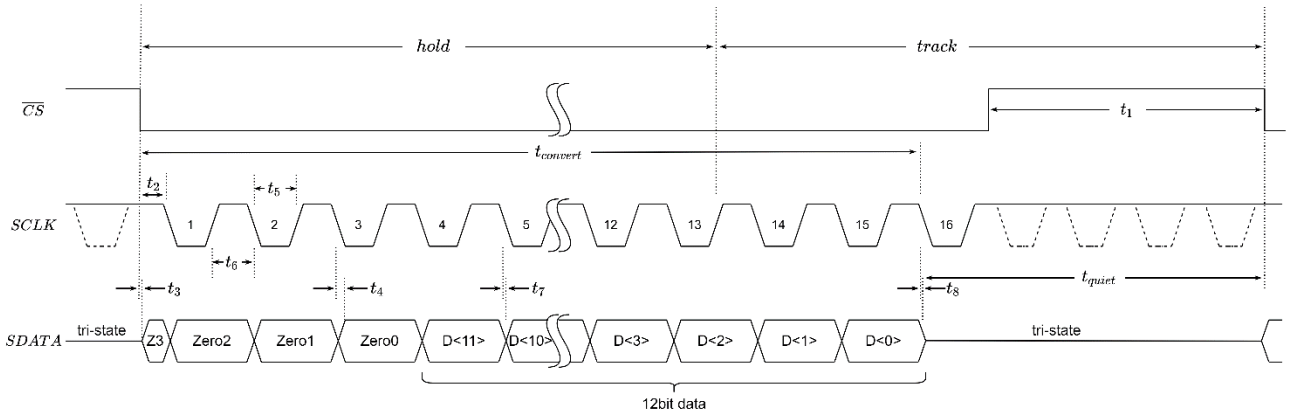


Figure 2: MDC97476 serial interface timing diagram

DEVICE FUNCTIONAL STAGES

The MDC97476 is fast, micropower, single-supply successive-approximation ADCs with charge redistribution DAC. **Figure 3** and **Figure 4** are brief schematics of the ADC in track phase and hold phase.

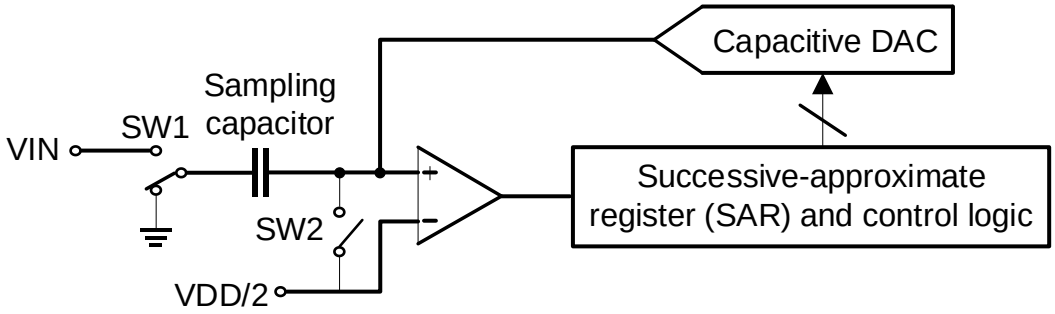


Figure 3: MDC97476 in hold phase

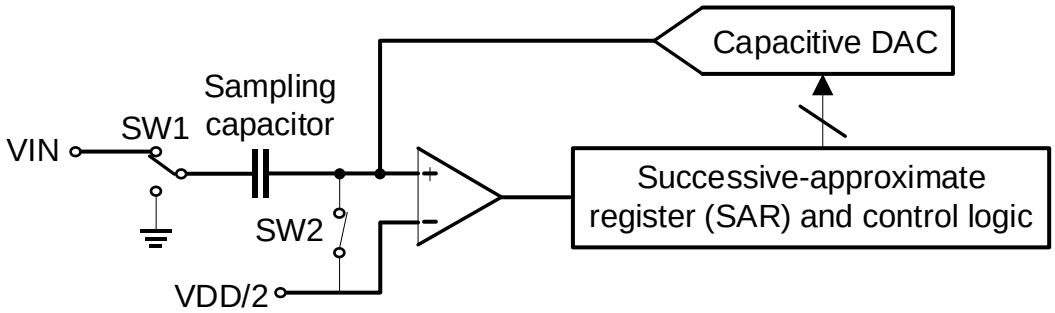


Figure 4: MDC97476 in track phase

Figure 3 shows the device in hold phase: SW2 is open, the sampling capacitor is connected to ground via SW1, maintaining the sampled voltage. The control logic then controls the capacitive DAC to add or subtract charge from the sampling capacitor until the comparator is balanced.

After the comparator is balanced, the control code applied to the DAC is the digital value of the analog input voltage. Then the device can move into track phase as shown in **Figure 4**. In track phase, SW2 is closed, and comparator is balanced, SW1 connects the sampling capacitor to VIN thus stored the input voltage on the sampling capacitor.

ADC TRANSFER FUNCTION

The output coding of the MDC97476 is straight binary. Code transitions occur at integer LSB values, such as 1 LSB, 2 LSB, and so on. The LSB size for the MDC97476 is VDD/4096. **Figure 5** shows the ideal transfer characteristic for the MDC97476.

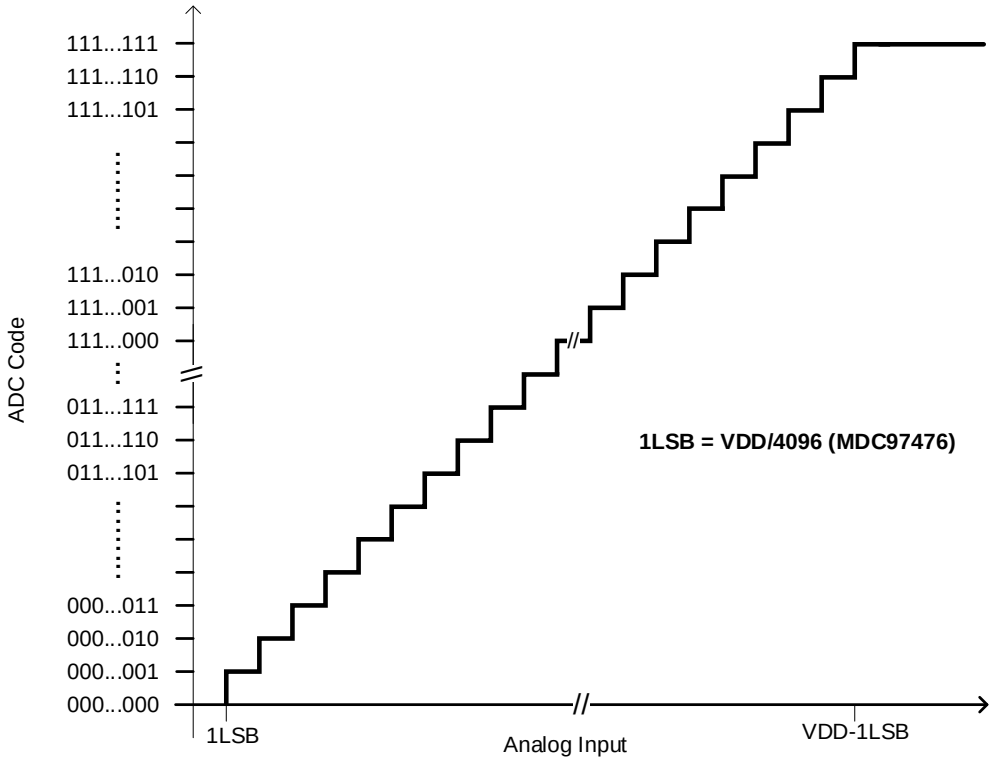


Figure 5: MDC97476 ideal transfer curve

ANALOG INPUT

Figure 6 shows an equivalent circuit for the MDC97476 input pin (V_{IN}). The input absolute voltage range should be between GND – 300 mV and VDD + 300 mV. Two diodes, D1 and D2, provide ESD protection for the analog input. The capacitor C1 in **Figure 6** represents the input pin capacitance, and typical value is 2 pF. The resistor R1 represents the lumped ON resistance of the track and hold switch. The capacitor C2 represents the ADC sampling capacitor, and typical value is 14 pF.

In applications where harmonic distortion and signal-to-noise ratio are critical, MDC97476 should be driven by a low-impedance source. A band-pass or low-pass filter is helpful to reduces harmonics and noise in improving THD and SNR performance.

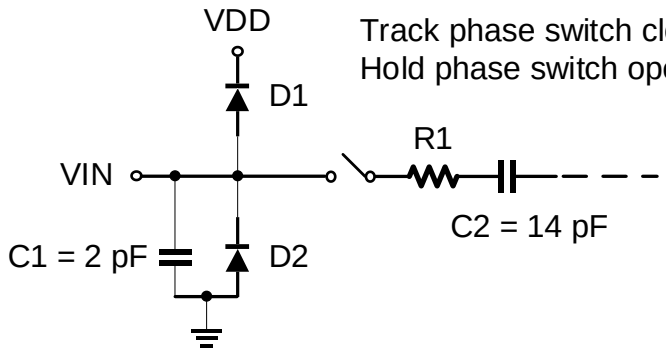


Figure 6 Equivalent analog input circuit

DIGITAL INPUTS

Similar ESD protection circuits are used in digital inputs and output, so the digital inputs and output voltage applied to the MDC97476 shares the same limitation of analog input.

MODES OF OPERATION

By controlling $\overline{CS}$ signal during conversion, MDC97476 can go into two possible modes: normal mode and sleep mode. The device enters normal mode when $\overline{CS}$ signal goes low and enters sleep mode when $\overline{CS}$ pulled high before the 10th falling edge of SCLK after $\overline{CS}$ is pulled low. Choosing different modes can help to optimize the power dissipation/throughput rate ratio for different application requirements.

NORMAL MODE

To keep the device in normal mode continuously, $\overline{CS}$ must be kept low until after the 10th falling edge of SCLK after the start of a conversion (remember that a conversion is initiated by bringing $\overline{CS}$ low).

The MDC97476 can obtain best throughput performance if stay in normal mode as there is no wake-up delay.

If $\overline{CS}$ is brought high after the 10th falling edge, and before the 16th falling edge, the device stays in normal mode, but the current conversion is aborted, and SDATA goes into tri-state.

If $\overline{CS}$ keeps low for more than 16 SCLK clock cycles, SDATA returns to tri-state at 16th SCLK clock falling edge as shown in **Figure 7**. A new conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by bringing $\overline{CS}$ low again.

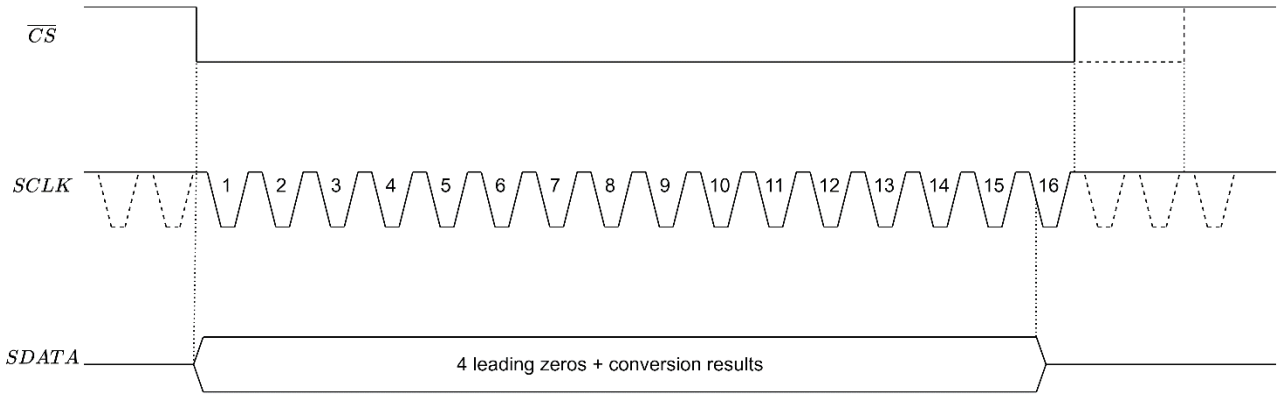


Figure 7: Normal mode operation

SLEEP MODE

Sleep Mode is intended for saving power consumption in applications that either sample discontinuously, or slow throughput rate. When the MDC97476 is in sleep mode, most of the analog circuitry is turned off.

Figure 8 shows how the device enter sleep mode. When $\overline{CS}$ is brought high after the 2nd falling edge and before the 10th falling edge, conversion would be interrupted, and device will enter sleep mode 2 cycles later. The current conversion is aborted and SDATA enters tri-state. If $\overline{CS}$ is brought high before the 2nd falling edge of SCLK, the device stays in normal mode; this prevents noise on the $\overline{CS}$ line accidentally changing mode.

To exit sleep mode, bring $\overline{CS}$ back low. At the falling edge of $\overline{CS}$, the MDC97476 begins waking up. Wake up typically takes 50 µs. This wake-up delay results in the first 50 conversion results being unusable. The valid result starts from the 51st conversion performed after wake-up begin, as shown in **Figure 9**.

If $\overline{CS}$ is brought back high before the 10th falling edge of SCLK, the device returns to sleep mode. This is done to avoid accidentally entering normal mode as a result of noise on the $\overline{CS}$ line. To exit sleep mode and remain in normal mode, $\overline{CS}$ must be kept low until after the 10th falling edge of SCLK.

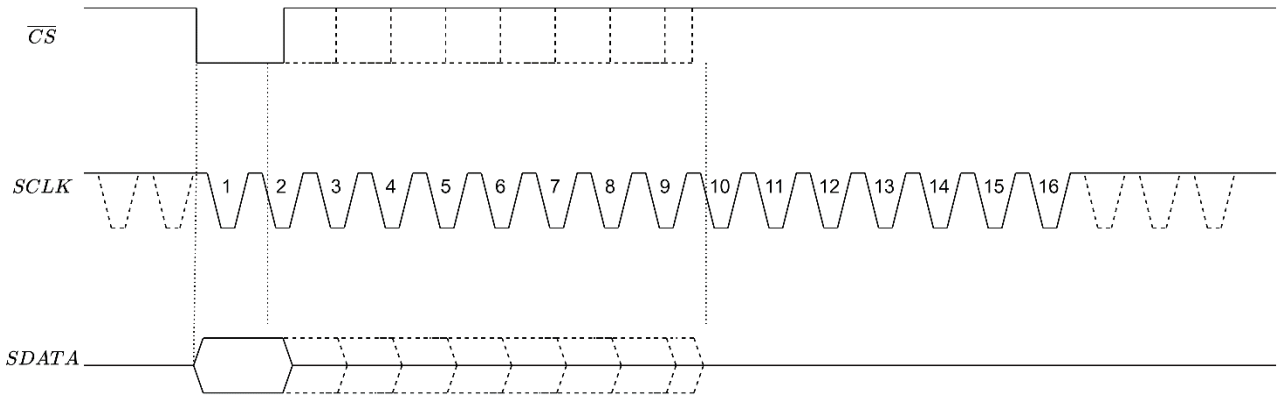


Figure 8 Entering sleep mode

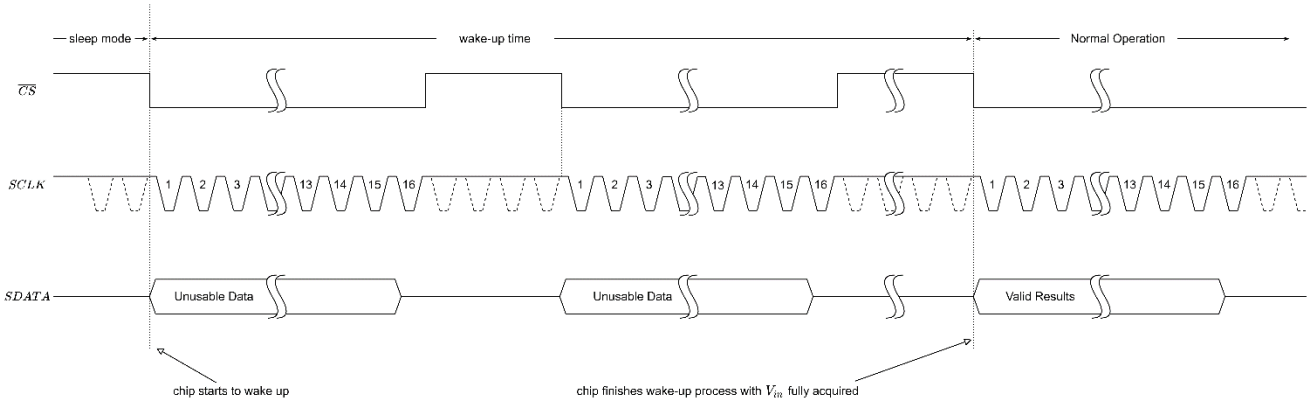


Figure 9 Wake up from sleep mode

POWER UP SEQUENCE

After VDD is up and stable, at least 200 cycles ($t_{clkwait}$) of stable $SCLK$ after at least 200 μs (t_{puwait}) to MDC97476 should be provided to help it get fully powered up. This $t_{clkwait}$ period is equivalent to 10 dummy samples operating $\overline{CS}$ and $SCLK$ in normal operation. During this time ($t_{clkwait}$), $\overline{CS}$ can be either high or low. It is recommended to keep $\overline{CS}$ high or operate $\overline{CS}$ the same manner in normal operation.

Figure 10 shows the detailed power up timing sequence.

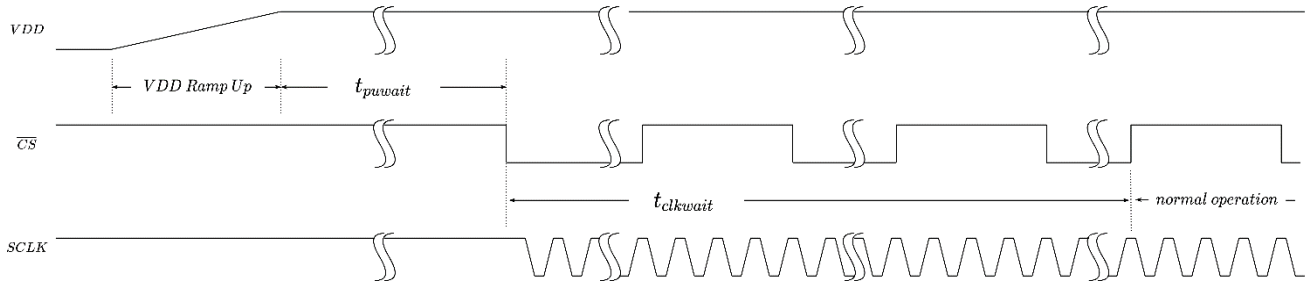


Figure 10 Power up sequence

TYPICAL APPLICATION

The reference voltage is critical for optimal ADC performance. Since MDC97476 uses V_{DD} as its reference voltage, V_{DD} must be treated carefully. A uniform ground plane and a dedicated V_{DD} plane are recommended for the MDC97476. The decoupling capacitors should be placed next to V_{DD}/GND pins to provide the best performance. As shown in **Figure 11**.

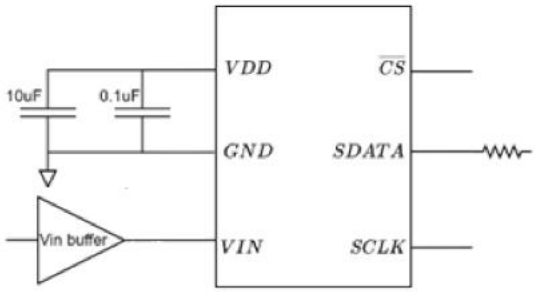


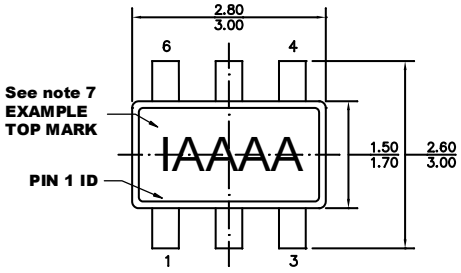
Figure 11 Schematic for typical application

LAYOUT GUIDELINE

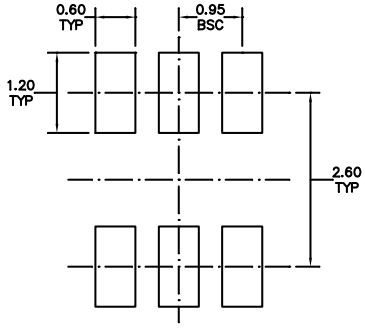
The reference voltage is critical for optimal ADC performance. A noisy reference voltage affects SNR and SINAD performance. Since MDC97476 uses V_{DD} as its reference voltage, V_{DD} must be treated carefully. A uniform ground plane and a dedicated V_{DD} plane are recommended for the MDC97476. The decoupling capacitors should be low ESR/ESL and placed next to V_{DD}/GND pins on the same side as the chip to provide the best performance.

PACKAGE INFORMATION

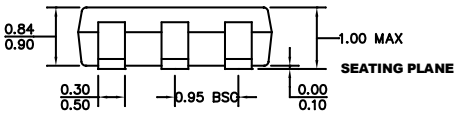
PACKAGE OUTLINE DRAWING FOR 6L TSOT23
MF-PO-D-0011 revision 3.0



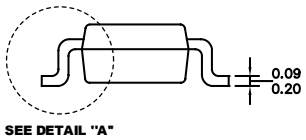
TOP VIEW



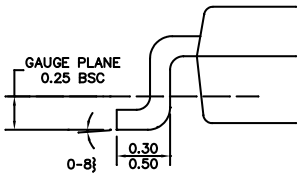
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)