microSD 6.10 Specification
Industrial grade wide temperature

v. 1.1

MK Founder Technology Co., Limited

Revision History

Revision	Release Date	History	Author
1.0	2021/09/03	First release	Eason
1.1	2022/07/05	Update Page #4, 5, 9 & 12 for added TLC product info	Ella

Overview

- **Capacity**
  - 64GB to 256GB
- **Flash Type**
  - TLC
- **Bus Speed Mode**
  - Up to UHS-104
- **Power Consumption**
  - Power Up Current < 250uA
  - Standby Current < 1mA
  - Read Current <400mA
  - Write Current <400mA
- **Performance**
  - Read: Up to 95 MB/s
  - Write: Up to 85 MB/s
- **CPRM optional (Content Protection for Recordable Media)**
- **MTBF**
  - More than 3,000,000 hours
- **Advanced Flash Management**
  - Static and Dynamic Wear Leveling
  - Bad Block Management
  - SMART Function[Noted2]
  - Auto-Read Refresh
  - Embedded Mode
- **Storage Temperature Range**
  - -40°C ~ 85°C
- **Operation Temperature Range**
  - -40°C ~ 85°C
- **RoHS compliant**
- **EMI compliant**

Performance and Power Consumption

Part Number	Capacity	Flash Structure	Specification	Performance		Power Consumption (MAX)		
				TestMetrixTest @500MB		Read (mA)	Write (mA)	Standby (mA)
				Read (MB/s)	Write (MB/s)			
MKUS064G-ISU1	64GB	64GB x 1	A2, V30, U3	95	50	400	400	1
MKUS128G-ISU2	128GB	64GB x 2	A2, V30, U3	95	85	400	400	1
MKUS256G-ISU4	256GB	64GB x 4	A2, V30, U3	95	85	400	400	1

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1. INTRODUCTION

1.1. General Description

The Micro Secure Digital (microSD) card version 6.10 is fully compliant to the specification released by SD Card Association. The Command List supports [Part 1 Physical Layer Specification Ver6.10 Final] definitions. Card Capacity of Non-secure Area, Secure Area Supports [Part 3 Security Specification Ver4.00 Final] Specifications.

The microSD 6.10 card comes with 8-pin interface, designed to operate at a maximum operating frequency of 208MHz. It can alternate communication protocol between the SD mode and SPI mode. It performs data error detection and correction with very low power consumption. Its capacity could reach 256GB with exFAT SDXC.

MK Industrial micro Secure Digital 6.10 card is one of the most popular cards today based on its high performance, good reliability and wide compatibility. Not to mention that it's well adapted for hand-held applications in semi-industrial/medical markets already. Moreover, with customized firmware technique.

1.2. Flash Management

1.2.1. Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, We applies the LDPC Algorithm, which can detect and correct errors occur during Read process, ensure data been read correctly, as well as protect data from corruption.

1.2.2. Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas are getting updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

MK provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND Flash is greatly improved.

1.2.3. Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. MK implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

1.2.4. Smart Function

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is a special function that allows a memory device to automatically monitor its health. MK provides a program named SmartInfo Tool to observe MK’s SD and microSD cards. **Note that this tool can only support MK’s industrial SD and microSD cards.** This tool will display the controller version, flash type, firmware version, endurance life ratio, good block ratio, and so forth. In addition, a warning message will appear under the following 3 conditions:

(1) When the life ratio remained is less than **10%**,

(2) When the amount of abnormal power on is more than **3,500** cycles, and

(3) When there are less than **5** usable blocks for replacing bad blocks.

1.2.5. Auto-Read Refresh

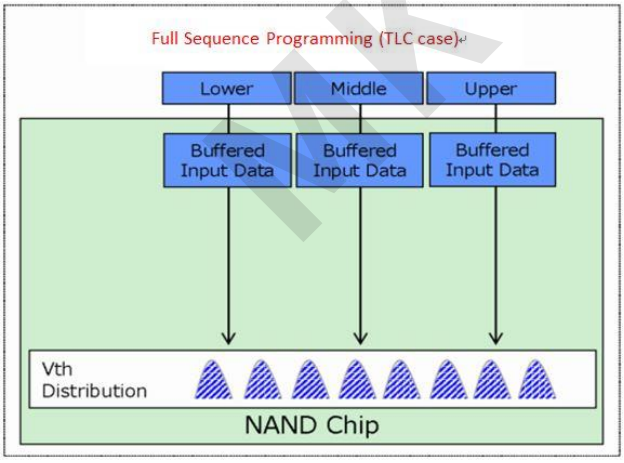
Auto-Read Refresh is especially applied on devices that read data mostly but rarely write data, such as GPS. When blocks are continuously read, then the device cannot activate wear leveling since it can only be applied while writing data. Thus, errors will accumulate and become uncorrectable. Accordingly, to avoid errors exceed the amount ECC can correct and blocks turn bad, MK's firmware will automatically refresh the bit errors when the error number in one block approaches the threshold, ex., 24 bits.

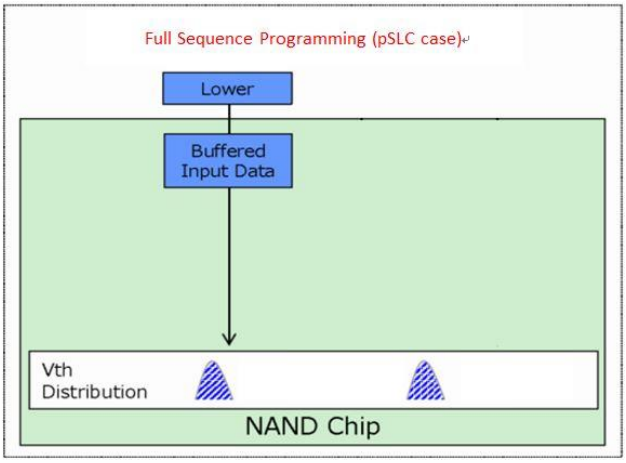
1.2.6. Embedded Mode

Embedded mode is a function specially designed for operating systems that do not utilize FAT. Often under non Windows OS, for example Linux or customized host, wear leveling mechanism of MK's cards will be affected or even disabled in some cases. With embedded mode activated, MK's cards ensure that under any circumstances, wear leveling mechanism can operate normally to keep the usage of blocks even throughout the card's life cycle. This is especially a great add-on for security cameras or drive recorders.

1.2.7. Pseudo SLC

Pseudo SLC can be considered as an extended version of TLC. While TLC does Full Sequence Programming into 8 Vth distribution, pSLC only does lower page programming into 2 Vth distribution. Accordingly, because only Lower pages are programmed, pSLC provides better performance and endurance than TLC. Moreover, pSLC performs similarly with SLC, yet pSLC is more cost-effective





2. PRODUCT SPECIFICATIONS

- **Capacity**
  - 64GB to 256GB
- **Operation Temp. Range**
  - -40~+85°C
- **Storage Temp. Range**
  - -40~+85°C
- **Support File System Specification Ver3.00**
- **Card capacity of non-secure area and secure area support [Part 3 Security Specification Ver4.0 Final] Specifications**
- **Support SD SPI mode**
- **Designed for read-only and read/write cards**
- **Bus Speed Mode (use 4 parallel data lines)**
  - **UHS-I mode**
    - SDR12: SDR up to 25MHz, 1.8V signaling
    - SDR25: SDR up to 50MHz, 1.8V signaling
    - SDR50: 1.8V signaling, frequency up to 100MHz, up to 50 MB/sec
    - SDR104: 1.8V signaling, frequency up to 208MHz, up to 104MB/sec.
    - DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50 MB/sec

    Note: Timing in 1.8V signaling is different from that of 3.3V signaling.
- **The command list supports [Part 1 Physical Layer Specification Ver6.10 Final] definitions**
- **Copyrights Protection Mechanism**
  - Compliant with the highest security of SDMI standard
- **Support optional CPRM (Content Protection for Recordable Media) of SD Card**
  - Compliant with [Physical Layer Specification Ver6.10 Final] CPRM optional definition.

    Note: CPRM card is compliant with [Physical Layer Specification Ver5.10 Final]
- **Password Protection of cards (optional)**
- **Write Protect feature using mechanical switch**
- **Built-in write protection features (permanent and temporary)**
- **Operation voltage range: 2.7 ~ 3.6V**

3.1. microSD Card Pins

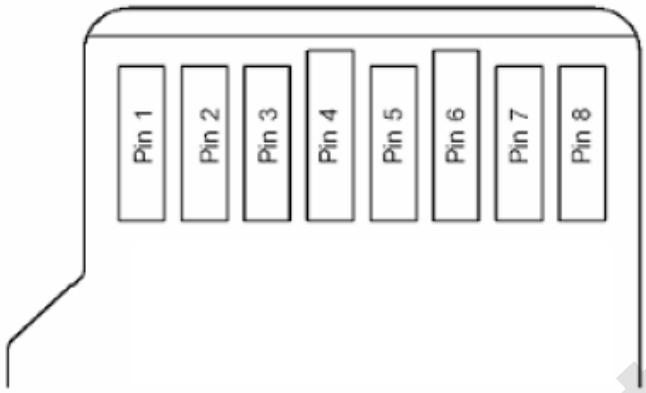


Figure 3-1 microSD Card Pin assignment (Back View of the card)

Table 3-1 microSD Memory Card Pad Assignment

pin	SD Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type	Description
1	DAT2	I/O/PP	Data Line [bit2]	RSV		
2	CD/DAT3 [2]	I/O/PP [3]	Card Detect/ Data Line [bit3]	CS	I [3]	Chip Select (neg. true)
3	CMD	PP	Command/Response	DI	I	Data In
4	V_{DD}	S	Supply voltage	V_{DD}	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS}	S	Supply voltage ground	V_{SS}	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line [bit1]	RSV		

(1) S: power supply, I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers.

(2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode as well while they are not used. It is defined so in order to keep compatibility to MultiMedia Cards.

(3) At power up, this line has a 50KOhm pull up enabled in the card. This resistor serves two functions: Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode, it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer with SET_CLR_CARD_DETECT (ACMD42) command.

3.2. microSD Card Bus Topology

The microSD card supports 2 alternative communication protocols, SD and SPI BUS mode.

Host can choose either one of both bus mode, same data can be read or written by both modes.

SD mode allows 4-bits data transfer ways, it provides high performance. SPI mode supports 1-bit data transfer and of course the performance is lower compared to SD mode.

3.3. SD Bus Mode Protocol

In default speed, the SD Memory Card bus has a single master (application); multiple slaves (Cards), synchronous star topology (refer to Figure 3-2). In high speed and UHS-I, the SD Memory Card bus has a single master (application) and single slave (card), synchronous point to point topology. Clock, power and ground signals are common to all cards. Command (CMD) and data (DAT0-DAT3) signals are dedicated to each card providing continues point to point connection to all the cards.

During initialization process commands are sent to each card individually, allowing the application to detect the cards and assign logical addresses to the physical slots. Data is always sent (received) to (from) each card individually. However, in order to simply the handling of the card stack, after the initialization process, all commands may be sent concurrently to all cards. Addressing information is provided in the command packet. SD bus allows dynamic configuration of the number of data lines. After power up, by default, the SD Memory Card will use only DAT0 for data transfer. After initialization the host can change the bus width (number of data active lines). This feature allows easy tradeoff between HW cost and system performance. Note that while DAT1 to DAT3 are not in use, the related Host's DAT lines should be in tri-state (input mode). For SDIO cards DAT1 and DAT2 are used for signaling.

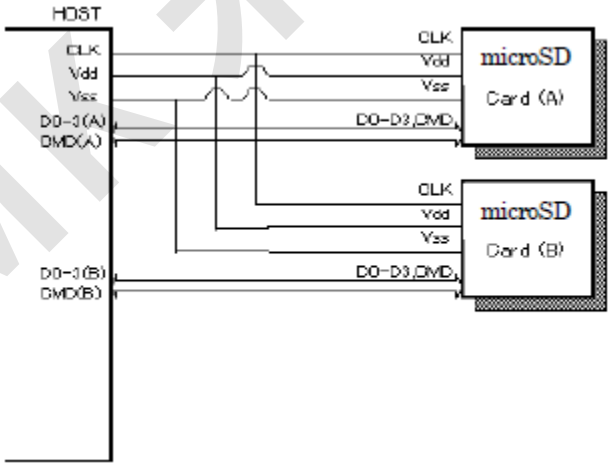


Figure 3-2 SD Memory Card System Bus Topology

The SD bus includes the following signals:

CLK: Host to card clock signal

CMD: Bidirectional Command/Response signal

DAT0-DAT3: 4 Bidirectional data signals

V_{DD}, V_{ss1}, V_{ss2}: Power and ground signals

Table 3-2 SD Mode Command Set

Card Command Class (CCC)	0 basic	1 Command Queue	2 block read	3 reserved	4 block write	5 erase	6 write protection	7 lock card	8 application specific	9 I/O mode	10 switch	11 extension
CMD0	+											
CMD2	+											
CMD3	+											
CMD4	+											
CMD5										+		
CMD6											+	
CMD7	+											
CMD8	+											
CMD9	+											
CMD10	+											
CMD11	+											
CMD12	+											
CMD13	+											
CMD15	+											
CMD16			+		+			+				
CMD17			+									
CMD18			+									
CMD19			+									
CMD20			+		+							
CMD21												+
CMD23			+		+							
CMD24					+							
CMD25					+							
CMD27					+							
CMD28							+					
CMD29							+					
CMD30							+					
CMD32						+						
CMD33						+						
CMD34-37											+	
CMD38						+						
CMD40								+				
CMD42								+				
CMD43-47		+										
CMD48												+
CMD49												+
CMD50											+	
CMD52										+		
CMD53										+		

Card Command Class (CCC)	0 basic	1 Command Queue	2 block read	3 reserved	4 block write	5 erase	6 write protec-tion	7 lock card	8 application specific	9 I/O mode	10 switch	11 extension
CMD55									+			
CMD56									+			
CMD57											+	
CMD58												+
CMD59												+
ACMD6									+			
ACMD13									+			
ACMD14									+			
ACMD15									+			
ACMD16									+			
ACMD22									+			
ACMD23									+			
ACMD28									+			
ACMD41									+			
ACMD42									+			
ACMD51									+			

Commands	Support requirements
CMD0	Mandatory
CMD2	Mandatory
CMD3	Mandatory
CMD4	Mandatory
CMD5	Optional
CMD6	Mandatory for cards version 1.10 and after
CMD7	Mandatory
CMD8	Mandatory for cards version 2.00 and after
CMD9	Mandatory
CMD10	Mandatory
CMD11	Mandatory for cards supporting UHS-I. Optional for cards that do not support UHS-I.
CMD12	Mandatory
CMD13	Mandatory
CMD15	Mandatory
CMD16	Mandatory
CMD17	Mandatory
CMD18	Mandatory
CMD19	Mandatory for cards supporting UHS-I. Optional for cards that do not support UHS-I.

Commands	Support requirements
CMD20	Not supported for SDSC cards. Mandatory for SDHC and SDXC cards that support Video Speed Class. Optional for SDHC cards that support: a) Speed Class; or b) UHS Speed Grade, and do not support Video Speed Class. Mandatory for SDXC cards that support Speed Class or UHS Speed Grade.
CMD21	Optional
CMD23	Not supported for SDSC cards. Mandatory for SDHC and SDXC cards that support UHS104. Optional for SDHC and SDXC cards that do not support UHS104.
CMD24	Mandatory for writable types of cards
CMD25	Mandatory for writable types of cards
CMD27	Mandatory for writable types of cards
CMD28	Optional
CMD29	Optional
CMD30	Optional
CMD32	Mandatory for writable types of cards
CMD33	Mandatory for writable types of cards
CMD34-37	Optional for cards version 1.10 and after
CMD38	Mandatory for writable types of cards Discard and FULE support is optional
CMD40	Optional
CMD42	Optional for cards version 1.01 and 1.10. Mandatory for cards version 2.00 and after. COP support is optional for CMD42
CMD43-47	Mandatory for cards supporting Command Queue
CMD48	Optional Mandatory for cards supporting Performance Enhancement functions (refer to 5.8.2)
CMD49	Optional Mandatory for cards supporting Performance Enhancement functions (refer to 5.8.2)
CMD50	Optional for cards version 1.10 and after
CMD52	Optional
CMD53	Optional
CMD55	Mandatory
CMD56	Mandatory
CMD57	Optional for cards version 1.10 and after
CMD58	Optional
CMD59	Optional
ACMD6	Mandatory
ACMD13	Mandatory
ACMD14	Optional
ACMD15	Optional

Commands	Support requirements
ACMD16	Optional
ACMD22	Mandatory for writable types of cards
ACMD23	Mandatory for writable types of cards
ACMD28	Optional
ACMD41	Mandatory
ACMD42	Mandatory
ACMD51	Mandatory

3.4. SPI Bus Mode Protocol

While the SD Memory Card channel is based on command and data bit streams that are initiated by a start bit and terminated by a stop bit, the SPI channel by byte oriented. Every command or data block is built for 8-bit bytes and is byte aligned with the CS signal (i.e. the length is a multiple of 8 clock cycles). The card starts to count SPI bus clock cycle at the assertion of the CS signal. Every command or data token shall be aligned with 8-clock cycle boundary.

Similar to the SD Memory Card Protocol, the SPI messages consist of command, response and data-block tokens.

The advantage of SPI mode is reducing the host design effort, especially for MMC host side, it just be modified by little change. Note: please use SD card specification to implement SPI mode function, not use MMC specification. For example, SPI mode is initialized by ACMD41, and the registers are different from MMC card, especially CSD register.

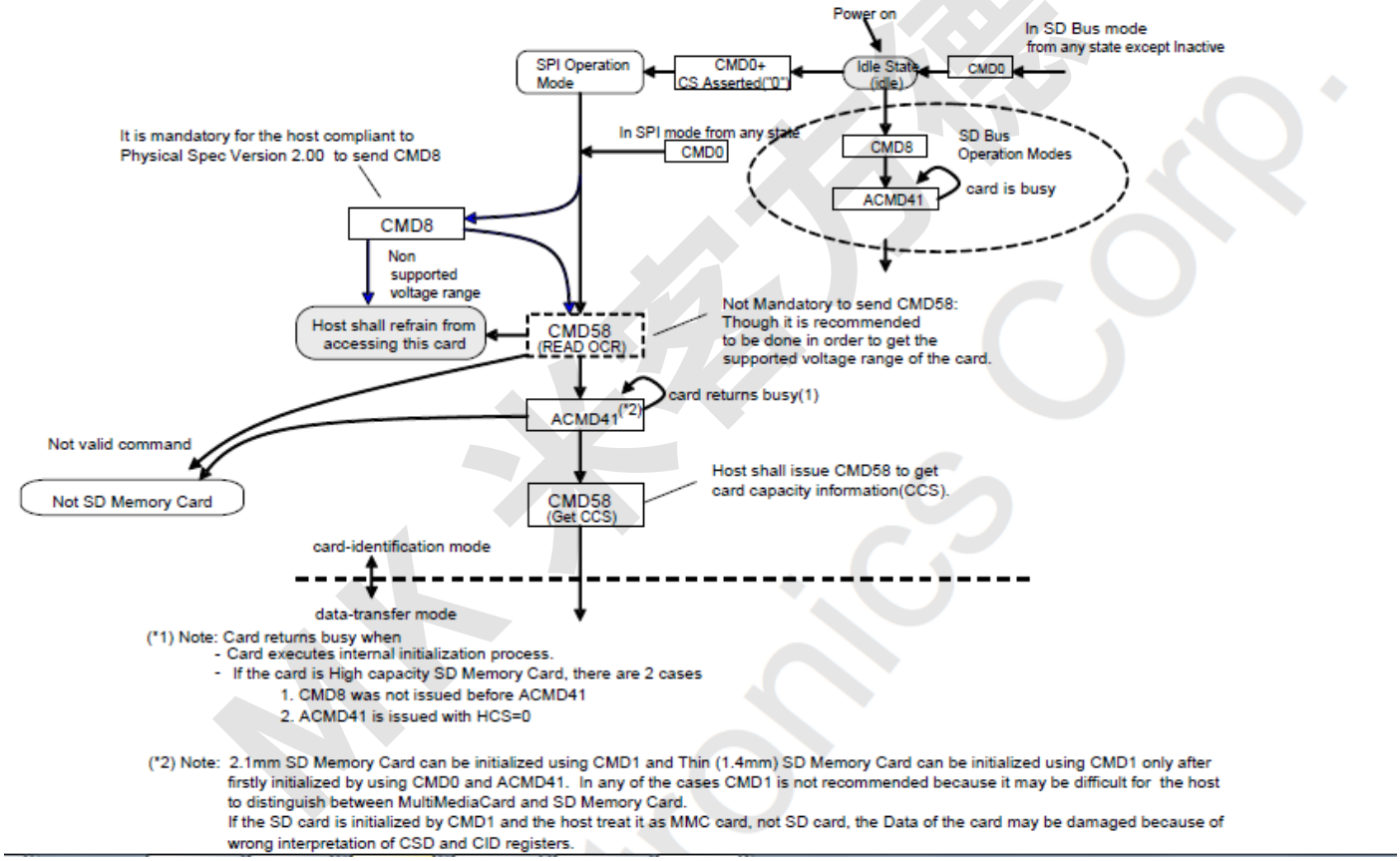


Figure 3-3 SD Memory Card State Diagram (SPI mode)

Table 3-3 SPI Mode Command Set

Card Command Class (CCC)		0	1	2	3	4	5	6	7	8	9	10	11
Supported commands	class description	basic	reserved	block read	reserved	block write	erase	write protection	lock card	application specific	I/O mode	switch	reserved
CMD0	Mandatory	+											
CMD1	Mandatory	+											
CMD5	Optional										+		
CMD6[2]	Mandatory											+	
CMD8[3]	Mandatory	+											
CMD9	Mandatory	+											
CMD10	Mandatory	+											
CMD12	Mandatory	+											
CMD13	Mandatory	+											
CMD16	Mandatory			+		+			+				
CMD17	Mandatory			+									
CMD18	Mandatory			+									
CMD24	Mandatory[1]					+							
CMD25	Mandatory[1]					+							

Card Command Class (CCC)		0	1	2	3	4	5	6	7	8	9	10	11
Supported commands	class description	basic	reserved	block read	reserved	block write	erase	write protection	lock card	application specific	I/O mode	switch	reserved
CMD27	Mandatory[1]					+							
CMD28	Optional							+					
CMD29	Optional							+					
CMD30	Optional							+					
CMD32	Mandatory[1]						+						
CMD33	Mandatory[1]						+						
CMD34-37[2]	Optional											+	
CMD38	Mandatory[1]						+						
CMD42[4]	(Note 4)								+				
CMD50[2]	Optional											+	
CMD52	Optional										+		
CMD53	Optional										+		
CMD55	Mandatory									+			
CMD56	Mandatory									+			
CMD57[2]	Optional											+	
CMD58	Mandatory	+											
CMD59	Mandatory	+											
ACMD13	Mandatory									+			
ACMD22	Mandatory[1]									+			
ACMD23	Mandatory[1]									+			
ACMD41	Mandatory									+			
ACMD42	Mandatory									+			
ACMD51	Mandatory									+			

Note (1): The commands related write and erase are mandatory only for the Writable types of Cards.
Note (2): This command was defined in spec version 1.10
Note (3): This command is newly defined in version 2.00
Note (4): This command is optional in Version 1.01 and 1.10 and mandatory from Version 2.00. COP support is optional for CMD42

3.5. SD/microSD card initialization

Figure 3-4 presents the initialization flow chart for UHS-I hosts and Figure 3-5 shows sequence of commands to perform voltage switch.

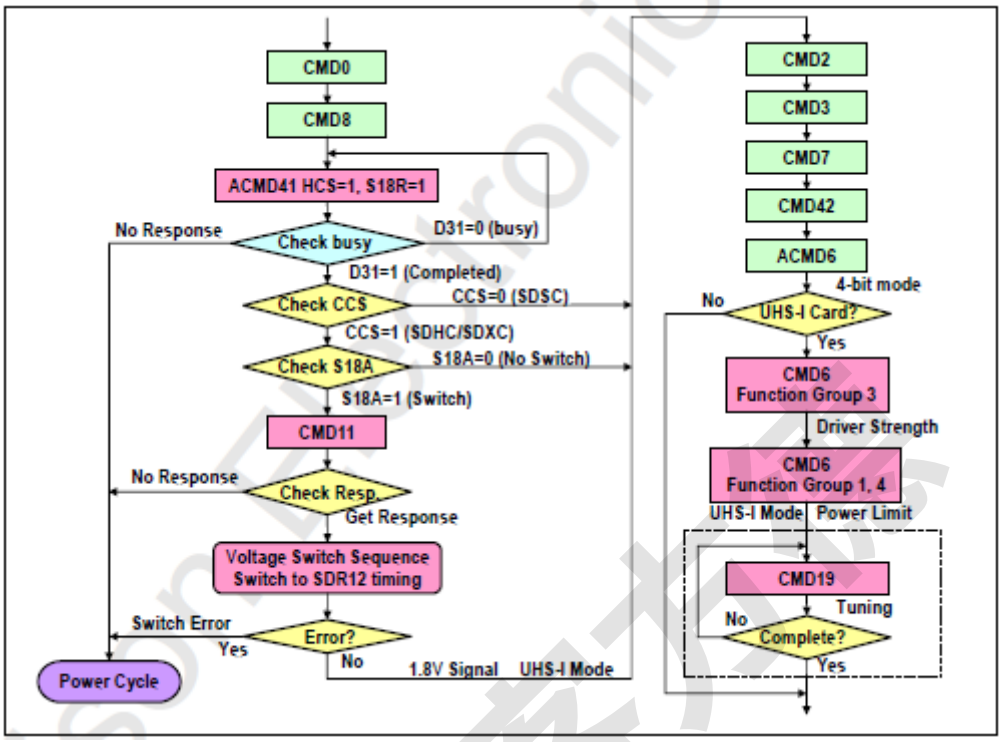


Figure 3-4 UHS-I Host Initialization Flow Chart

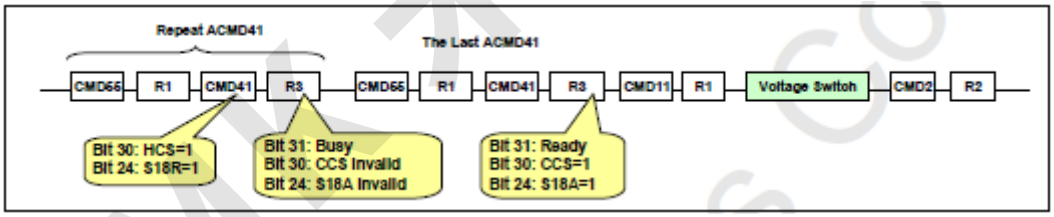


Figure 3-5 ACMD41 Timing Followed by Voltage Switch Sequence

When signaling level is 3.3V, host repeats to issue ACMD41 with HCS=1 and S18R=1 until the response indicates ready. The argument (HCS and S18R) of the first ACMD41 is effective but the all following ACMD41 should be issued with the same argument.

If Bit31 indicates ready, host needs to check CCS and S18A.

The card indicates S18A=0, which means that voltage switch is not allowed and the host needs to use current signaling level.

Table 3-4 S18R and S18A Combinations

Current Signaling Level	S18R	S18A	Comment
3.3V	0	0	1.8V signaling is not requested
	1	0	The card does not support 1.8V signaling
	1	1	Start signal voltage switch sequence
1.8V	X	0	Already switched to 1.8V

To change signaling level at the same time between host and card, signal voltage switch sequence is invoked by CMD11 as shown in Figure 3-6. CMD11 is issued only when S18A=1 in the response of ACMD41.

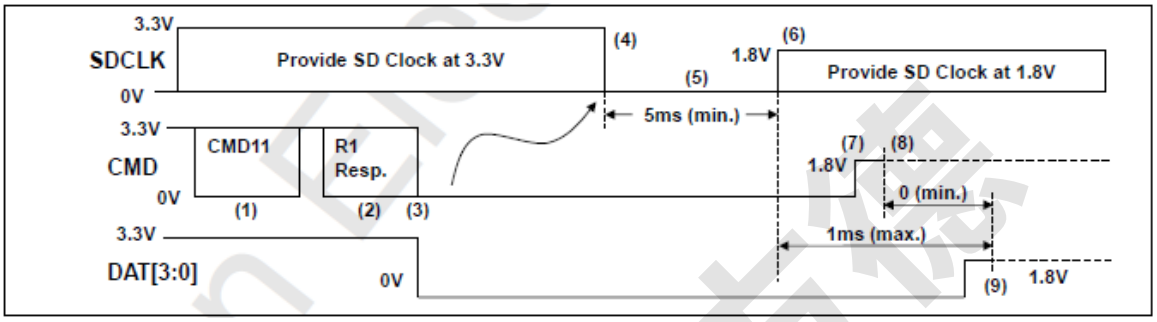


Figure 3-6 Signal Voltage Switch Sequence

4. ENVIRONMENTAL SPECIFICATIONS

4.1. Environmental Conditions

Temperature and Humidity

- Storage Temperature Range
  - -40°C ~ 85°C
- Operation Temperature Range
  - -40°C ~ 85°C

Table 4-1 High Temperature Test Condition

	Temperature	Humidity	Test Time
Operation	85°C	0% RH	300 hours
Storage	85°C	0% RH	500 hours

Result: No any abnormality is detected.

Table 4-2 Low Temperature Test Condition

	Temperature	Humidity	Test Time
Operation	-40°C	0% RH	168 hours
Storage	-40°C	0% RH	500 hours

Result: No any abnormality is detected.

Table 4-3 High Humidity Test Condition

	Temperature	Humidity	Test Time
Operation	55°C	95% RH	4 hours
Storage	55°C	95% RH	500 hours

Result: No any abnormality is detected.

Table 4-4 Temperature Cycle Test

	Temperature	Test Time	Cycle
Operation	-40°C	30 min	20 Cycles
	85°C	30 min	
Storage	-40°C	30 min	50 Cycles
	85°C	30 min	

Result: No any abnormality is detected.

Shock

Table 4-5 Shock Specification

	Acceleration Force	Half Sin Pulse Duration
Industrial SD/microSD card	1500G	0.5ms

Result: No any abnormality is detected when power on.

Vibration

Table 4-6 Vibration Specification

	Condition		Vibration Orientation
	Frequency/Displacement	**Frequency/Acceleration**	
Industrial microSD card	20Hz~80Hz/1.52mm	80Hz~2000Hz/20G	X, Y, Z axis/30 min for each

Result: No any abnormality is detected when power on.

Drop

Table 4-7 Drop Specification

	Height of Drop	Number of Drop
Industrial SD/microSD card	150cm free fall	6 face of each unit

Result: No any abnormality is detected when power on.

Bending

Table 4-8 Bending Specification

	Force	Action
Industrial SD/microSD card	≥ 10N	Hold 1min/5times

Result: No any abnormality is detected when power on.

Torque

Table 4-9 Torque Specification

	Force	Action
Industrial SD/microSD card	0.1N-m or +/-2.5 deg	Hold 30 seconds/5times

Result: No any abnormality is detected when power on.

Salt Spray Test

Table 4-10 Salt Spray Specification

	Condition	Action
Industrial microSD card	Concentration: 3% NaCl Temperature: 35℃	Storage for 24 HRS

Result: No any abnormality is detected when power on.

Waterproof Test

Table 4-11 Waterproof Specification

	Condition	Action
Industrial microSD card	Water temperature: 25℃ Water depth: The lowest point of unit is locating 1000mm below surface.	Storage for 30 mins

Result: JIS IPX7 compliance. No any abnormality is detected when power on.

Test X-Ray Exposure Test

Table 4-12 X-Ray Exposure Specification

	Condition	Action
Industrial microSD card	0.1 Gy of medium-energy radiation (70 keV to 140 keV, cumulative dose per year) to both sides of the card	Storage for 30 mins

Result: ISO 7816-1 compliance. No any abnormality is detected when power on.

Switch Cycle Test

Table 4-13 Switch Cycle Test

	Applied Force	Result
Industrial microSD card	0.4~0.5 N 1000 times	PASS

Result: No any abnormality is detected when power on

Durability Test

Table 4-14 Durability Test

	Mating cycle	Result
Industrial microSD card	10000 times	PASS

Result: No any abnormality is detected when power on

Electrostatic Discharge (ESD)

Table 4-15 Contact ESD Specification

	Condition	Result
Industrial microSD card	Contact: +/- 4KV each item 25 times Air: +/- 8KV 10 times	PASS

EMI Compliance

- FCC: CISPR22
- CE: EN55022
- BSMI 13438

4.2. MTBF

MTBF, an acronym for Mean Time Between Failures, is a measure of a device's reliability. Its value represents the average time between a repair and the next failure. The measure is typically in units of hours. The higher the MTBF value, the higher the reliability of the device. The predicted result of MK's microSD/SD is more than 3,000,000 hours.

Analysis software: Relex7.3
Analysis Method：Telcordia SR-332, Reliability Prediction of Electronic Equipment.
Operational Temperature(Ta) of test environment :30℃
Temperature(Tc) of Device when evaluation: 45℃

5. SD CARD COMPARISON

Table 5-1 Comparing SD6.X Standard, SD6.0 SDHC and SD6.0 SDXC

	SD6.10 Standard	SD6.10 SDHC	SD6.10 SDXC
Addressing Mode	Byte (1 byte unit)	Block (512 byte unit)	Block (512 byte unit)
HCS/CCS bits of ACMD41	Support	Support	Support
CMD8 (SEND_IF_COND)	Support	Support	Support
CMD16 (SET_BLOCKLEN)	Support	Support (Only CMD42)	Support (Only CMD42)
Partial Read	Support	Not Support	Not Support
Lock/Unlock Function	Mandatory	Mandatory	Mandatory
Write Protect Groups	Optional	Not Support	Not Support
Supply Voltage 2.0v – 2.7v (for initialization)	Not Support	Not Support	Not Support
Total Bus Capacitance for each signal line	40pF	40pF	40pF
CSD Version (CSD_STRUCTURE Value)	1.0 (0x0)	2.0 (0x1)	2.0 (0x1)
Speed Class	Optional	Mandatory (Class 2 / 4 / 6 / 10)	Mandatory (Class 2 / 4 / 6 / 10)

6. ELECTRICAL SPECIFICATIONS

6.1. Electrical Specifications

Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit
1	T_a	Operating Temperature	-40	+85	℃
2	T_{st}	Storage Temperature	-40	+85	℃

Parameter	Symbol	Min	MAX	Unit
Operating Temperature	T_a	-40	+85	℃
V_{DD} Voltage	V_{DD}	2.7	3.6	V

6.2. DC Characteristic

6.2.1. Bus Operation Conditions for 3.3V Signaling

Table 6-1 Threshold Level for High Voltage Range

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75*V_{DD}		V	I_{OH}=-2mA V_{DD} Min
Output Low Voltage	V_{OL}		0.125*V_{DD}	V	I_{OL}=2mA V_{DD} Min
Input High Voltage	V_{IH}	0.625*V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.25*V_{DD}	V	
Power Up Time			250	ms	From 0V to V_{DD} min

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4	-	V	I_{OH}=-2mA
Output Low Voltage	V_{OL}	-	0.45	V	I_{OL}=2mA
Input High Voltage	V_{IH}	1.27	2.00	V	
Input Low Voltage	V_{IL}	V_{ss}-0.3	0.58	V	

Parameter	Symbol	Min	Max.	Unit	Remarks
Input Leakage Current		-2	2	uA	DAT3 pull-up is disconnected.

Table 6-2 Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max.	Unit	Remarks
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

6.2.2. Bus Signal Line Levels

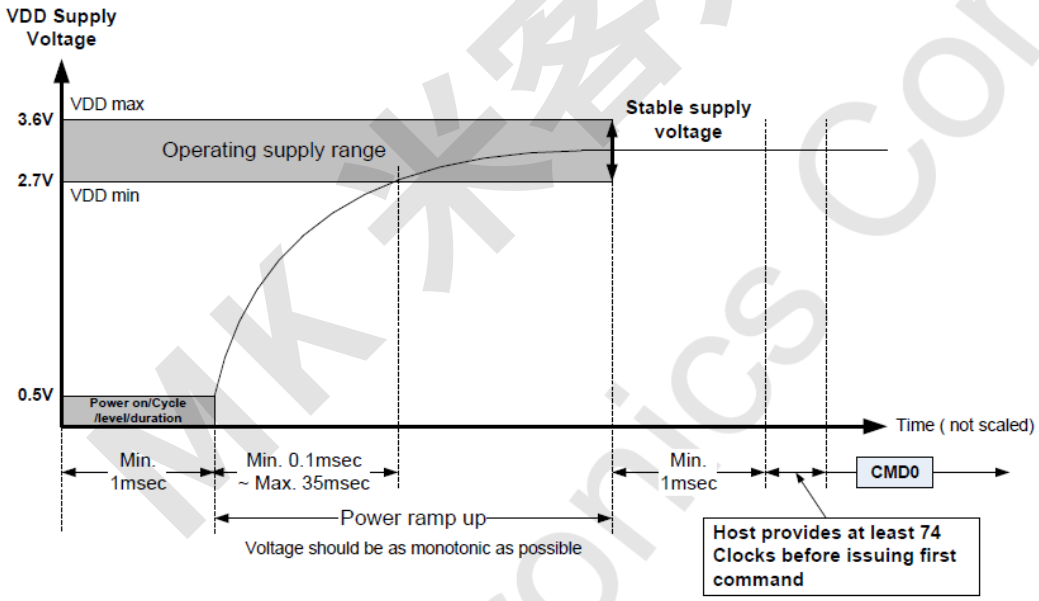
Bus Operation Conditions – Signal Line's Load

Total Bus Capacitance = C_{HOST} + C_{BUS} + N C_{CARD}

Parameter	symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card C_{HOST}+C_{BUS} shall not exceed 30 pF
Card Capacitance for each signal pin	C_{CARD}		10[1]	pF	
Maximum signal line inductance			16	nH	
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	kΩ	May be used for card detection
Capacity Connected to Power Line	C_C		5	uF	To prevent inrush current

6.2.3. Power Up Time of Host

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.



Power On or Power Cycle

Followings are requirements for Power on and Power cycle to assure a reliable SD Card hard reset.

(1) Voltage level shall be below 0.5V

(2) Duration shall be at least 1ms.

Power Supply Ramp Up

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD (min.) and VDD (max.) and host can supply SDCLK.

Followings are recommendation of Power ramp up:

(1) Voltage of power ramp up should be monotonic as much as possible.

(2) The minimum ramp up time should be 0.1ms.
(3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.
(4) Host shall wait until VDD is stable.
(5) After 1ms VDD stable time, host provides at least 74 clocks before issuing the first command.

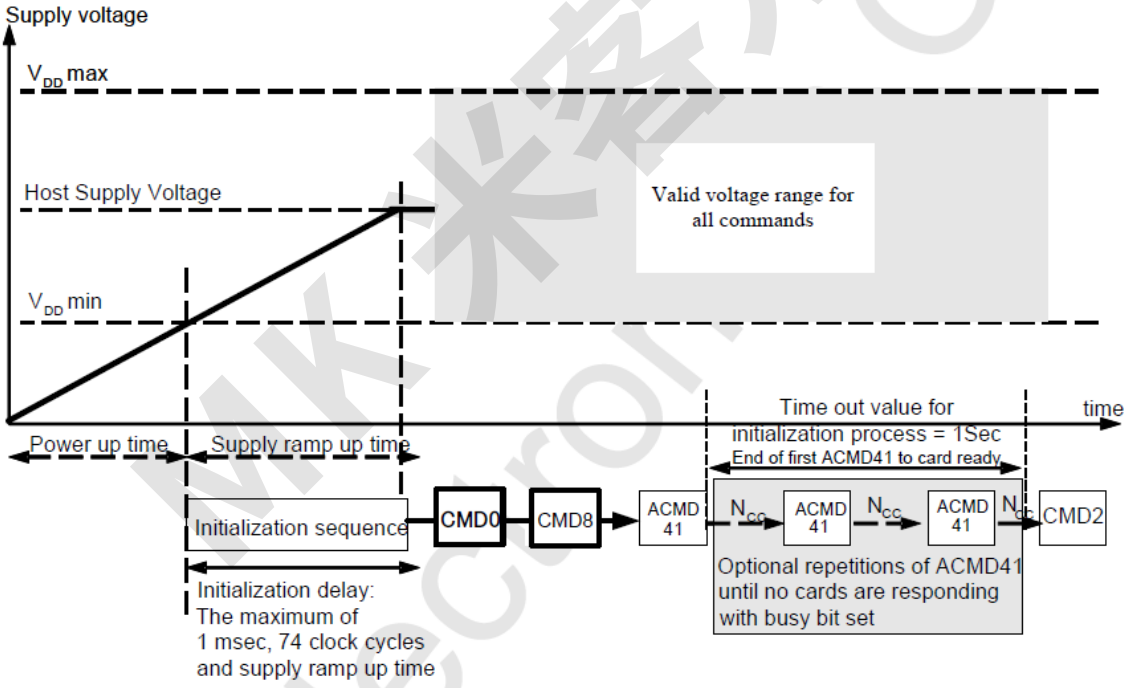
Power Down and Power Cycle

• When the host shuts down the power, the card VDD shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.

• If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in *Inactive State*. To create a power cycle, the host shall follow the power down description before power up the card (i.e. the card VDD shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

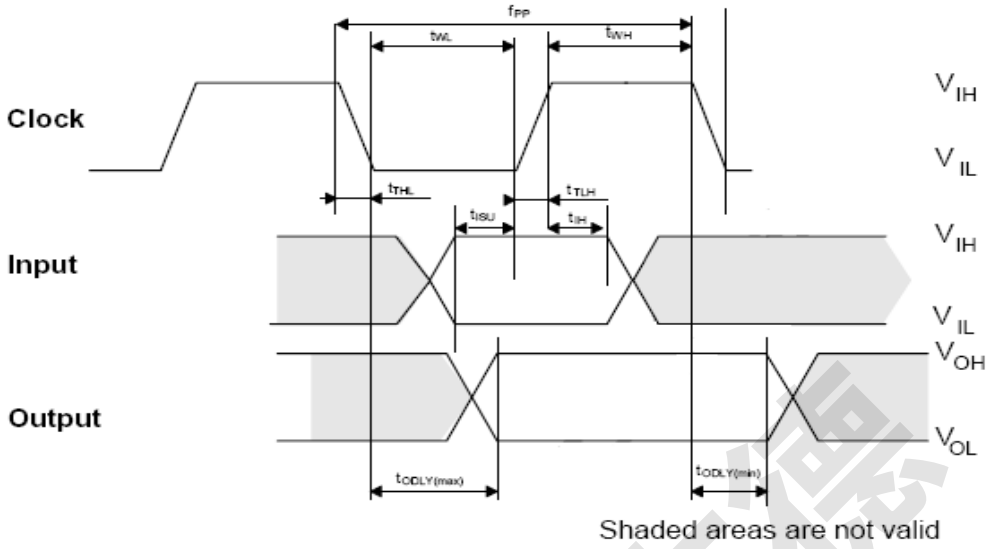
6.2.4. Power Up Time of Card

A device shall be ready to accept the first command within 1ms from detecting VDD min. Device may use up to 74 clocks for preparation before receiving the first command.



6.3. AC Characteristic

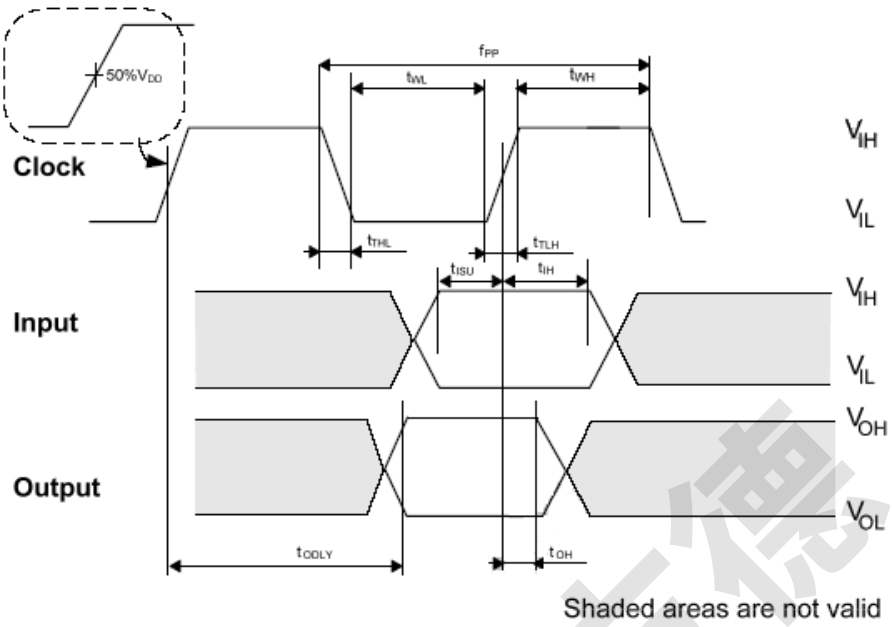
6.3.1. microSD Interface timing (Default)



Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{card}≤10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	$0_{(1)}$/100	400	kHz	C_{card}≤10 pF (1 card)
Clock low time	t_{WL}	10		ns	C_{card}≤10 pF (1 card)
Clock high time	t_{WH}	10		ns	C_{card}≤10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{card}≤10 pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{card}≤10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{card}≤10 pF (1 card)
Input hold time	t_{IH}	5		ns	C_{card}≤10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L≤40 pF (1 card)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	C_L≤40 pF (1 card)

(1) 0Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

6.3.2. microSD Interface Timing (High-Speed Mode)

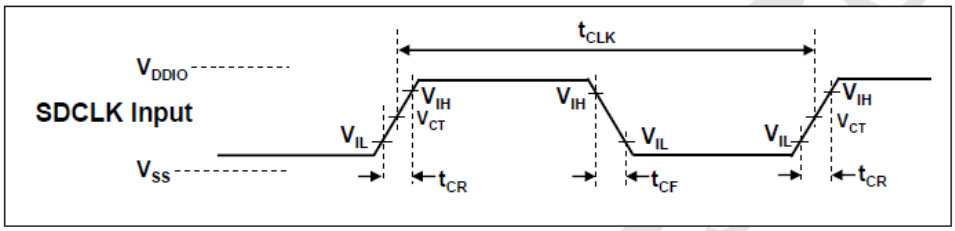


Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{card} ≤ 10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{card} ≤ 10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{card} ≤ 10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{card} ≤ 10 pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{card} ≤ 10 pF (1 card)
Input hold time	t_{IH}	2		ns	C_{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	C_L ≤ 40 pF (1 card)
Output Hold time	T_{OH}	2.5		ns	C_L ≤ 15 pF (1 card)
Total System capacitance of each line[1]	C_L		40	pF	CL ≤ 15 pF (1 card)

(1) In order to satisfy severe timing, the host shall drive only one card.

6.3.3. microSD Interface timing (SDR12, SDR25, SDR50 and SDR 104 Modes)

Input:

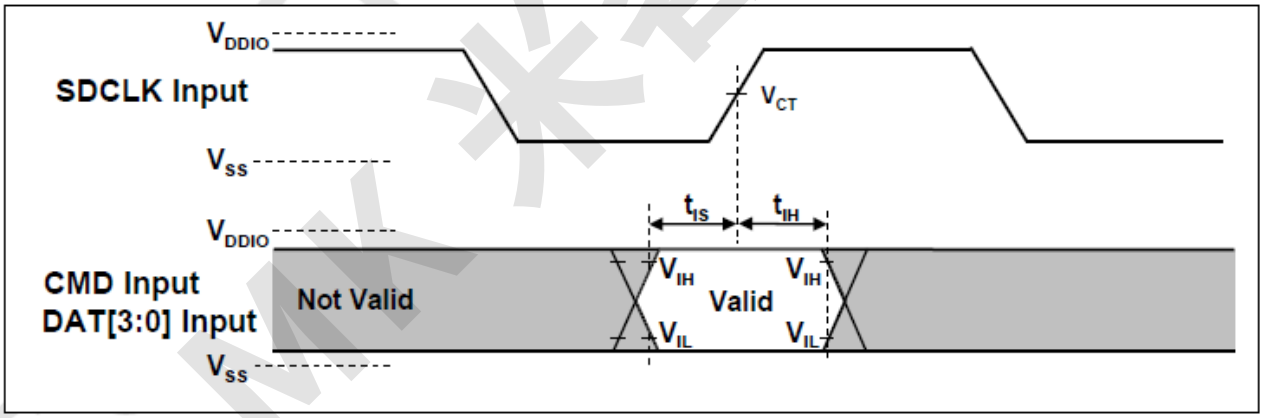


Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max.), Between rising edge, V_{CT}= 0.975V
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency
Clock Duty	30	70	%	

Clock Signal Timing

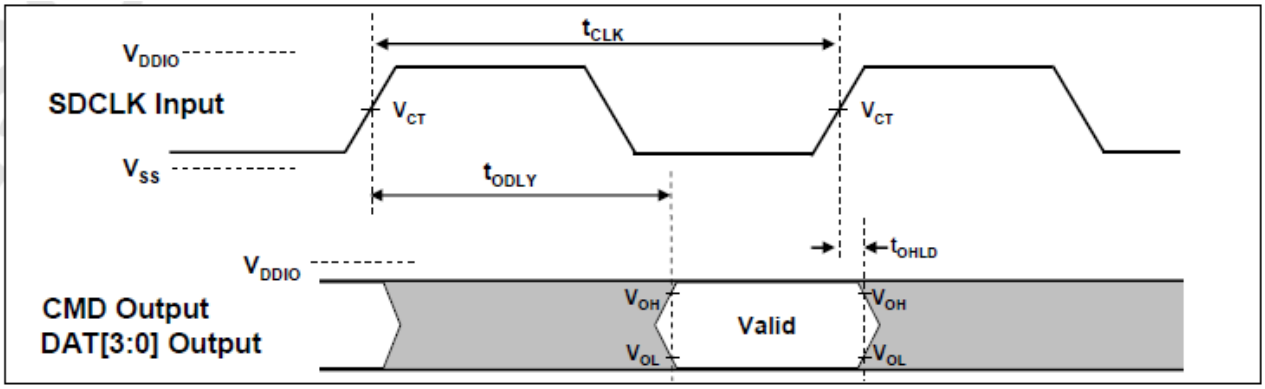
SDR50 and SDR104 Input Timing:



Card Input Timing

Symbol	Min	Max	Unit	SDR104 Mode
t_{IS}	1.40	-	ns	C_{CARD} =10pF, V_{CT}= 0.975V
t_{IH}	0.8[1]	-	ns	C_{CARD} = 5pF, V_{CT}= 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR50 Mode**
t_{IS}	3.00	-	ns	C_{CARD} =10pF, V_{CT}= 0.975V
t_{IH}	0.8[1]	-	ns	C_{CARD} = 5pF, V_{CT}= 0.975V

Output:

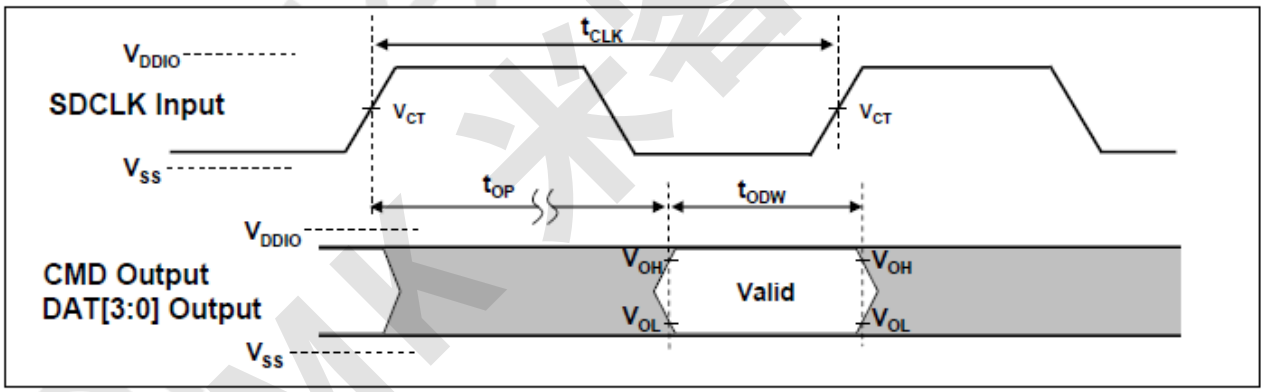


Output Timing of Fixed Data Window

Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK}>=10.0ns, C_L=30pF, using driver Type B, for SDR50
t_{ODLY}	-	14	ns	t_{CLK}>=20.0ns, C_L=40pF, using driver Type B, for SDR25 and SDR12,
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.), C_L=15pF

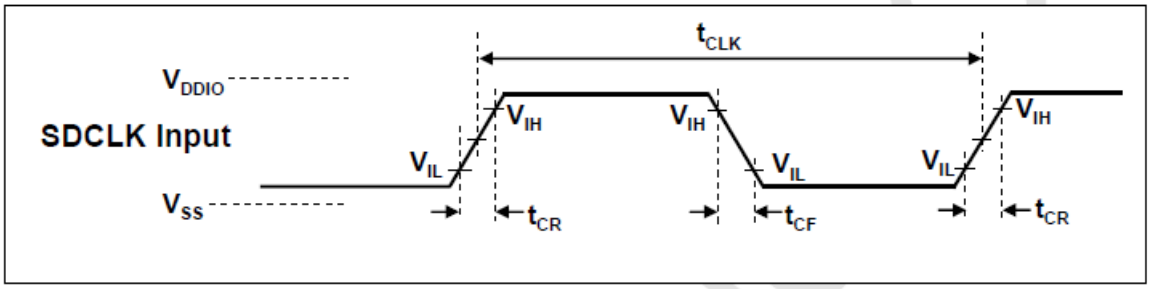
Output Timing of Fixed Data Window

Output (SDR104 mode):



Symbol	Min	Max	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
$\triangle t_{OP}$	-350	+1550	ps	Delay variable due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

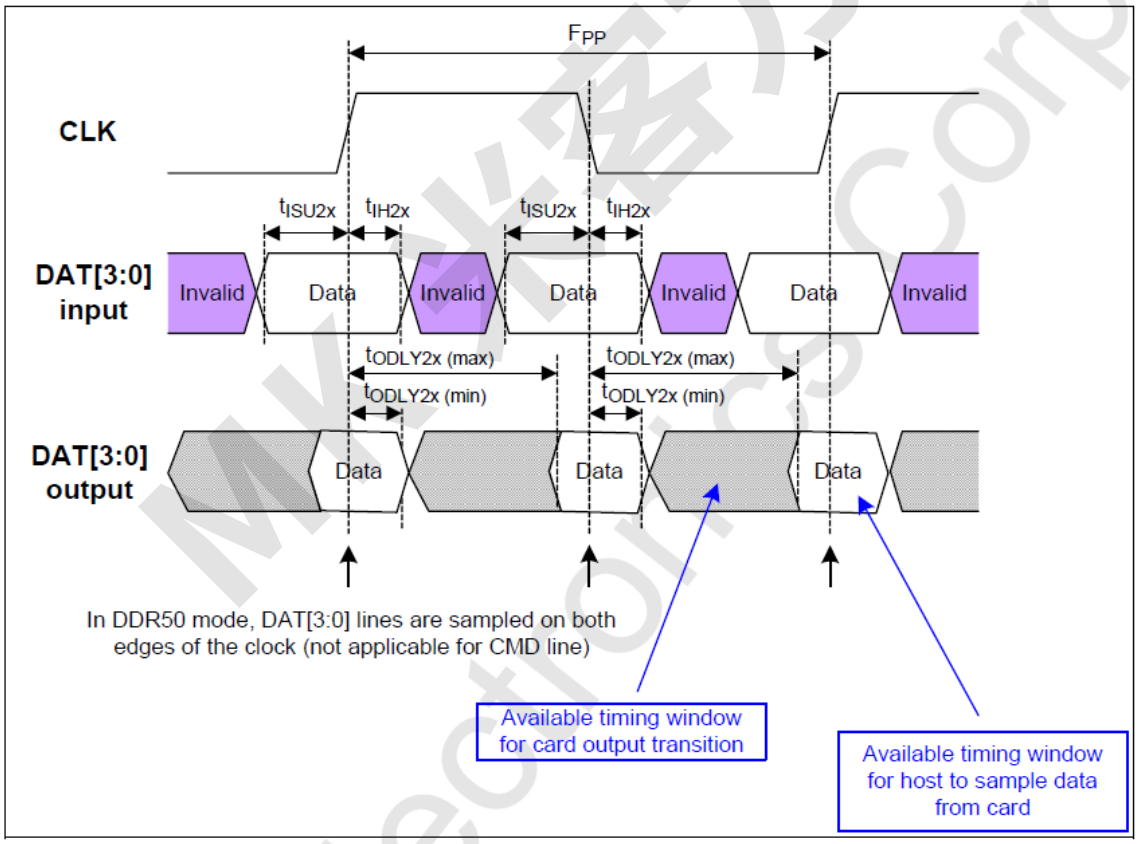
6.3.4. microSD Interface timing (DDR50 Modes)



Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, C_{CARD}=10pF
Clock Duty	45	55	%	

Clock Signal Timing



Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	3	-	ns	C_{card}≤10 pF (1 card)

Input hold time	t_{IH}	0.8	-	ns	C_{card}≤10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	C_L≤30 pF (1 card)
Output Hold time	T_{OH}	1.5	-	ns	C_L≥15 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	C_{card}≤10 pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{card}≤10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	C_L≤25 pF (1 card)
Output Hold time	T_{OH2x}	1.5	-	ns	C_L≥15 pF (1 card)

Bus Timings – Parameters Values (DDR50 mode)

7.1. Efficient Data Writing to SD Memory Card

In order to optimize sequential writing performance and WAF (Write Amplification Factor), it is recommended to use allocation unit (AU) writing.

It is recommended that Multiple_Block_Write shall be used as a command for writing data, and the size of data written by each command should be the FAT cluster x n (n: integer)

7.1.1. Write_Single_Block and Write_Multiple_Block

Write single block (CMD24) was written by one sector (512Bytes), which is suitable to write small area such like updating file system area (FAT). Besides, Write multiple blocks (CMD25) is a command for writing data to blocks that have sequential address per command, which is suitable to write large area such as user data. Write multiple blocks with a cluster unit (512Byte x 128 Sectors = 64KByte) in the file system is an efficient access to the flash memory, it is obviously to provide higher speed to compared to single write block.

And it could be estimated that SD card internal process would be reduced to save power consumption and flash write amplification factor, that is why the efficient data writing was recommended. To avoid the command issued by 512Bytes with single write block, software processes in the host device become faster.

For this operation, check the sectors in the SD card and file system as Figure 7-1

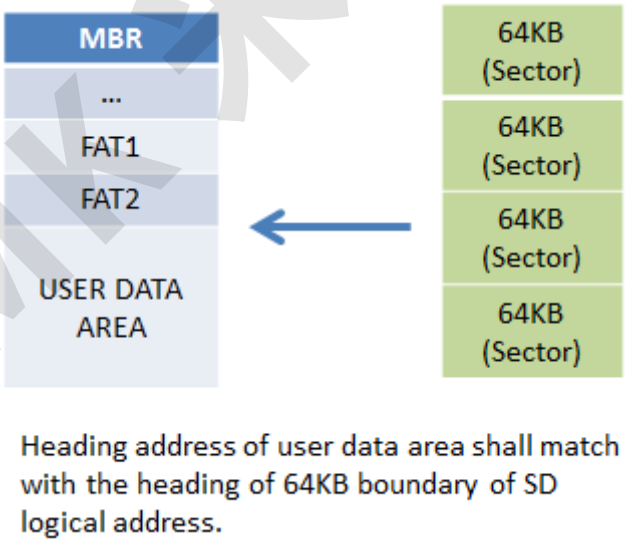


Figure 7-1 Matching between logical address and file system

Note: Large Cluster unit is better for performance and WAF, for example, 128KB, 256KB or 512KB. Large cluster unit also can save write command numbers and few transfer time.

7.2. Basic Process of Error Handling

7.2.1. Retry Process

Execute the process by sending commands again, especially for signal issue between card and host.

7.2.2. Recovery Process

Confirm card status is in Transfer State, if card status is not in Transfer State, please issue Stop command to recover it and execute or continue flow. If there was UECC during read/write status, we could use recovery process to recover it.

7.2.3. Tuning Write Command Process

In order to adjust Host CMD and CLK timing, the way is issue tuning command to confirm what the device response and data was received by host. Based on the response, host was adjusting the timing step by step and recording the pass range. Through this flow host could adjust the appropriate timing settings to avoid unexpected handshaking issue.

7.2.4. Tuning Read Command Process

In order to adjust Host CLK and DAT timing, the way is issue tuning command to confirm what the device response and data was received by host. Based on the response, host was adjusting the timing step by step and recording the pass range. Through this flow host could adjust the appropriate timing settings to avoid unexpected handshaking issue.

7.2.5. Exception Handling Process

No doubt that sometimes we would face all error handling above could not recover it successfully, and we could react based on the situation.

- If there was error in response, we could re-initialize the card.
- If it was signal issue, we could set up signal status by reading data and tuning command.

7.3. Common Error Handling in SPI and SD mode

7.3.1. Time-out

Run the Retry Process. No response from CMD, it might be signal or status got problem. To avoid the infinite loop, implement a retry counter in the host so that, if the retry counter expires, the exception handling starts in the host.

7.3.2. Error Detect (CMD CRC Error)

Run the Recovery Process. If it got second time failure with CRC, the setting might be too margin to receive response stably. Suggestion is use tuning write command to fix timing and then retry it.

7.3.3. Error Detect (Other Error) in SPI and SD mode

Run the Recovery Process.

7.3.4. Others

Most errors could be recovered by running the Recovery Process, let card come into Transfer State and then

executing the flow we planned. If it does not work, please use exception method to come back initial state.

7.4. Data Error Handling in SPI and SD mode

7.4.1. Time-out

Run the Recovery Process. While the state was recovered, run the flow again.

7.4.2. Read CRC16 Error

Run the Recovery Process. If it got second time failure with CRC, the setting might be too margin to receive data stably. Suggestion is use tuning read date to fix timing and then retry it.

7.4.3. Write CRC Status Error

Run the Recovery Process. If it got second time failure with CRC, the setting might be too margin to receive CRC status stably. Suggestion is use tuning read date to fix timing and then retry it.

7.4.4. Others

Most errors could be recovered by running the Recovery Process, let card come into Transfer State and then executing the flow we planned.

7.5. Multiple Block Write (CMD25) Process

- If Response is ADDRESS_OUT_OF_RANGE, please confirm writing address.
- If Response is DEVICE_IS_LOCKED, please stop writing data.
- If Response is COM_CRC_ERROR, run retry or tuning.

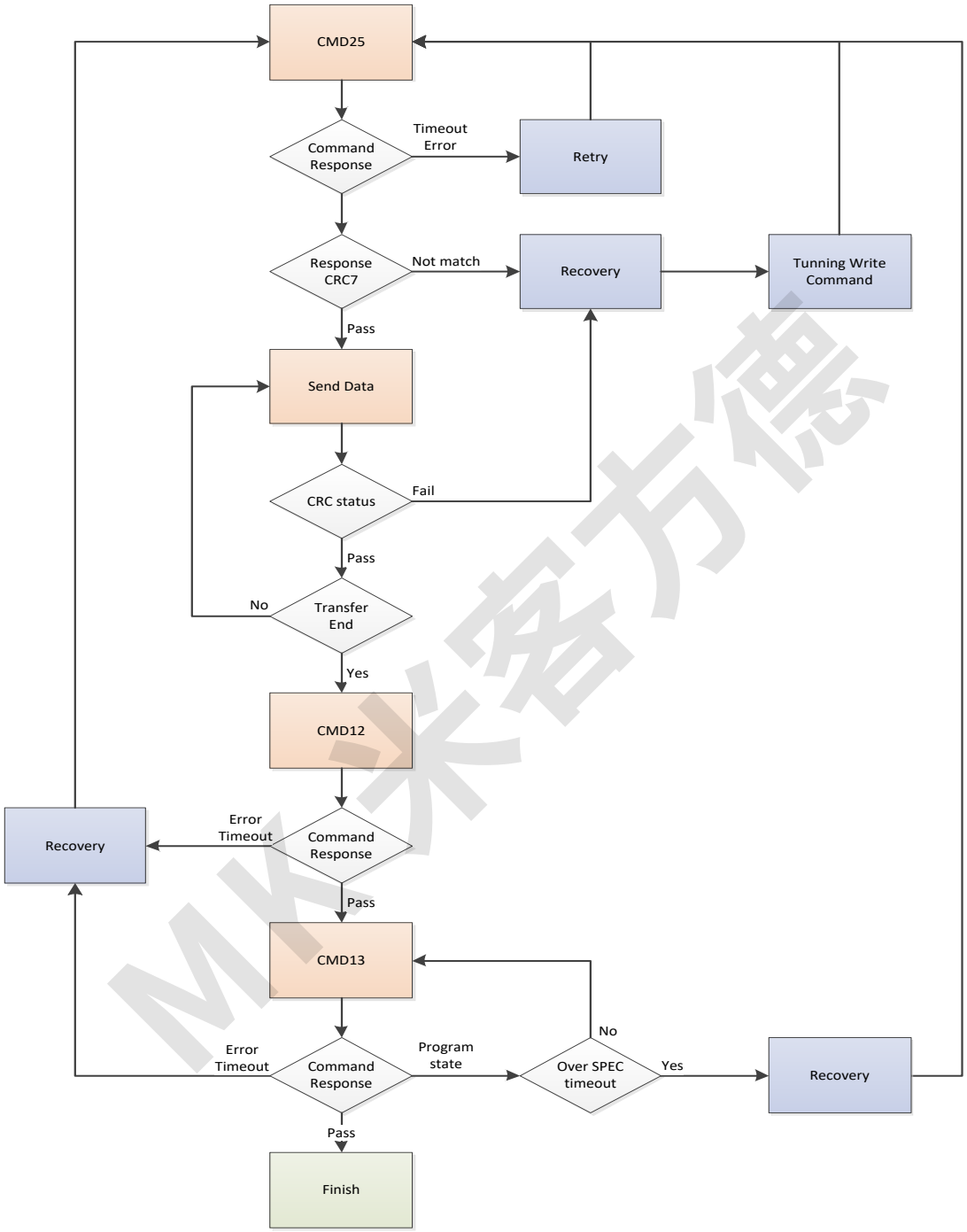


Figure 7-2 Multiple Write (CMD25) Error Handling

7.6. Retry Error handling

In order to avoid signal issue caused unexpected response from device, we could use Retry Process to fix it.

- Please make sure card state is in transfer state before issuing following commands.
- To avoid the infinite loop, implement a retry counter in the host.
- If the device could not respond to CMD13 normally, please run exception handling to recover card status.

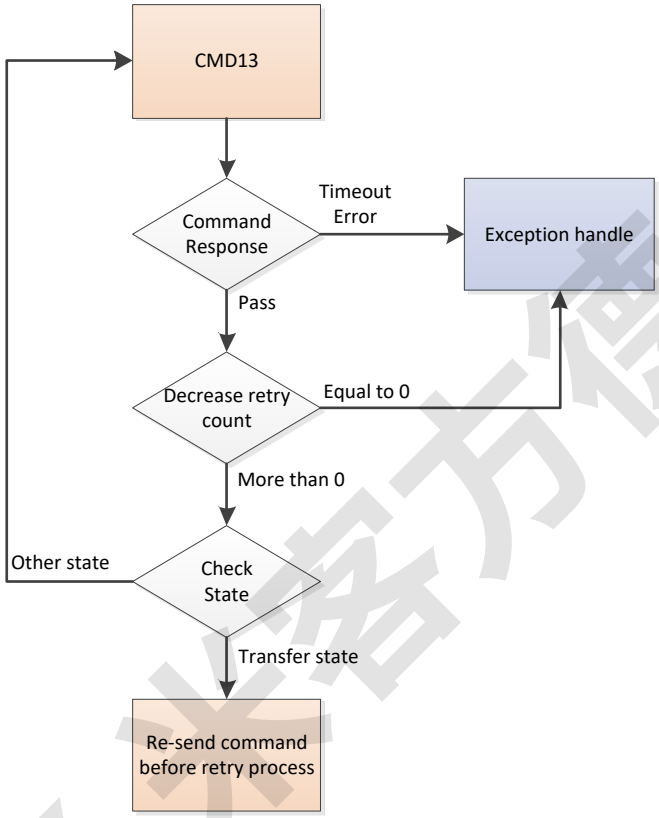


Figure 7-3 Retry Error Handling Process

7.7. Recovery Error Handling

Sometimes the device failure could not be recovered by Retry Process, it suggests to execute STOP Command (CMD12) to stop whole commands and response and then run following flow.

- Please confirm card status is in Transfer state
- In order to avoid infinite loops, host has to set up a retry counter number.

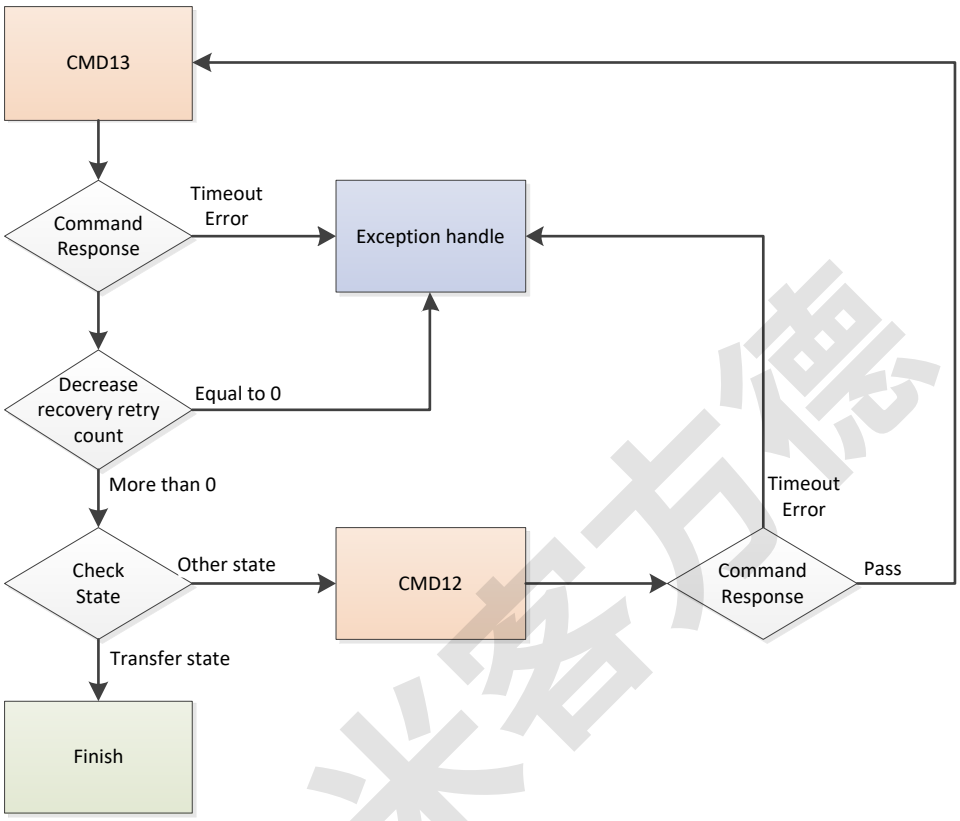


Figure 7-4 Recovery Error Handling Process

7.8. Tuning Write Command Error Handling

Reconfirm the card's pass range, to make sure card could receive host commands.

- If there was no any pass window, it might be connect issue or signal issue
- Pass Range depends on frequency level, higher frequency makes fewer pass range

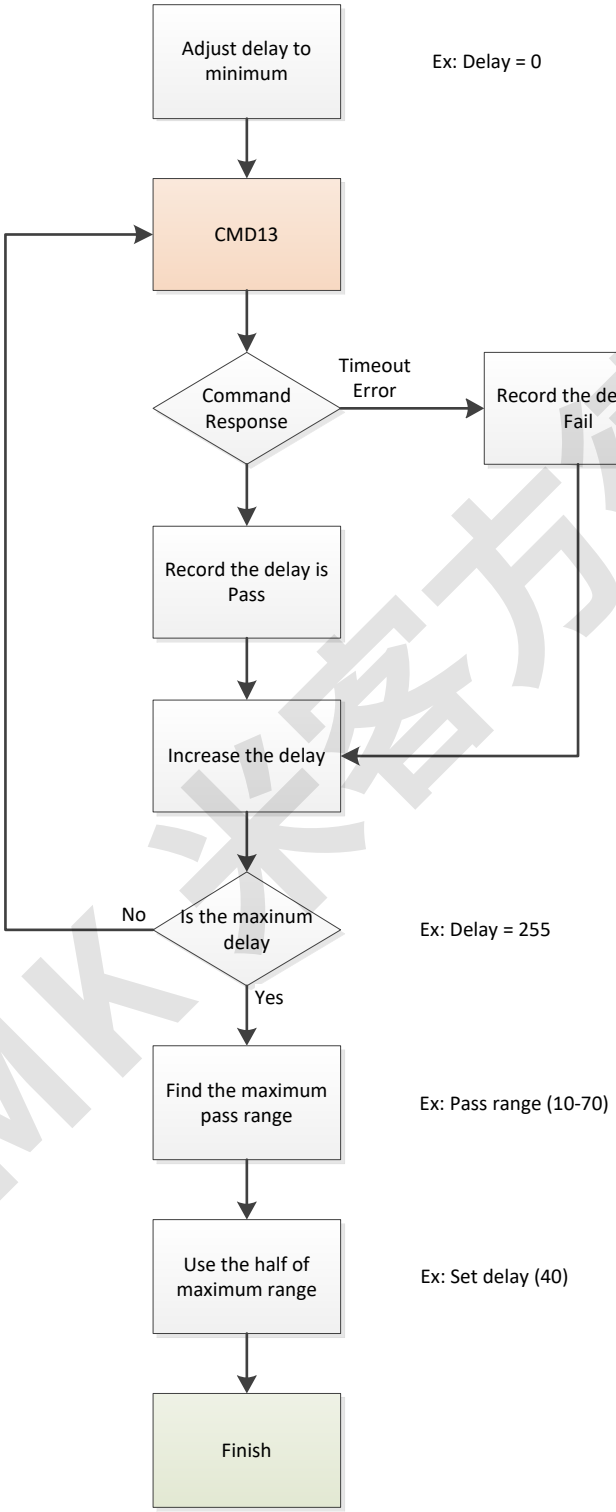


Figure 7-5 Tuning Write Command Error Handling Process

7.9. Exception Error Handling

- Error in Card's response or data output time-out, it could re-initialize the card.
- If there was CMD CRC7 issue, it could use tuning write command process to find out appropriate timing.
- If there was DAT CRC16 issue, it could use tuning read command process to find out appropriate timing.

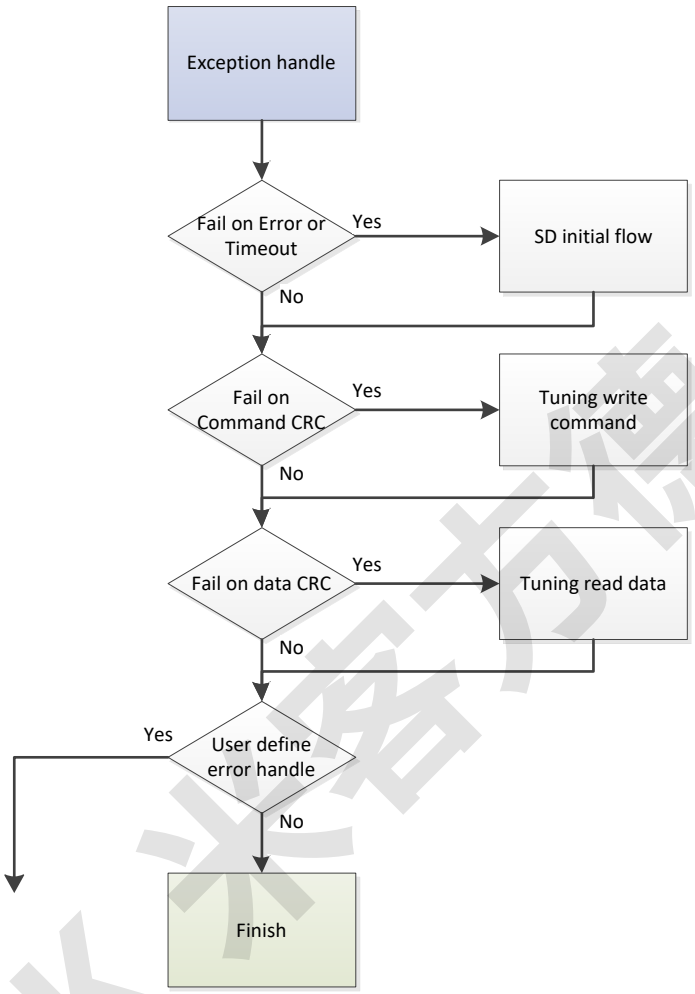


Figure 7-6 Exception Error Handling Process

7.10. Multiple Blocks Read (CMD18) Error Handling Process

- If card responded ADDRESS_OUT_OF_Range, please check writing address
- If card responded DEVICE_IS_LOCKED, please stop writing data
- If card responded COM_CRC_ERROR, run Retry or Tuning Process

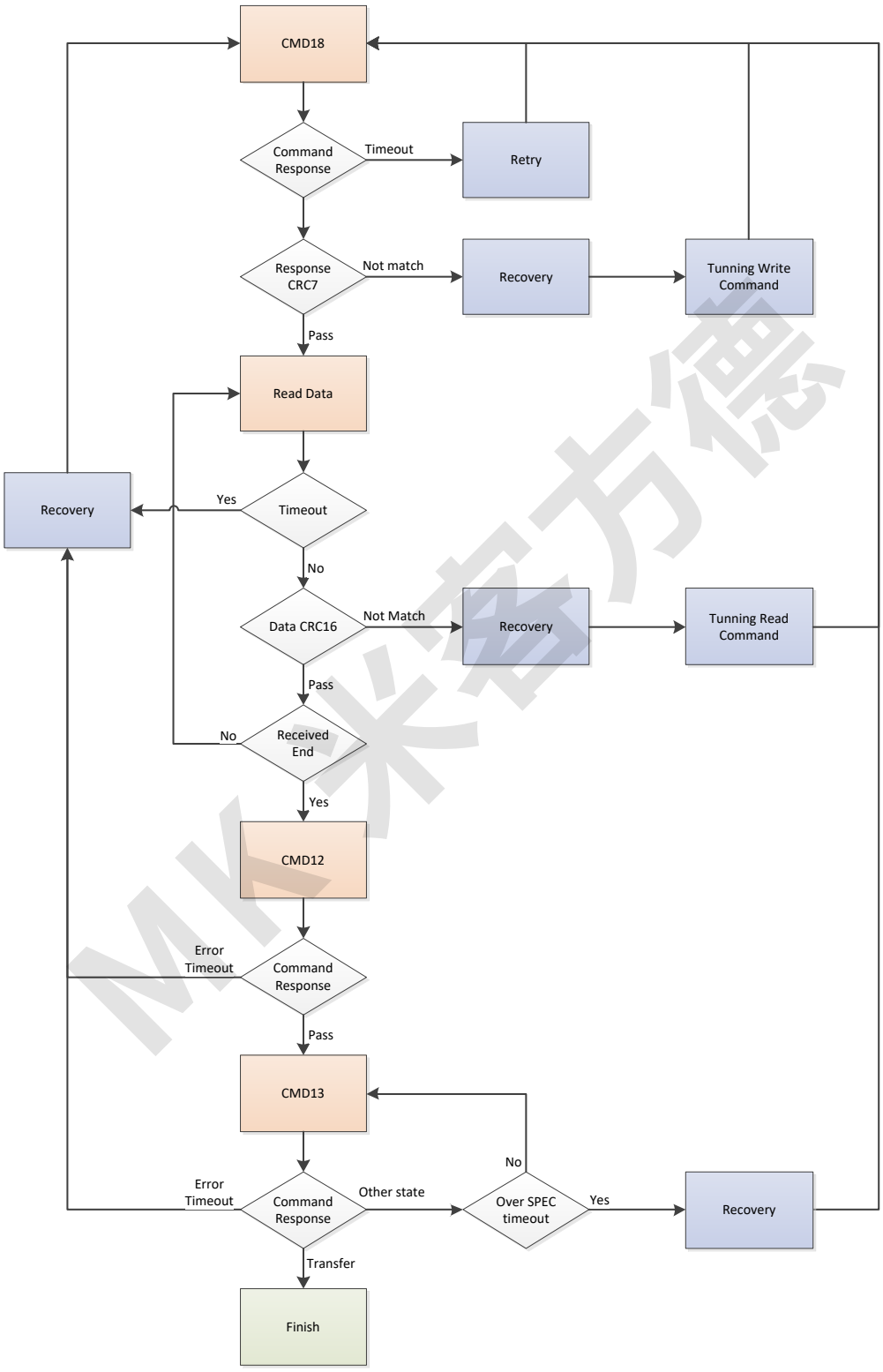


Figure 7-7 Multiple Blocks Read (CMD18) Error Handling Process

7.11. Tuning Read Data Error Handling

Reconfirm the card's pass range, to make sure host could receive card's Response and Data.

- If there was no any pass window, it might be the connect issue or signal issue
- Pass Range depends on frequency level, higher frequency makes fewer pass range

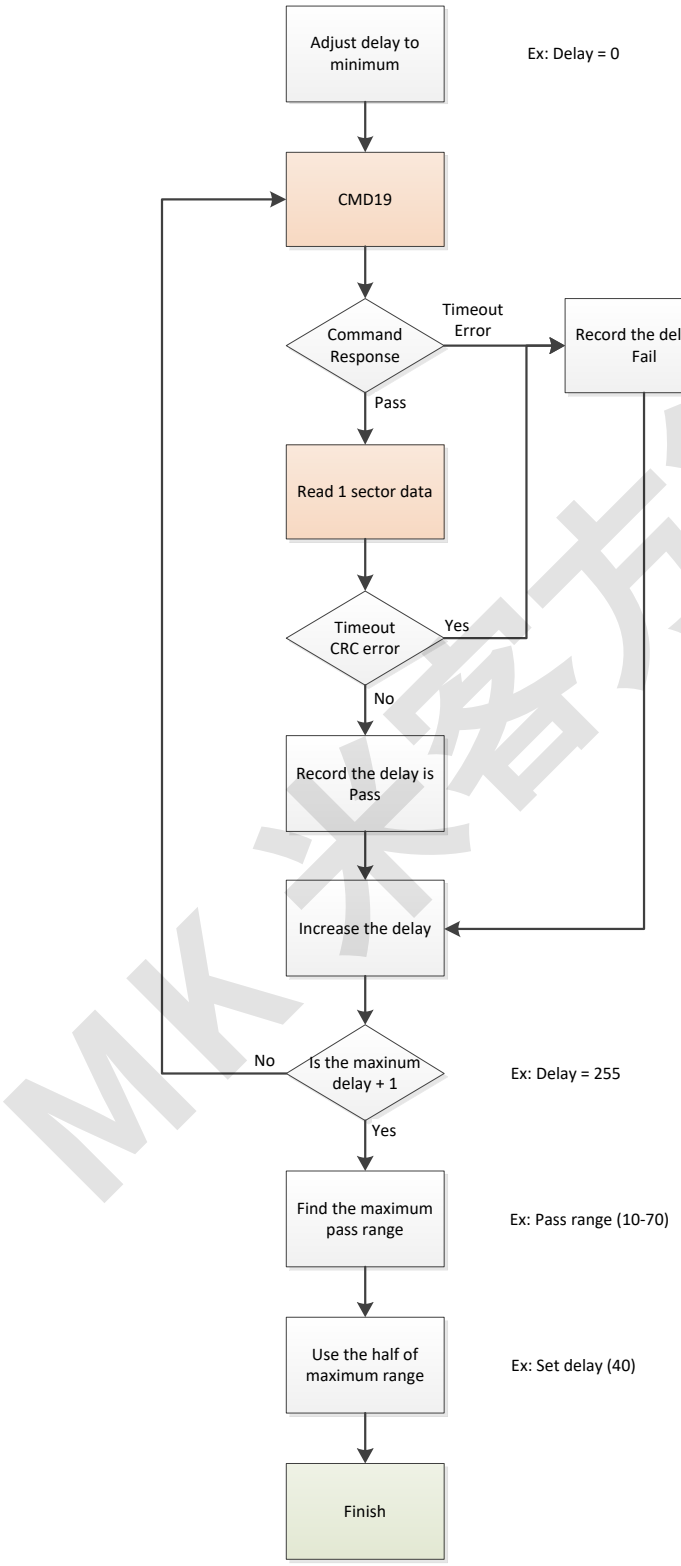
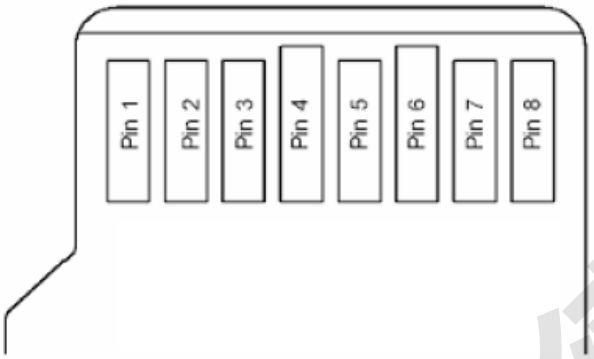


Figure 7-8 Tuning Read Data Error Handling Process

8. INTERFACE

8.1. Pad Assignment and Descriptions



pin	SD Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type	Description
1	DAT2	I/O/PP	Data Line[bit2]	RSV		
2	CD/DAT3 [2]	I/O/PP [3]	Card Detect/ Data Line[bit3]	CS	I [3]	Chip Select (neg true)
3	CMD	PP	Command/Response	DI	I	Data In
4	V_{DD}	S	Supply voltage	V_{DD}	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS}	S	Supply voltage ground	V_{SS}	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line[bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line[bit1]	RSV		

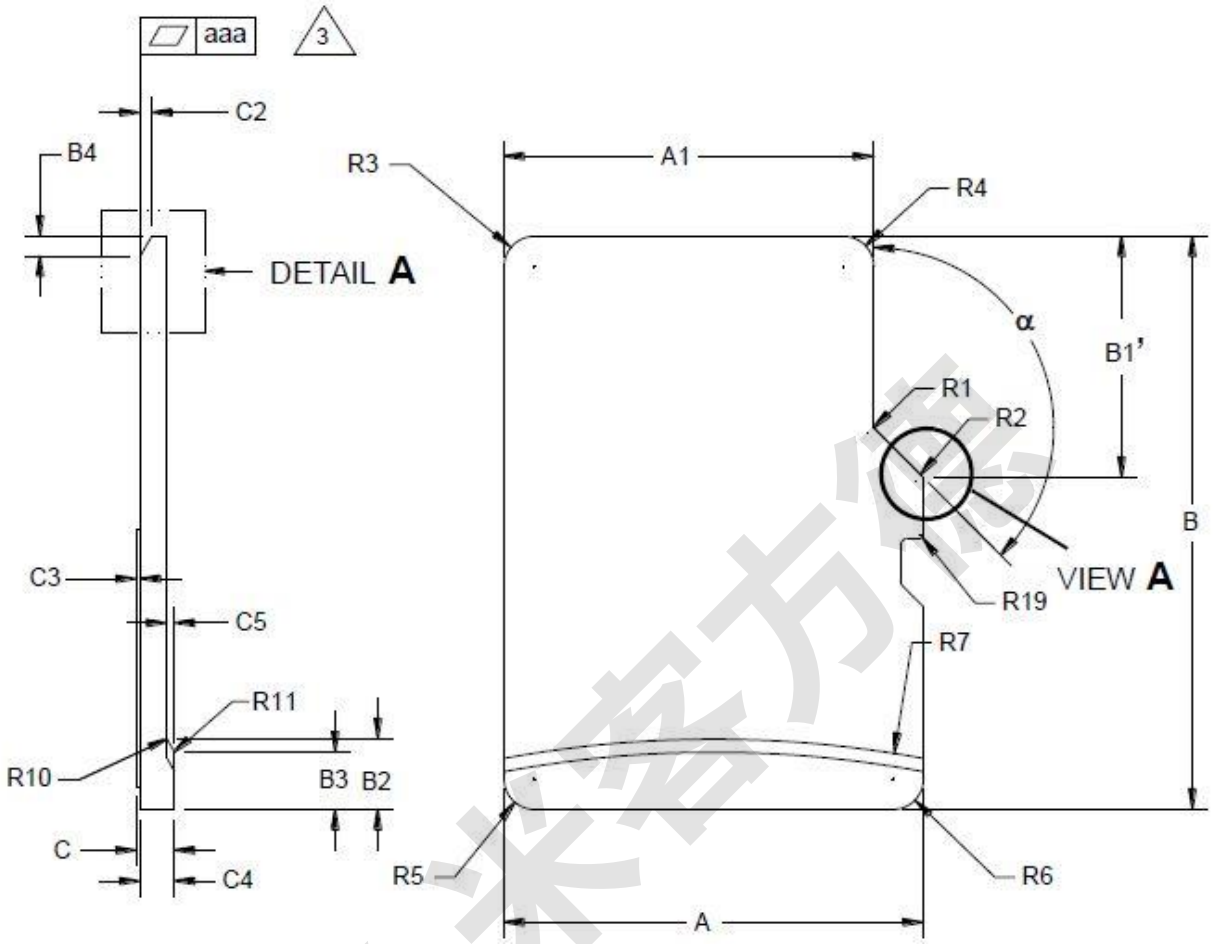
(1) S: power supply, I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers

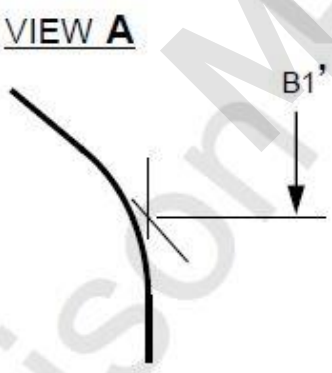
(2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMedia Cards.

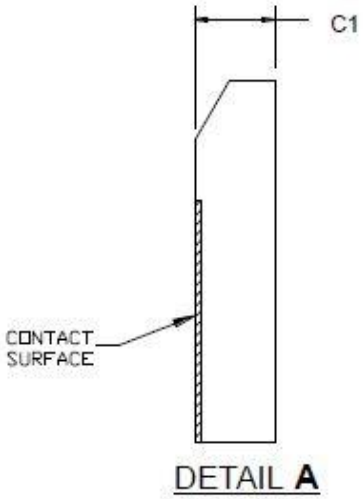
(3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer period, with SET_CLR_CARD_DETECT (ACMD42) command.

Name	Width	Description
CID	128bit	Card identification number; card individual number for identification. **Mandatory**
RCA[1]	16bit	Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization. **Mandatory**
DSR	16bit	Driver Stage Register; to configure the card's output drivers. **Optional**
CSD	128bit	Card Specific Data; information about the card operation conditions. **Mandatory**
SCR	64bit	SD Configuration Register; information about the SD Memory Card's Special Features capabilities **Mandatory**
OCR	32bit	Operation conditions register. **Mandatory.**
SSR	512bit	SD Status; information about the card proprietary features **Mandatory**
OCR	32bit	Card Status; information about the card status **Mandatory**

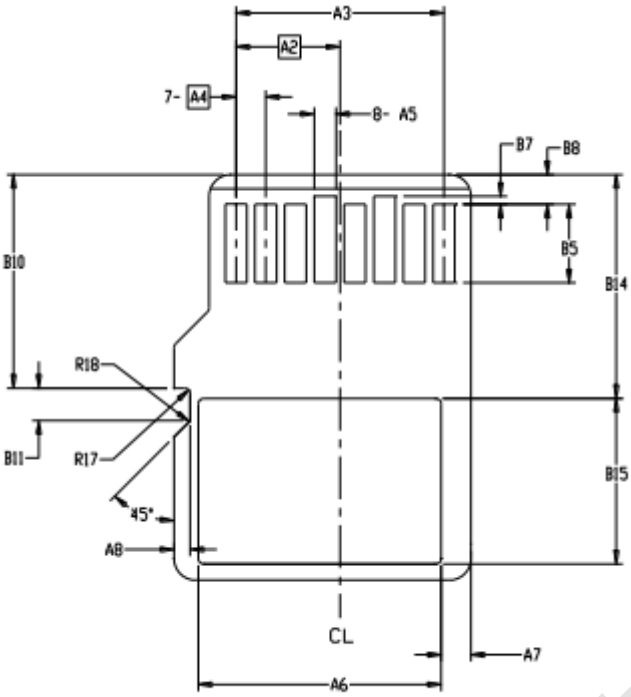
9. PHYSICAL DIMENSION







As measurement point is changed like as VIEW A, symbol B1 is changed to symbol B1'. There is no modification in mechanical dimension.



Type A

	COMMON DIMENSION			
SYMBOL	MIN	NOM	MAX	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
A10	1.35	1.40	1.45	
A11	6.50	6.60	6.70	
A12	0.50	0.55	0.60	
A13	0.40	0.45	0.50	
A14	0.05	-	-	
A15	5.71	5.81	5.91	
A16	6.47	6.57	6.67	
A17	6.62	6.72	6.82	
A18	7.38	7.48	7.58	
A19	7.75	7.85	7.95	
A20	8.55	8.65	8.75	
A21	0.90	-	-	
A22	-	-	8.50	
B	14.90	15.00	15.10	
B1'	6.13	6.23	6.33	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
B12	3.60	3.70	3.80	
B13	2.80	2.90	3.00	
B14	8.20	-	-	
B15	-	-	6.20	
B16	5.80	5.90	6.00	
B17	0.20	0.30	0.40	
B18	7.80	8.80	8.90	
B19	8.70	8.80	8.90	
B20	-	3.20	-	REF
B21	1.90	2.00	2.10	
B22	9.00	-	-	
B23	0.10	-	-	

C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
C4	0.80	-	1.10	
C5	0.15	-	-	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.60	0.80	0.90	
R6	0.60	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20	④	-	0.15	
α	133°	135°	137°	
aaa	-	-	0.10	

Notes:

1. DIMENSIONING and TOLERANCING per ASME Y14.5M-1994.
2. Dimensions are in millimeters.
3. ③ COPLANARITY is additive to C1 MAX thickness.
4. ④ All edges shall not be sharp as tested per UL1439 "Test for Sharpness of Edges on Equipment."
5. Refer to Appendix E about test method of warpage.
6. As measurement point is changed, symbol B1 is changed to symbol B1'.
7. C4 and C5 are added from Version 4.00.