APM
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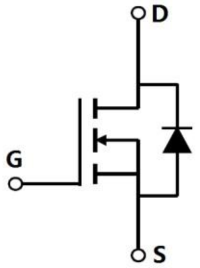
APG60N10S

100V N-SGT Enhancement Mode MOSFET

General Description

APG60N10S use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics.

This device is specially designed to get better ruggedness and suitable to use in



Features

Low RDS(on) & FOM

Extremely low switching loss

Excellent stability and uniformity or Invertors

Applications

Consumer electronic power supply

Motor control

Synchronous-rectification

Isolated DC

Synchronous-rectification applications

.

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
APG60N10S	SOP-8	APG60N10S XXX YYYY	3000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_A=25˚C	Continuous Drain Current[1]	60	A
I_D@T_A=70˚C	Continuous Drain Current[1]	42	A
I_{DM}	Pulsed Drain Current[2]	180	A
EAS	Single Pulse Avalanche Energy[3]	12	mJ
I_{AS}	Avalanche Current	9	A
P_D@T_A=25˚C	Total Power Dissipation[4]	100	W
T_{STG}	Storage Temperature Range	-55 to 150	˚C
T_J	Operating Junction Temperature Range	-55 to 150	˚C
$R_{θJA}$	Thermal Resistance Junction-Ambient [1](t≦10s)	40	˚C/W
$R_{θJA}$	Thermal Resistance Junction-Ambient [1]	75	˚C/W
$R_{θJC}$	Thermal Resistance Junction-Case[1]	24	˚C/W

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Electrical Characteristics (T_A=25℃unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	100	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=11.5A	---	8	12	mΩ
	Static Drain-Source On-Resistance[2]	V_{GS}=4.5V , I_D=9.5A	---	12	15.5	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	1.2	---	2.5	V
I_{DSS}	Drain-Source Leakage Current	V_{DS}=80V , V_{GS}=0V , T_J=25˚C	---	---	1	uA
		V_{DS}=80V , V_{GS}=0V , T_J=55˚C	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=5V , I_D=11.5A	---	45	---	S
Qg	Total Gate Charge (10V)	V_{DS}=50V , V_{GS}=10V , I_D=11.5A	---	35	---	nC
Qg	Total Gate Charge (4.5V)		---	16	---	
Qgs	Gate-Source Charge		---	8	---	
Qgd	Gate-Drain Charge		---	4	---	
Td(on)	Turn-On Delay Time	V_{DD}=50V , V_{GS}=10V , R_G=3 , I_D=11.5A	---	9	---	ns
Tr	Rise Time		---	4.5	---	
Td(off)	Turn-Off Delay Time		---	35	---	
Tf	Fall Time		---	5.5	---	
Ciss	Input Capacitance	V_{DS}=50V , V_{GS}=0V , f=1MHz	---	2550	---	pF
Coss	Output Capacitance		---	305	---	
Crss	Reverse Transfer Capacitance		---	12	---	
I_S	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	4	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=1A , T_J=25˚C	---	---	1.1	V
t_{rr}	Reverse Recovery Time	I_F=11.5A , di/dt=100A/μs , T_J=25˚C	---	28	---	nS
Q_{rr}	Reverse Recovery Charge		---	120	---	nC

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.3mH,I_{AS}=9A
4.The power dissipation is limited by 150˚C junction temperature
5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

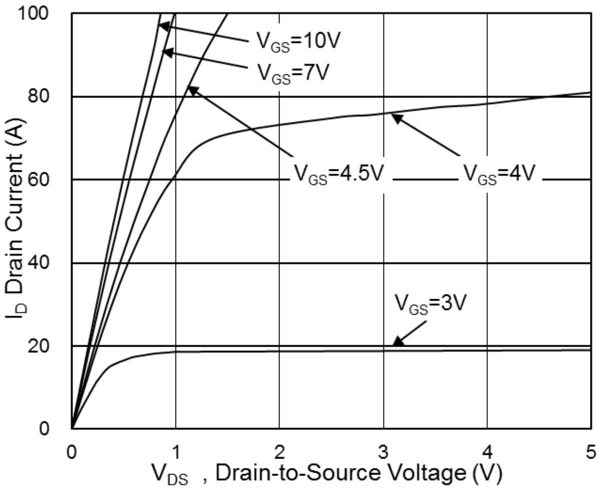


Fig.1 Typical Output Characteristics

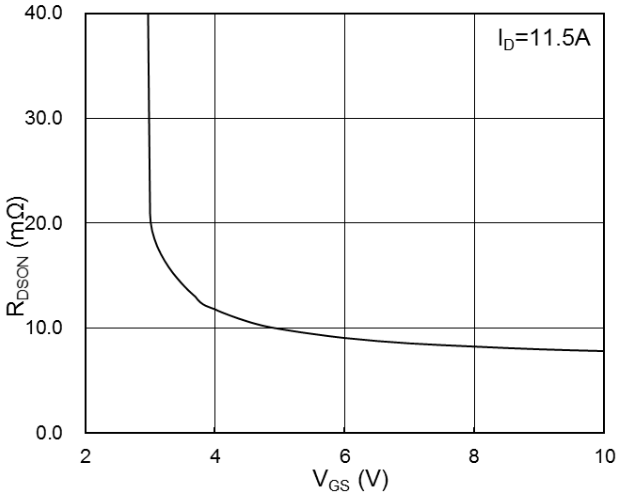


Fig.2 On-Resistance vs. G-S Voltage

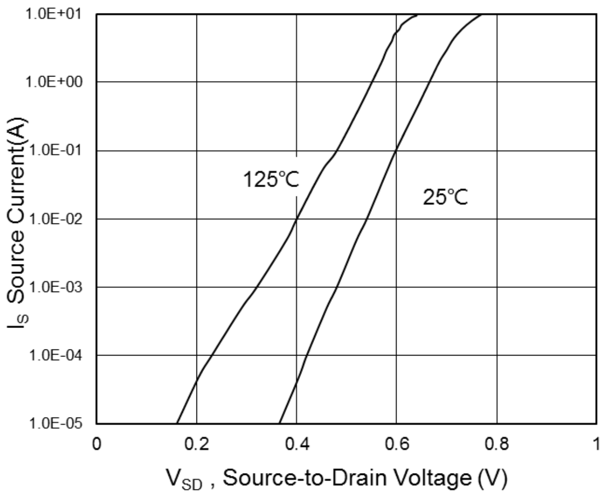


Fig.3 Source-Drain Forward Characteristics

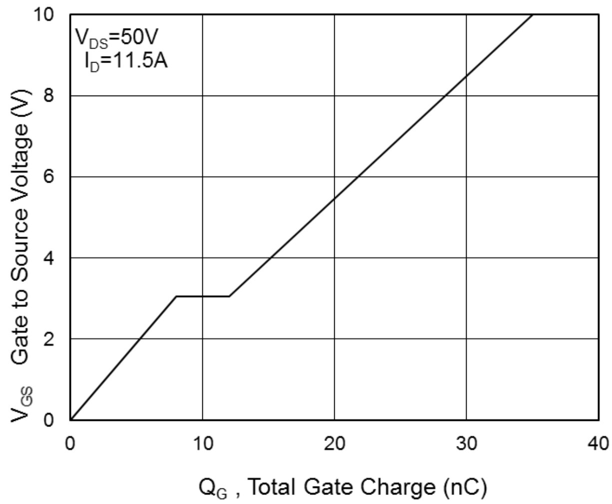


Fig.4 Gate-Charge Characteristics

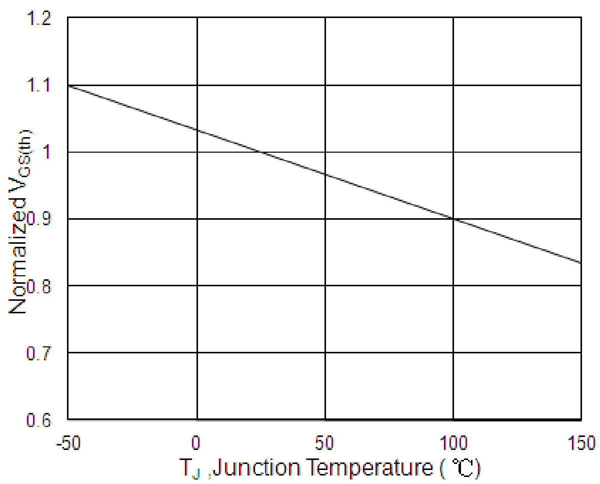


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

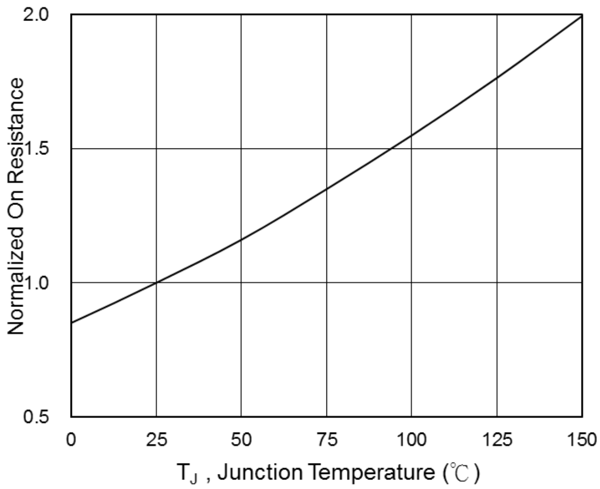


Fig.6 Normalized R_{DSON} vs. T_J

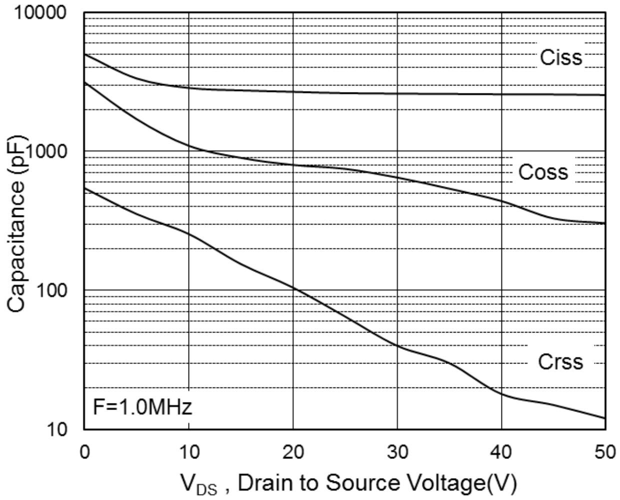


Fig.7 Capacitance

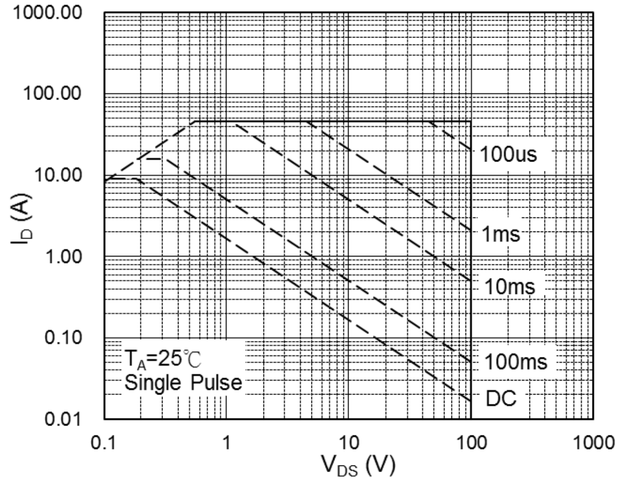


Fig.8 Safe Operating Area

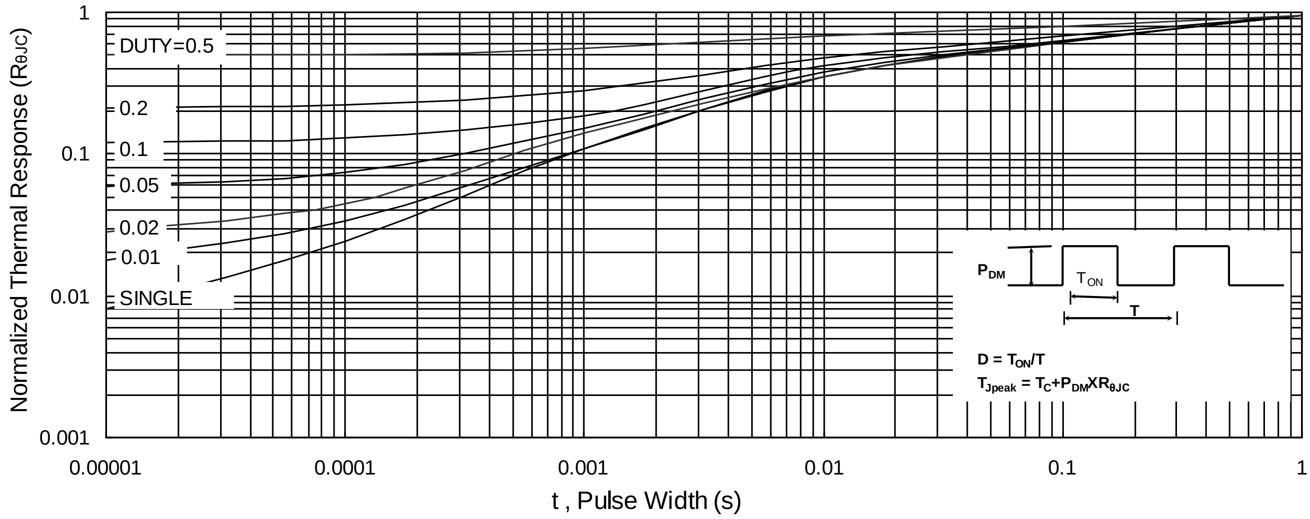


Fig.9 Normalized Maximum Transient Thermal Impedance

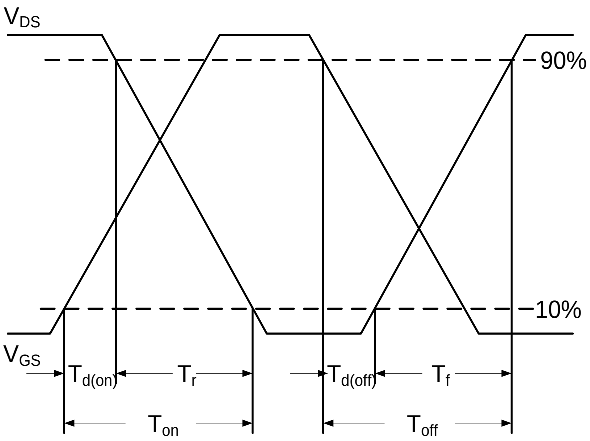


Fig.10 Switching Time Waveform

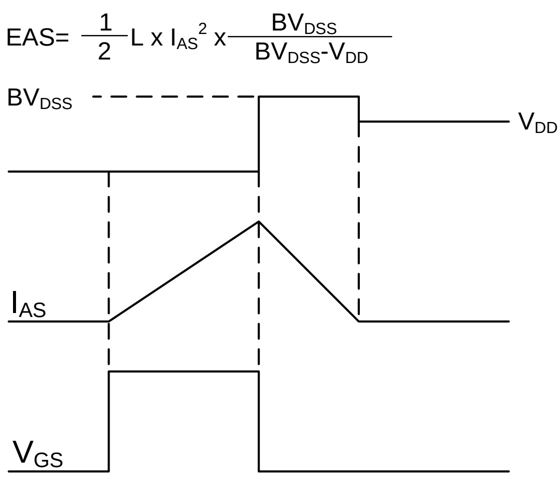
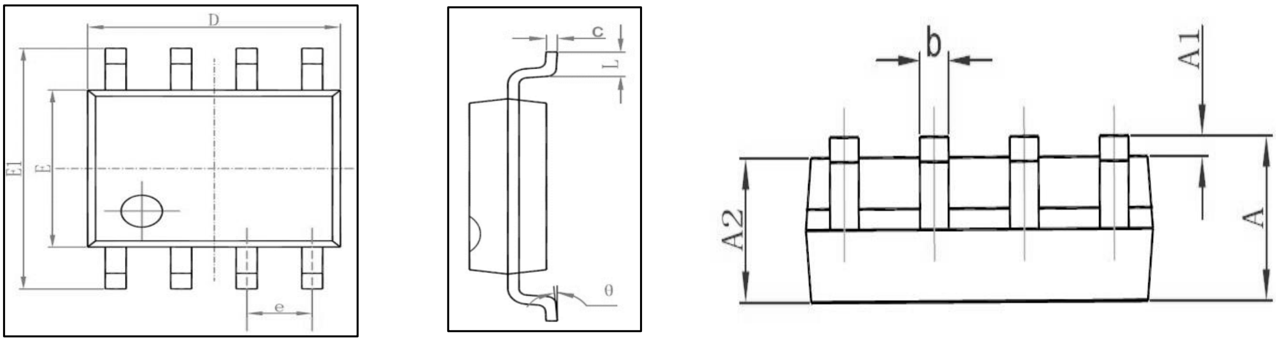
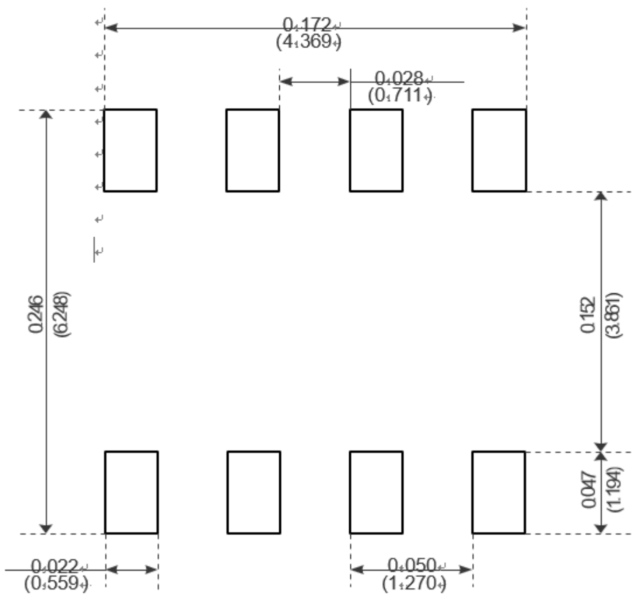


Fig.11 Unclamped Inductive Switching Waveform

Package Mechanical Data-SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads

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Edition	Date	Change
Rve1.0	2018/12/31	Initial release
Rve2.0	2019/5/31	Reduce Cisss and Rds