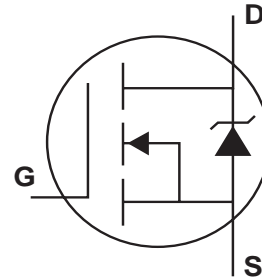


Description

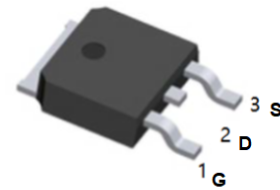
The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques.

Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



Features

- V_{DS} (V) = 100V
- I_D = 17A (V_{GS} = 10V)
- $R_{DS(ON)}$ = 105m Ω (V_{GS} = 10V)



TO-252(DPAK) top view

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	17	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	12	
I_{DM}	Pulsed Drain Current ①⑤	60	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	79	W
	Linear Derating Factor	0.53	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy②⑤	150	mJ
I_{AR}	Avalanche Current①⑤	9.0	A
E_{AR}	Repetitive Avalanche Energy①⑤	7.9	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.9	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) **	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.122	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	105	mΩ	V _{GS} = 10V, I _D = 10A ④
		—	—	125		V _{GS} = 5.0V, I _D = 10A ④
		—	—	155		V _{GS} = 4.0V, I _D = 9.0A ④
V _{GS(th)}	Gate Threshold Voltage	1.0	—	2.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	7.7	—	—	S	V _{DS} = 25V, I _D = 9.0A⑤
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 100V, V _{GS} = 0V
		—	—	250		V _{DS} = 80V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -16V
Q _g	Total Gate Charge	—	—	34	nC	I _D = 9.0A
Q _{gs}	Gate-to-Source Charge	—	—	4.8		V _{DS} = 80V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	20		V _{GS} = 5.0V, See Fig. 6 and 13 ④⑤
t _{d(on)}	Turn-On Delay Time	—	7.2	—	ns	V _{DD} = 50V
t _r	Rise Time	—	53	—		I _D = 9.0A
t _{d(off)}	Turn-Off Delay Time	—	30	—		R _G = 6.0Ω, V _{GS} = 5.0V
t _f	Fall Time	—	26	—		R _D = 5.5Ω, See Fig. 10 ④⑤
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact⑥
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	800	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	160	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	90	—		f = 1.0MHz, See Fig. 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	17	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①②	—	—	60		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 9.0A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	140	210	ns	T _J = 25°C, I _F = 9.0A
Q _{rr}	Reverse Recovery Charge	—	740	1100	nC	di/dt = 100A/μs ④⑤
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② V_{DD} = 25V, starting T_J = 25°C, L = 3.1mH
R_G = 25Ω, I_{AS} = 9.0A. (See Figure 12)
- ③ I_{SD} ≤ 9.0A, di/dt ≤ 540A/μs, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 175°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%
- ⑤ Uses IRL530N data and test conditions
- ⑥ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact

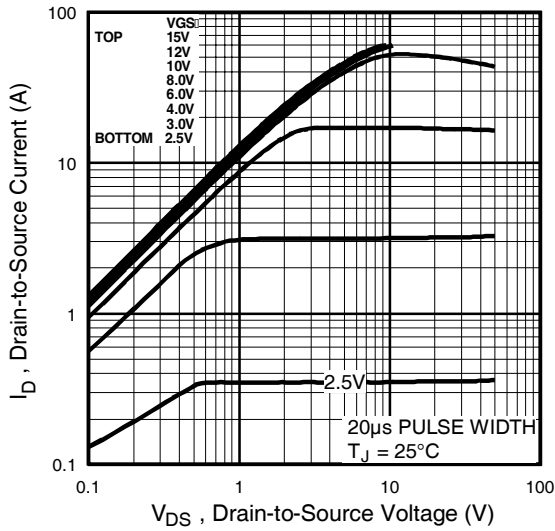


Fig 1. Typical Output Characteristics

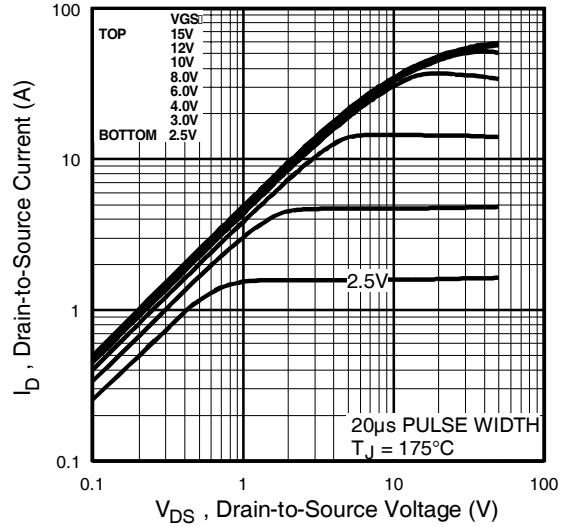


Fig 2. Typical Output Characteristics

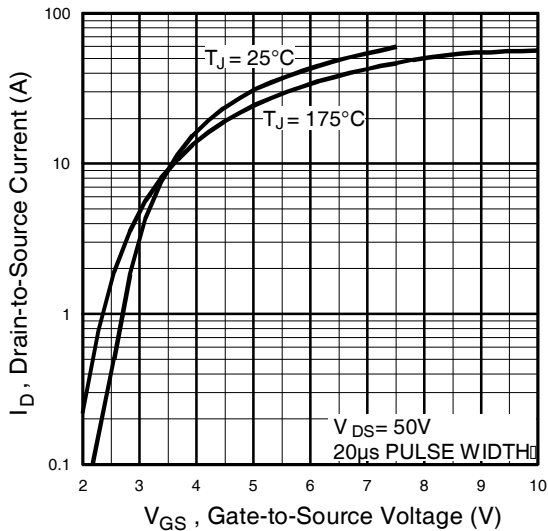


Fig 3. Typical Transfer Characteristics

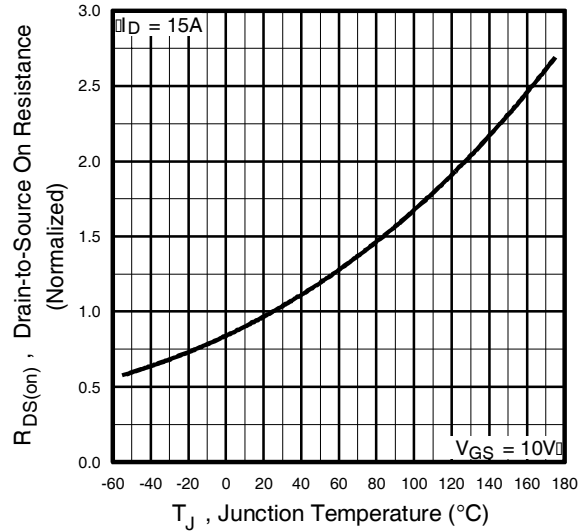


Fig 4. Normalized On-Resistance Vs. Temperature

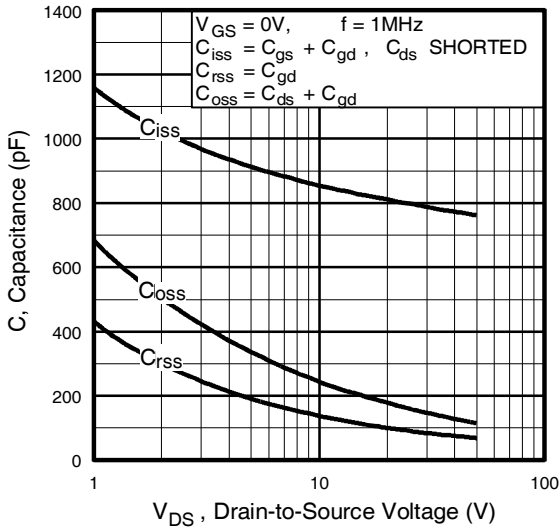


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

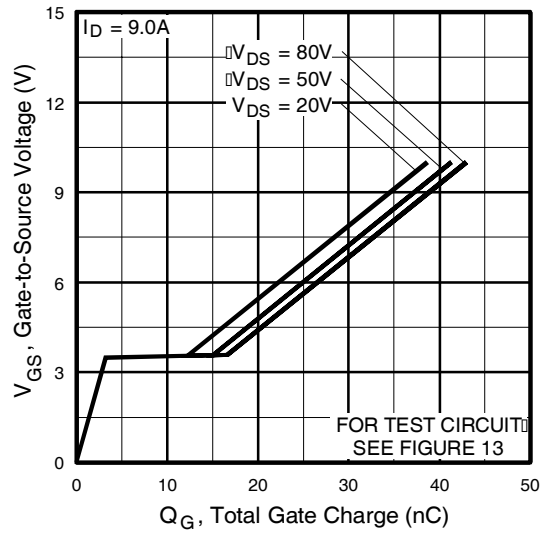


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

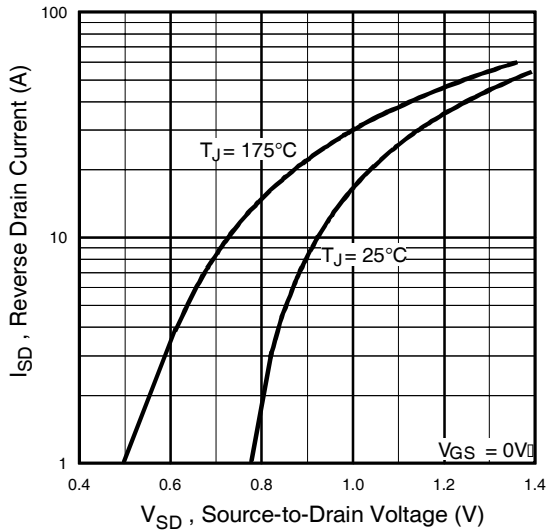


Fig 7. Typical Source-Drain Diode Forward Voltage

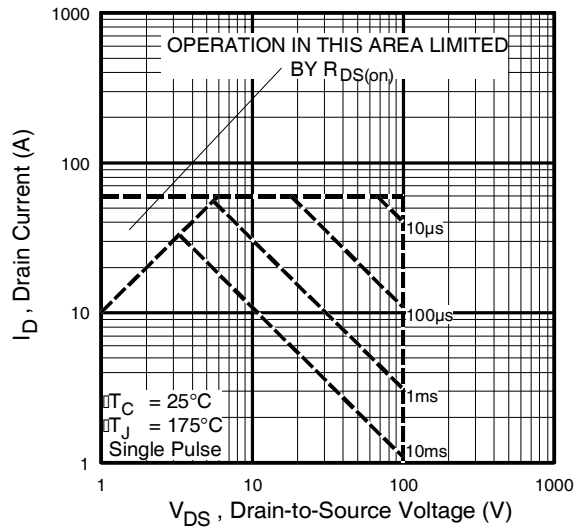


Fig 8. Maximum Safe Operating Area

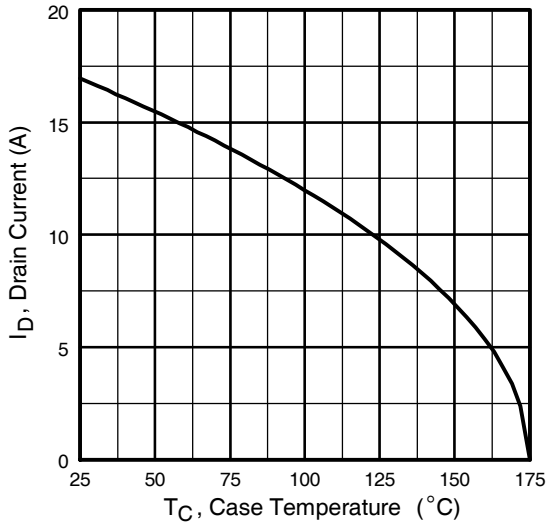


Fig 9. Maximum Drain Current Vs. Case Temperature

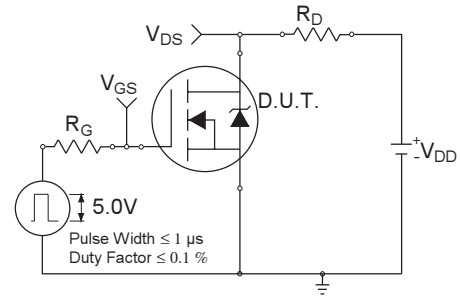


Fig 10a. Switching Time Test Circuit

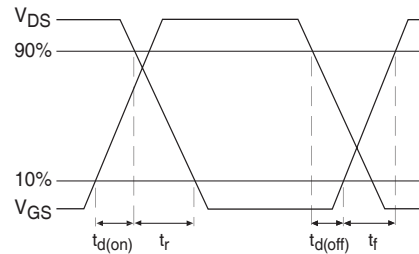


Fig 10b. Switching Time Waveforms

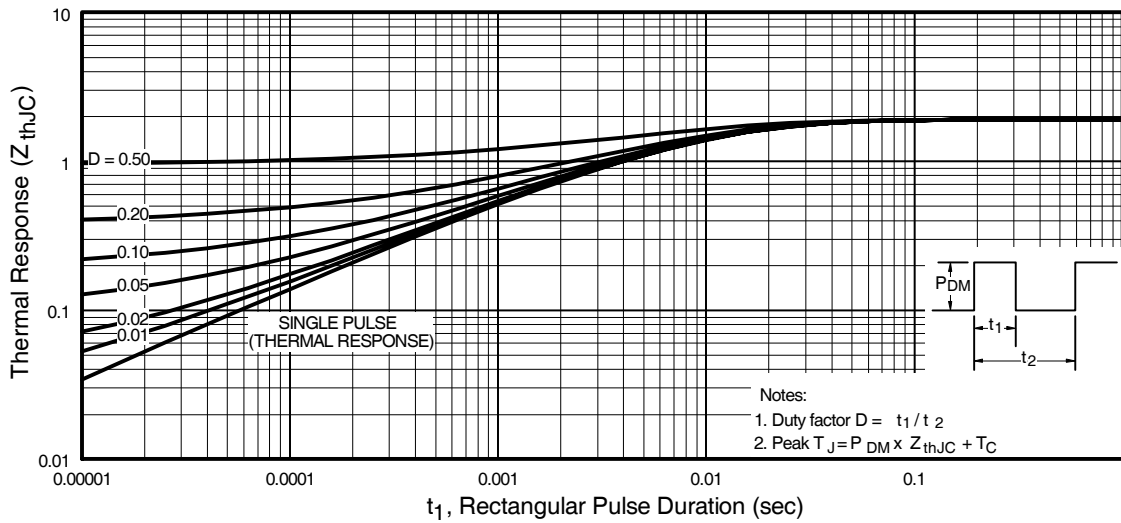


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

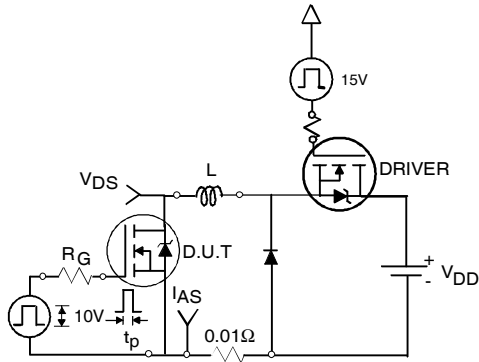


Fig 12a. Unclamped Inductive Test Circuit

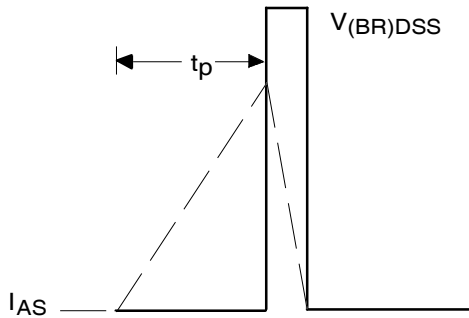


Fig 12b. Unclamped Inductive Waveforms

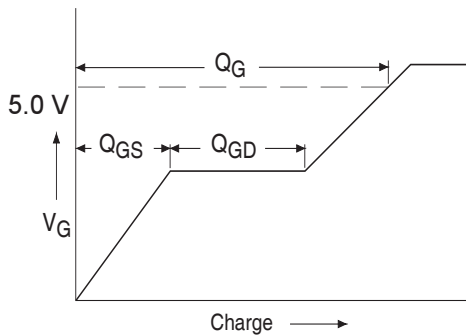


Fig 13a. Basic Gate Charge Waveform

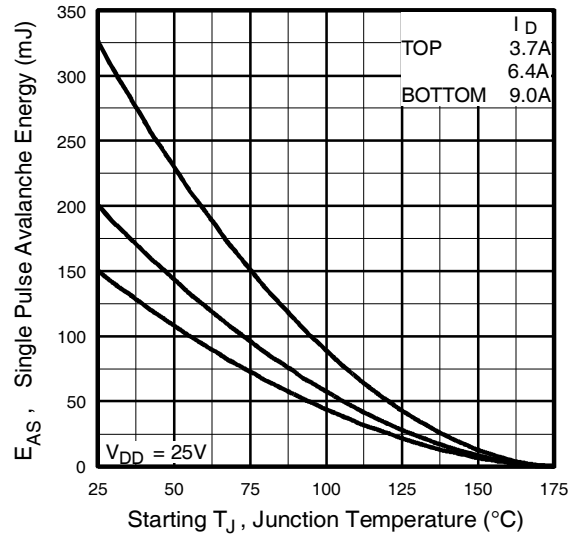


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

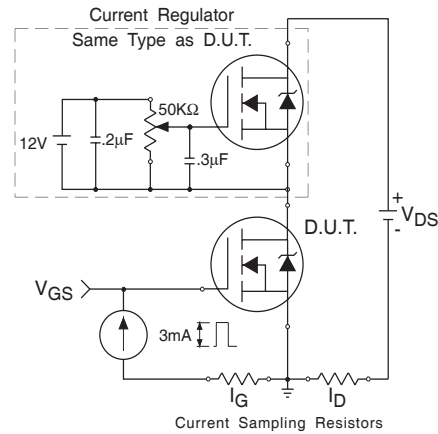
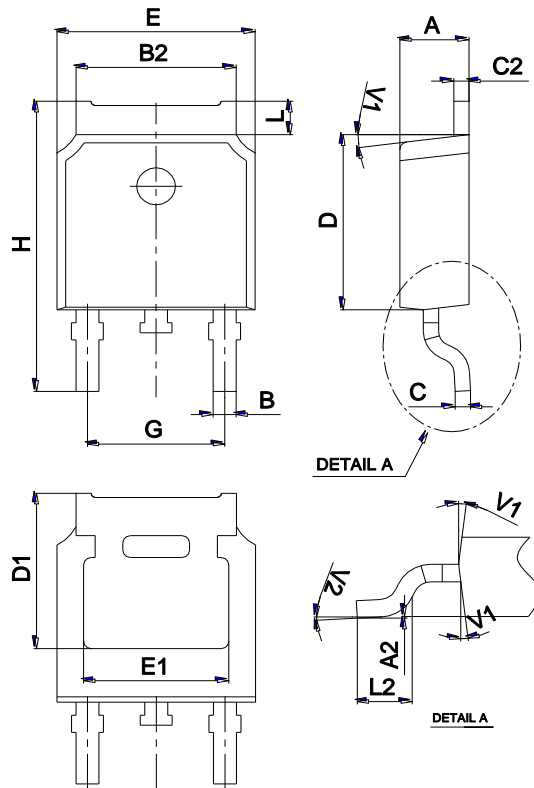


Fig 13b. Gate Charge Test Circuit

Package Mechanical Data TO-252

N-Channel MOSFET



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Ordering information

Order code	Package	Baseqty	Delivery mode
UMW IRLR3410TR	TO-252	2500	Tape and reel