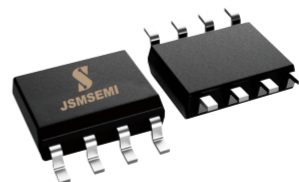


DESCRIPTION

The RSS090P03 is the P-Channel logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology..

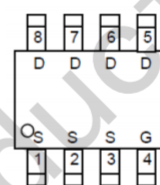
This high density process is especially tailored to minimize on-state resistance.

This device is suitable for use as a load switch or in PWM and gate charge for most of the synchronous buck converter applications

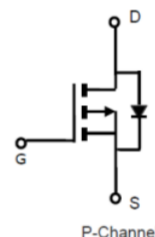


FEATURE

- ◆ **-30V/-13A, $R_{DS(ON)} = 9\text{ m}\Omega$ (typ.)@ $V_{GS} = -10\text{V}$**
- ◆ **-30V/-7.0A, $R_{DS(ON)} < 14.5\text{ m}\Omega$ (typ.)@ $V_{GS} = -4.5\text{V}$**
- ◆ Super high design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and Maximum DC current capability
- ◆ Full RoHS compliance
- ◆ SOP8 package design



TOP VIEW
SOP-8



APPLICATIONS

- ◆ High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/GA
- ◆ Newworking DC-DC Power System
- ◆ Load Switch
- ◆ Power Management in Note Book

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current ($T_A = 25^\circ\text{C}$)	$V_{GS} = 10\text{V}$	-13
	Continuous Drain Current ($T_A = 70^\circ\text{C}$)		-9.5
I_{DM}	Pulsed Drain Current	-40	A
I_S	Continuous Source Current (Diode Conduction)	-2.0	A
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	2.0
		$T_A = 70^\circ\text{C}$	1.5
T_J	Operation Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55~+150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	85	$^\circ\text{C/W}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress rating only and functional device operation is not implied

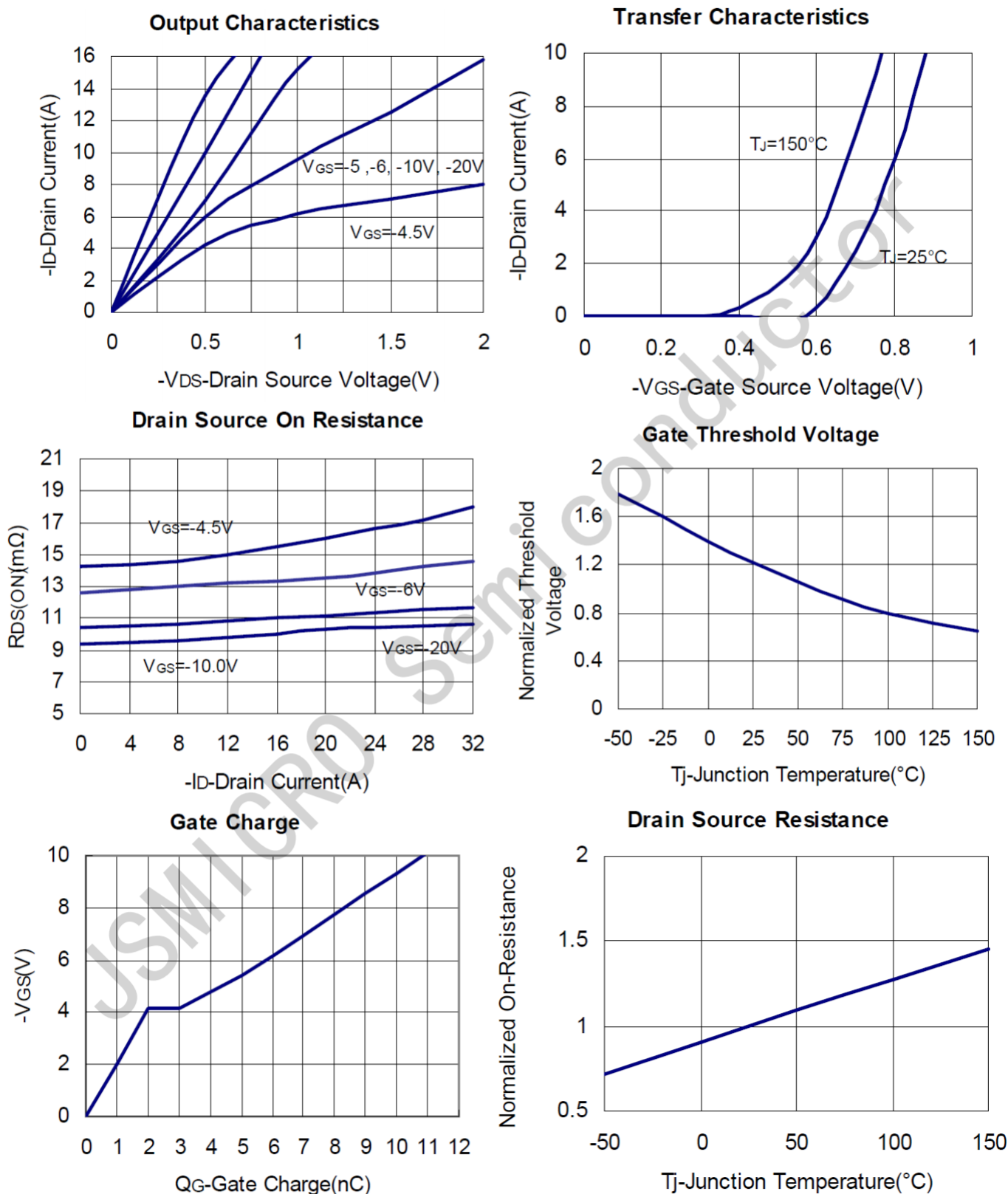
ELECTRICAL CHARACTERISTICS ($T_A=25\text{ }^{\circ}\text{C}$ Unless otherwise noted)

Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0	-1.4	-2.0	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 25V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-30V, V_{GS}=0$			-1	μA
		$V_{DS}=-30V, V_{GS}=0$ $T_J=55^{\circ}C$			-5	
$R_{DS(ON)}$	Drain-Source On-Resistance	$V_{GS}=-10V, I_D=-10A$		9	13	m Ω
		$V_{GS}=-4.5V, I_D=-7.0A$		14.5	17	
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	$I_S=-2.3A, V_{GS}=0V$		-0.75	-1.0	V
Dynamic Parameters						
Q_g	Total Gate Charge	$V_{DS}=-15V$ $V_{GS}=-4.5V$ $I_D=-10A$		30	42	nC
Q_{gs}	Gate-Source Charge			10	14	
Q_{gd}	Gate-Drain Charge			10.4	14.6	
C_{iss}	Input Capacitance	$V_{DS}=-15V$ $V_{GS}=0V$ $f=1MHz$		2050	2730	pF
C_{oss}	Output Capacitance			506	710	
C_{rss}	Reverse Transfer Capacitance			420	590	
$T_{d(on)}$	Turn-On Time	$V_{DS}=-15V$ $I_D=-10A$		9.3	19	nS
T_r				10.2	18	
$T_{d(off)}$	Turn-Off Time	$V_{GEN}=-10V$ $R_G=3.3\Omega$		117	232	
T_f				24	46	

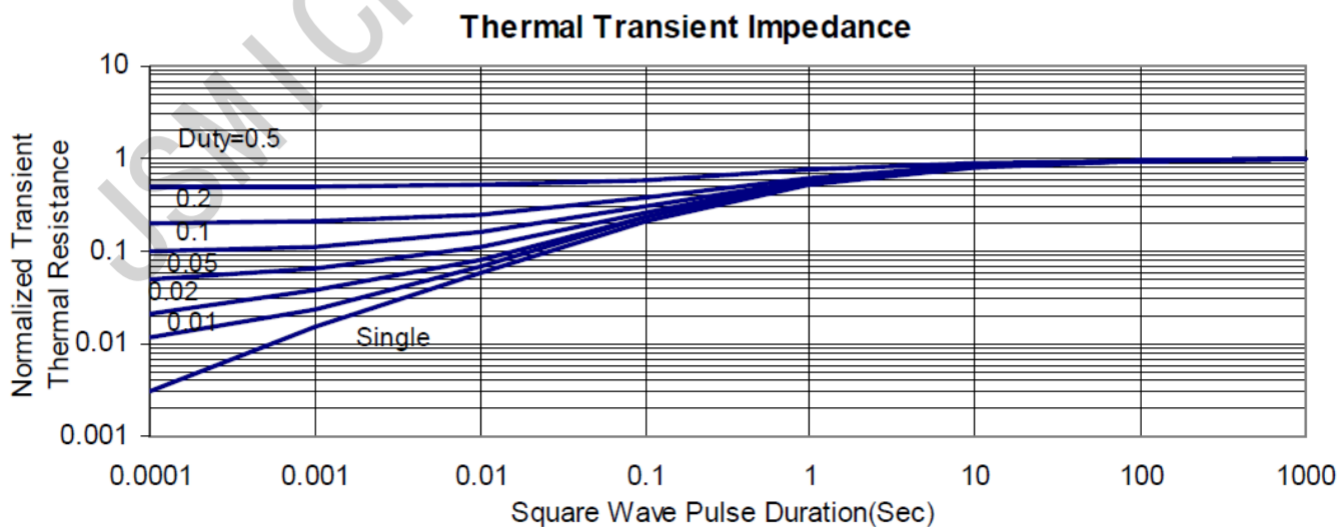
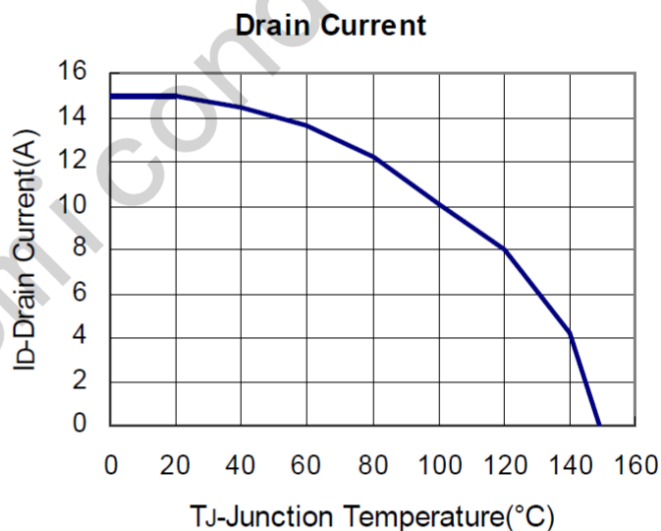
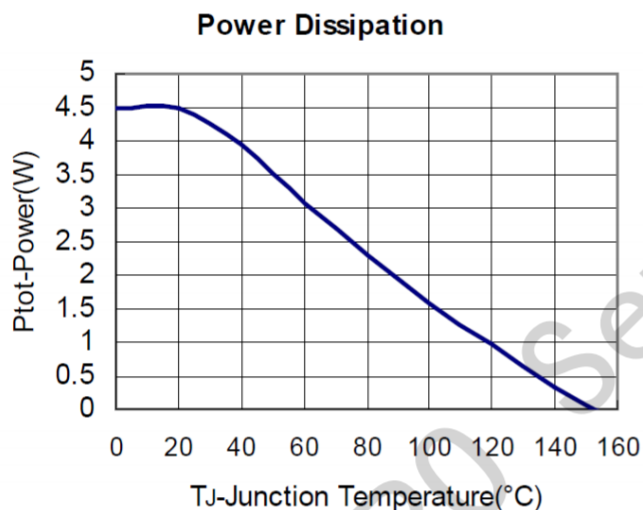
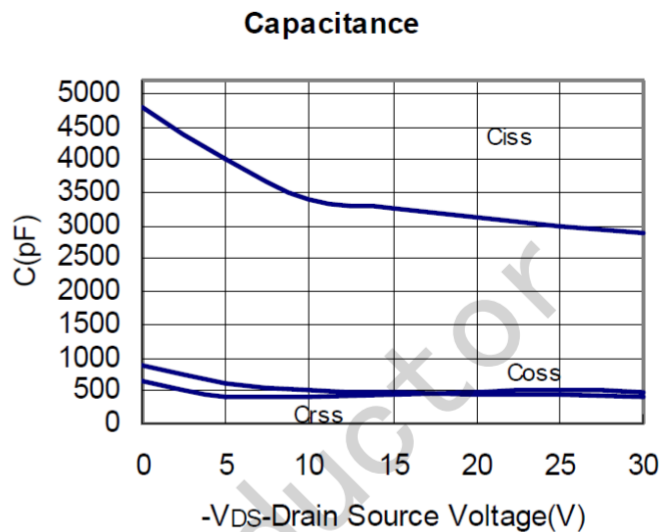
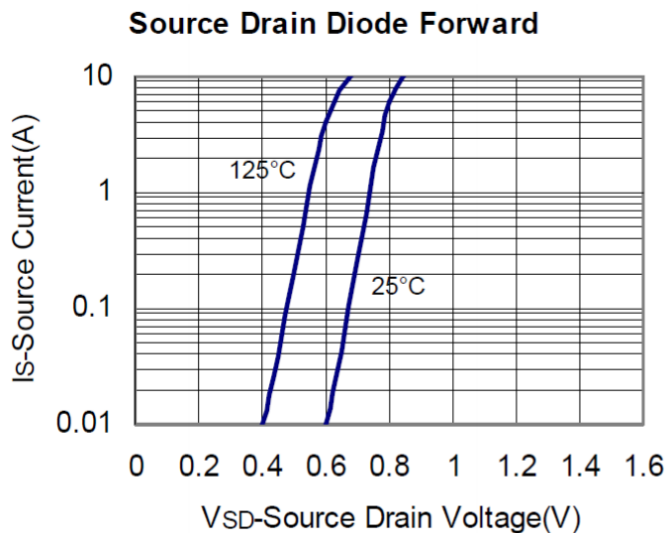
Note: 1. Pulse test: pulse width $\leq$ 300uS, duty cycle $\leq$ 2%

2.Static parameters are based on package level with recommended wire bonding

■ **TYPICAL CHARACTERISTICS** (25 °C Unless Note)

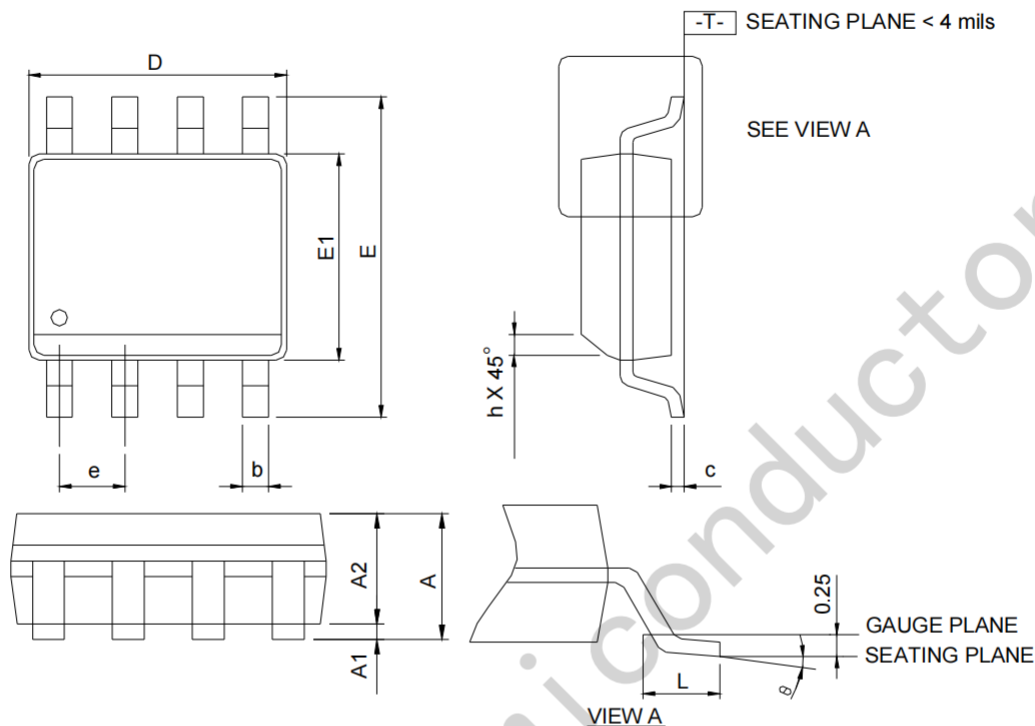


TYPICAL CHARACTERISTICS (continuous)



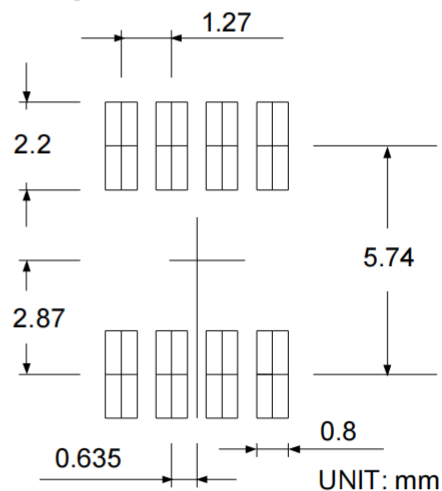
Package Information

SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

RECOMMENDED LAND PATTERN



Note: 1. Follow JEDEC MS-012 AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.