G3R40MT12J
1200 V 40 mΩ SiC MOSFET

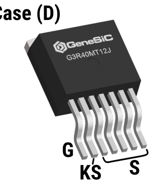
Silicon Carbide MOSFET
N-Channel Enhancement Mode

V_{DS}	=	1200 V
$R_{DS(ON)(Typ.)}$	=	40 mΩ
I_D (T_C = 100°C)	=	42 A

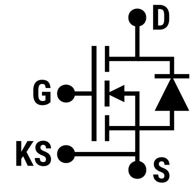
Features

- G3R™ SiC MOSFET Technology
- Superior Q_G x $R_{DS(ON)}$ Figure of Merit
- Low Capacitances and Low Gate Charge
- Normally-Off Stable Operation up to 175°C
- Fast and Reliable Body Diode
- High Avalanche and Short Circuit Ruggedness
- Low Conduction Losses at High Temperatures
- Optimized Package with Separate Driver Source Pin

Package



TO-263-7



D = Drain
G = Gate
S = Source
KS = Kelvin Source

RoHS
REACH

Advantages

- Increased Power Density for Compact System
- High Frequency Switching
- Reduced Losses for Higher System Efficiency
- Minimized Gate Ringing
- Improved Thermal Capabilities
- High Cost-Performance Index
- Ease of Paralleling without Thermal Runaway
- Simple to Drive

Applications

- Solar Inverters
- EV/HEV Charging
- Motor Drives
- High Voltage DC-DC Converters
- Switched Mode Power Supplies
- UPS
- Smart Grid Transmission and Distribution
- Induction Heating and Welding

Absolute Maximum Ratings (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values	Unit	Note
Drain-Source Voltage	$V_{DS(max)}$	V_{GS} = 0 V, I_D = 100 µs	1200	V	
Gate-Source Voltage (Dynamic)	$V_{GS(max)}$		-10 / +25	V	
Gate-Source Voltage (Static)	$V_{GS(op)}$	Recommended Operation	-5 / +20	V	
Continuous Forward Current	I_D	T_C = 100°C, V_{GS} = 20 V T_C = 135°C, V_{GS} = 20 V	42 31	A	Fig. 15
Pulsed Drain Current	$I_{D(pulse)}$	t_P ≤ 10µs, D ≤ 1%, Note 1	140	A	Fig. 14
Power Dissipation	P_D	T_c = 25°C	222	W	Fig. 16
Operating and Storage Temperature	T_j , T_{stg}		-55 to 175	°C	

Thermal/Package Characteristics

Parameter	Symbol	Conditions	Values Min.	Values Typ.	Values Max.	Unit	Note
Thermal Resistance, Junction - Case	R_{thJC}			0.68		°C/W	Fig. 13
Weight	W_T			1.45		g	

Note 1: Pulse Width t_P Limited by $T_{j(max)}$

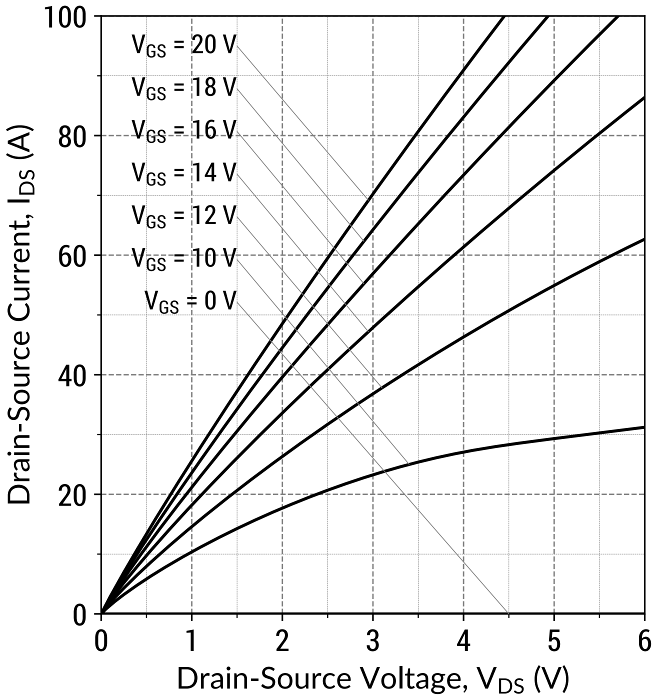
Electrical Characteristics (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values Min.	Values Typ.	Values Max.	Unit	Note
Drain-Source Breakdown Voltage	V_{DSS}	V_{GS} = 0 V, I_D = 100 µA	1200			V	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V		1		µA	
Gate Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 25 V V_{DS} = 0 V, V_{GS} = -10 V			100 -100	nA	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 10.0 mA V_{DS} = V_{GS}, I_D = 10.0 mA, T_j = 175°C	2.3	3.0 2.1	4.0	V	Fig. 9
Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 35 A V_{DS} = 10 V, I_D = 35 A, T_j = 175°C		16.6 15.0		S	Fig. 4
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 20 V, I_D = 35 A V_{GS} = 20 V, I_D = 35 A, T_j = 175°C		40 62	48	mΩ	Fig. 5-8
Input Capacitance	C_{iss}	V_{DS} = 800 V, V_{GS} = 0 V f = 1 MHz, V_{AC} = 25mV		1974		pF	Fig. 11
Output Capacitance	C_{oss}			141		pF	Fig. 11
Reverse Transfer Capacitance	C_{rss}			12.5		pF	Fig. 11
C_{oss} Stored Energy	E_{oss}			86		µJ	Fig. 12
C_{oss} Stored Charge	Q_{oss}			173		nC	
Gate-Source Charge	Q_{gs}	V_{DS} = 800 V, V_{GS} = -5 / +20 V I_D = 35 A Per IEC607478-4		22		nC	Fig. 10
Gate-Drain Charge	Q_{gd}			36		nC	Fig. 10
Total Gate Charge	Q_g			103		nC	Fig. 10
Internal Gate Resistance	$R_{G(int)}$	f = 1 MHz, V_{AC} = 25 mV		2.0		Ω	

Reverse Diode Characteristics

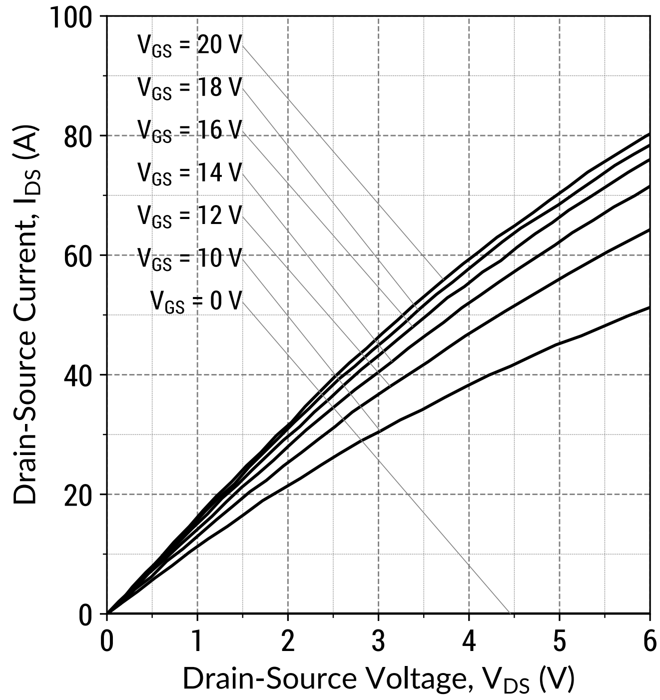
Parameter	Symbol	Conditions	Values Min.	Values Typ.	Values Max.	Unit	Note
Diode Forward Voltage	V_{SD}	V_{GS} = -5 V, I_{SD} = 17 A V_{GS} = -5 V, I_{SD} = 17 A, T_j = 175°C		4.5 4.0		V	Fig. 17-18
Continuous Diode Forward Current	I_S	V_{GS} = -5 V, T_c = 100°C		23		A	
Diode Pulse Current	$I_{S(pulse)}$	V_{GS} = -5 V, Note 1		140		A	

Figure 1: Output Characteristics (T_j = 25°C)



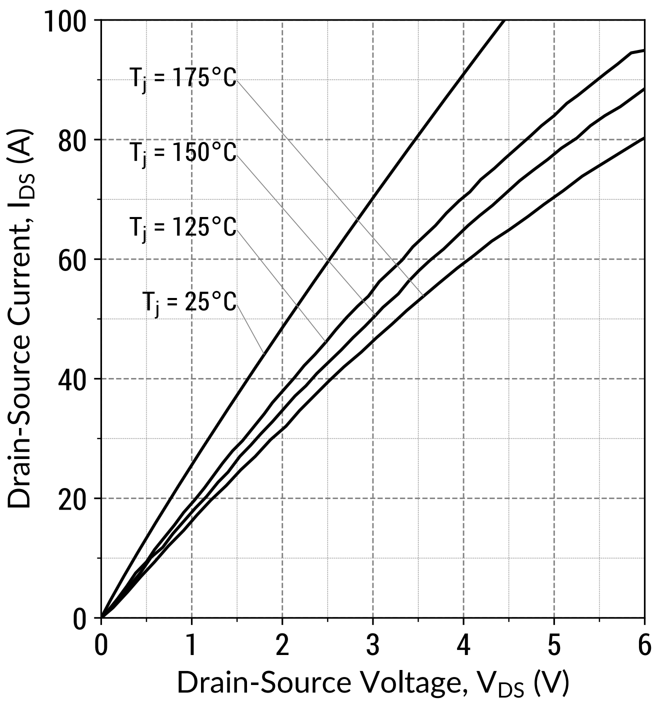
$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Figure 2: Output Characteristics (T_j = 175°C)



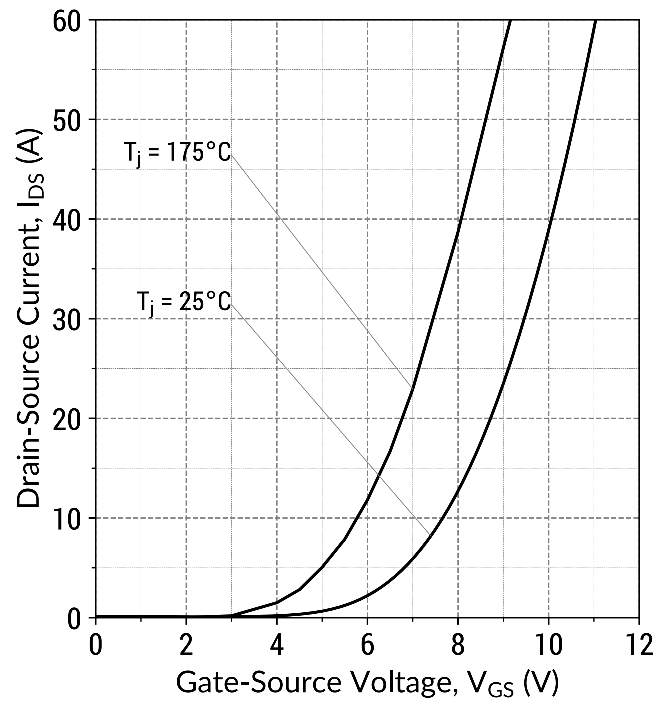
$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Figure 3: Output Characteristics (V_{GS} = 20 V)



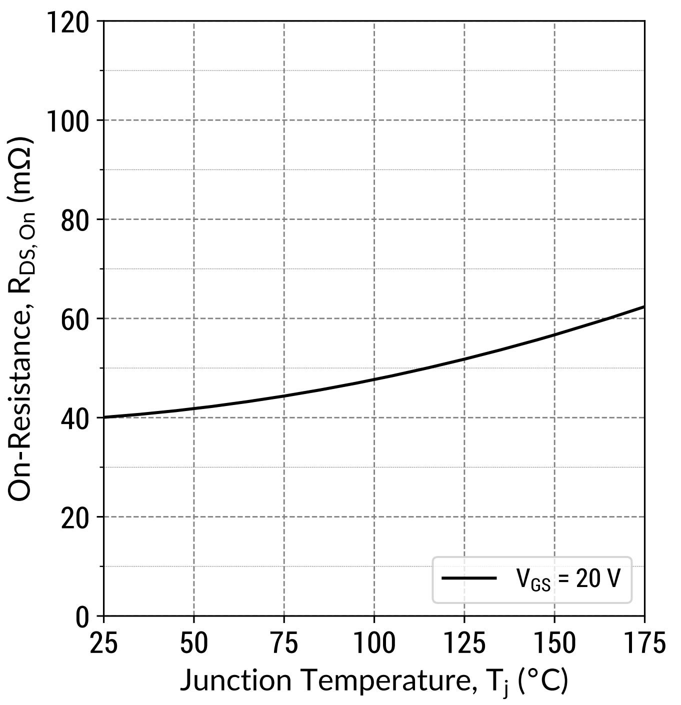
$I_D = f(V_{DS}, T_j)$; t_P = 250 µs

Figure 4: Transfer Characteristics (V_{DS} = 10 V)



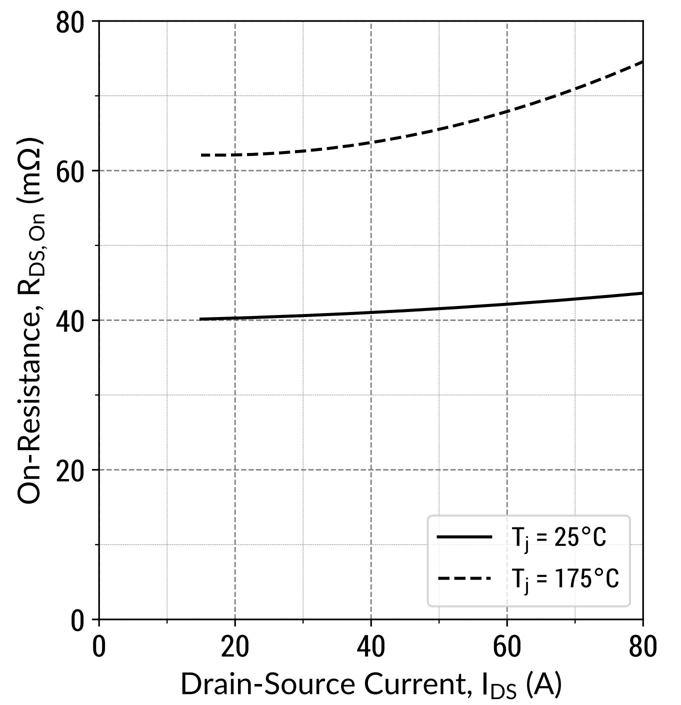
$I_D = f(V_{GS}, T_j)$; t_P = 100 µs

Figure 5: On-State Resistance v/s Temperature



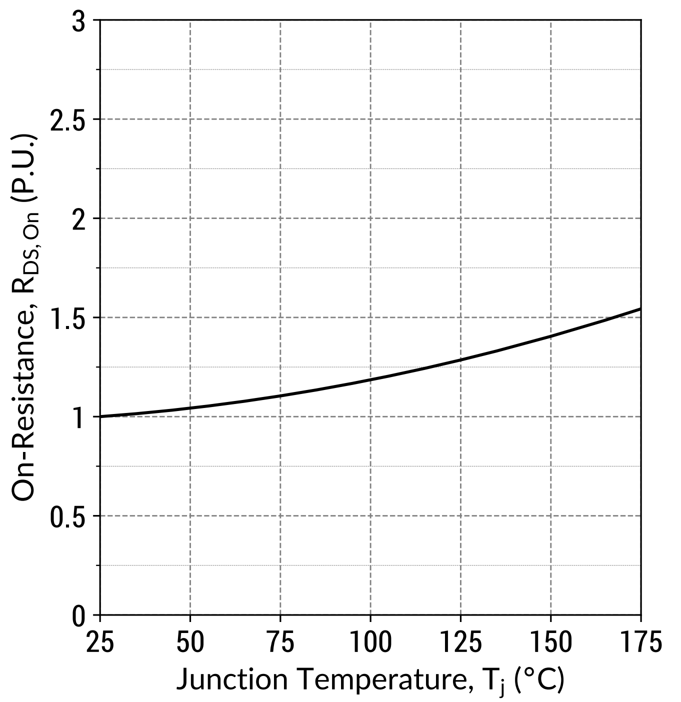
$R_{DS(ON)} = f(T_j, V_{GS})$; t_P = 250 µs; I_D = 35 A

Figure 6: On-State Resistance v/s Drain Current



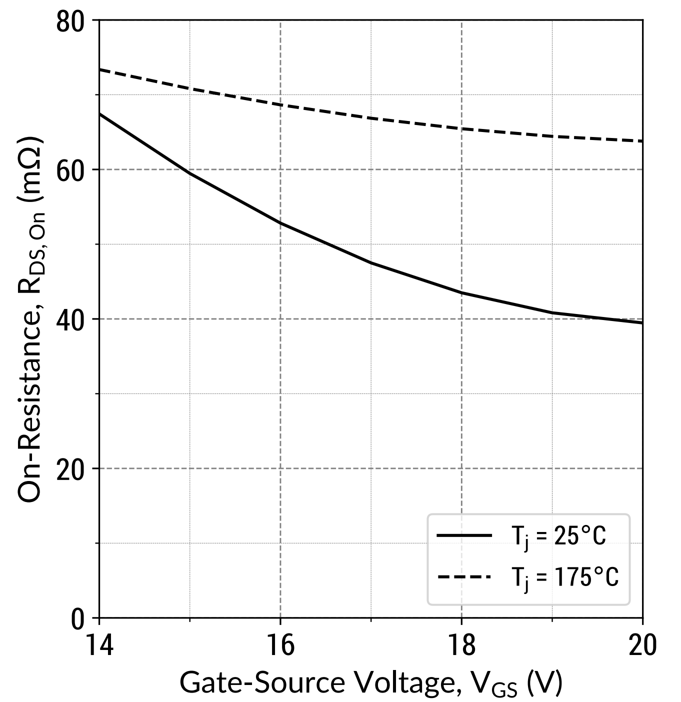
$R_{DS(ON)} = f(T_j, I_D)$; t_P = 250 µs; V_{GS} = 20 V

Figure 7: Normalized On-State Resistance v/s Temperature



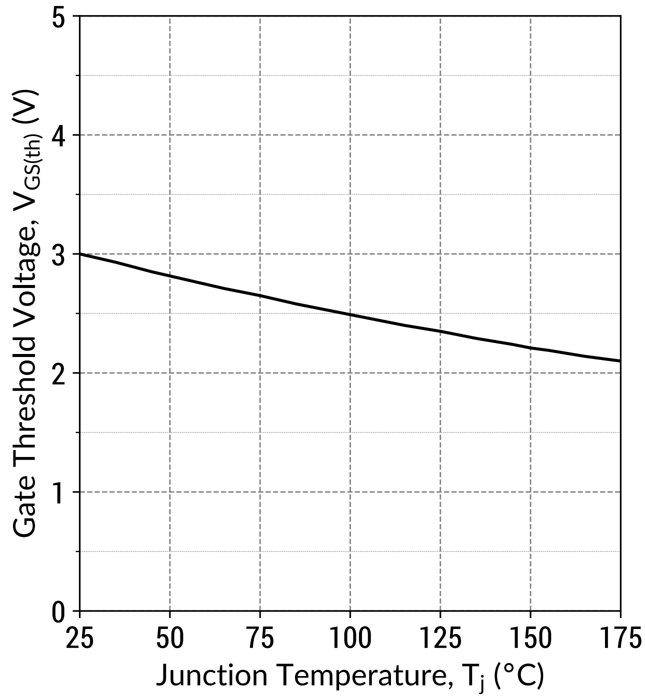
$R_{DS(ON)} = f(T_j)$; t_P = 250 µs; I_D = 35 A; V_{GS} = 20 V

Figure 8: On-State Resistance v/s Gate Voltage



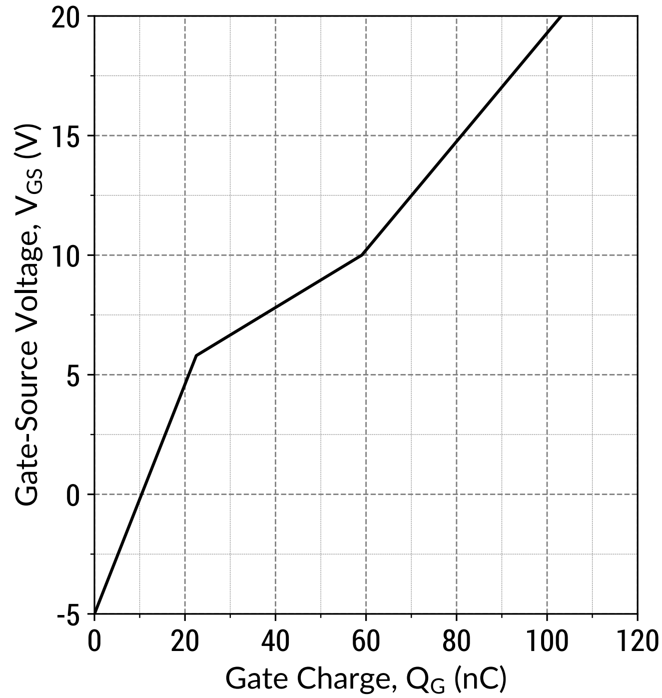
$R_{DS(ON)} = f(T_j, V_{GS})$; t_P = 250 µs; I_D = 35 A

Figure 9: Threshold Voltage Characteristics



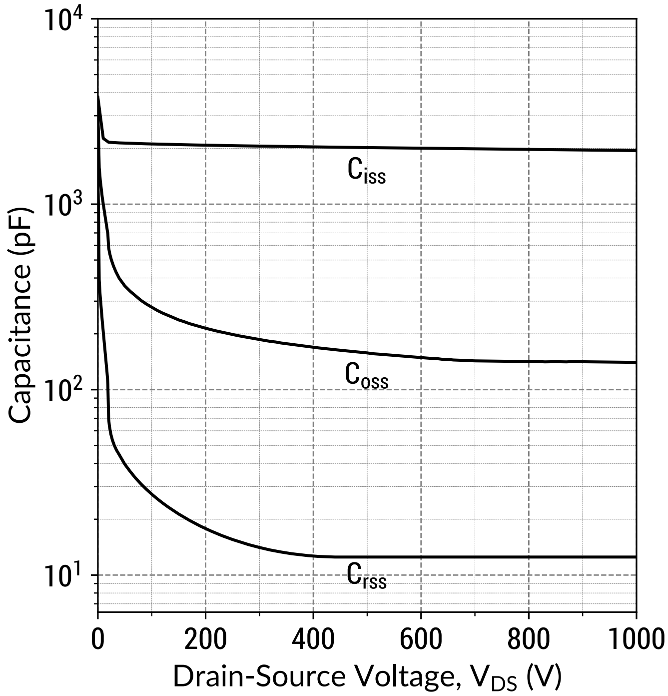
$V_{GS(th)} = f(T_j)$; $V_{DS} = V_{GS}$; $I_D = 10.0$ mA

Figure 10: Gate Charge Characteristics



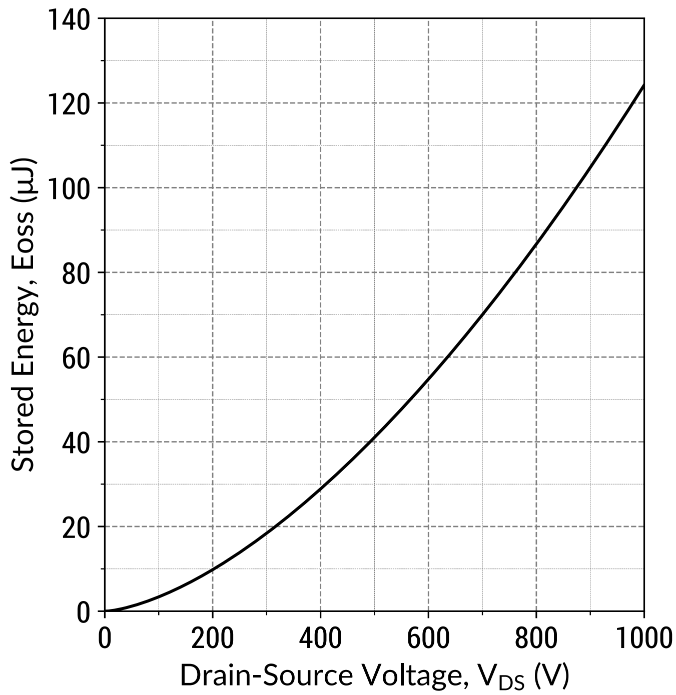
$I_D = 35$ A; $V_{DS} = 800$ V; $T_c = 25$°C

Figure 11: Capacitance v/s Drain-Source Voltage



f = 1 MHz; V_{AC} = 25mV

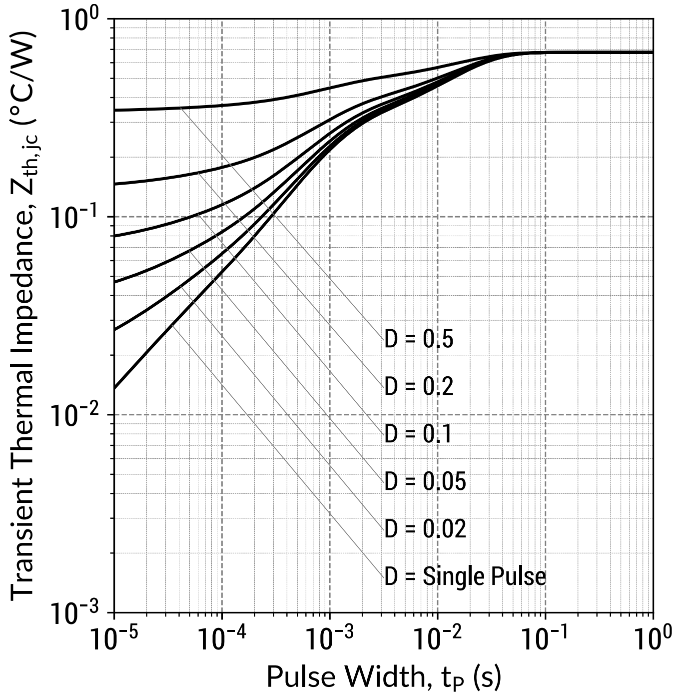
Figure 12: Output Capacitor Stored Energy



$E_{oss} = f(V_{DS})$

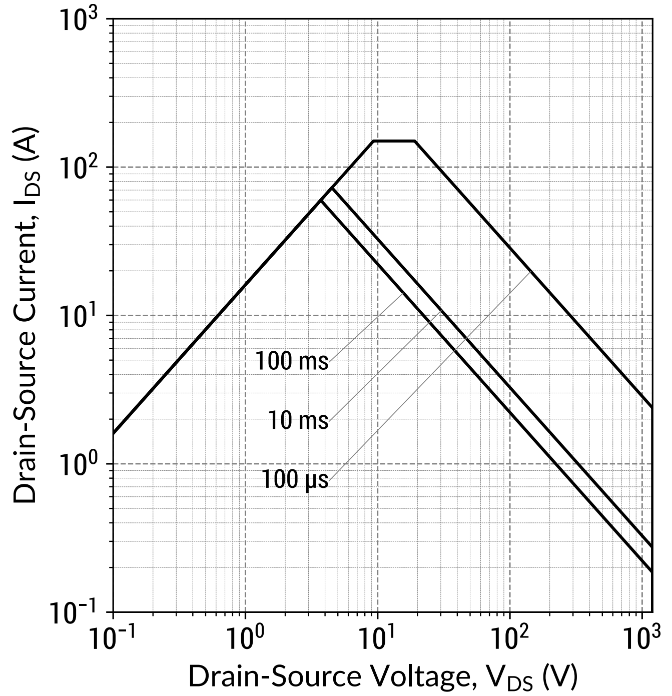
GeneSiC SEMICONDUCTOR

Figure 13: Transient Thermal Impedance



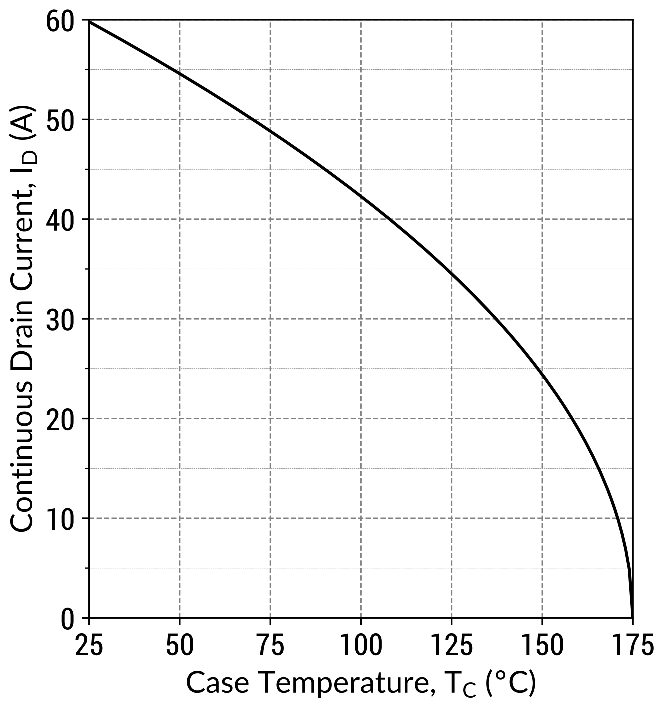
$Z_{th,jc} = f(t_P, D)$; $D = t_P/T$

Figure 14: Safe Operating Area (T_c = 25°C)



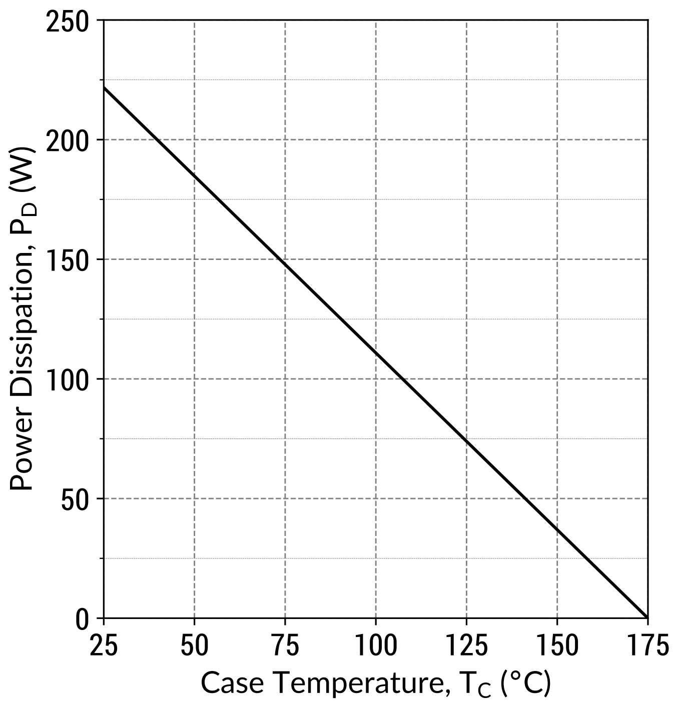
$I_D = f(V_{DS}, t_P)$; $T_j \leq 175°C$; $D = 0$

Figure 15: Current De-rating Curve



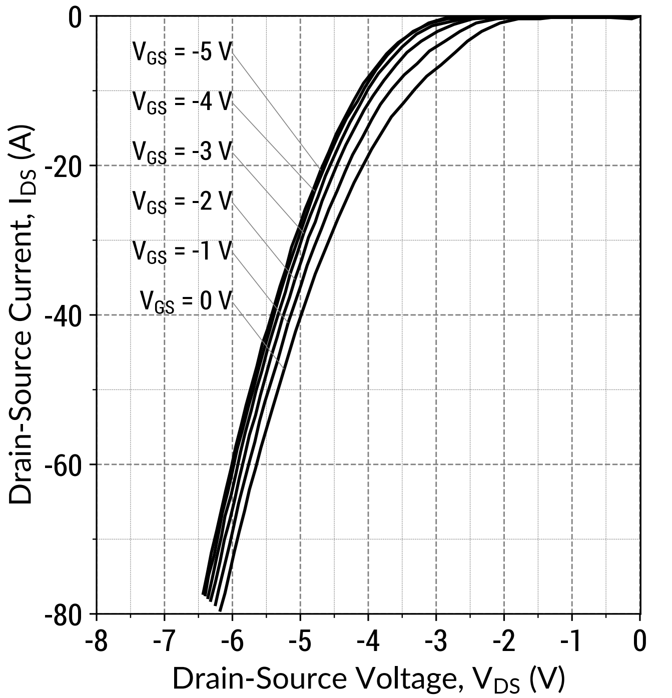
$I_D = f(T_C)$; $T_j \leq 175°C$

Figure 16: Power De-rating Curve



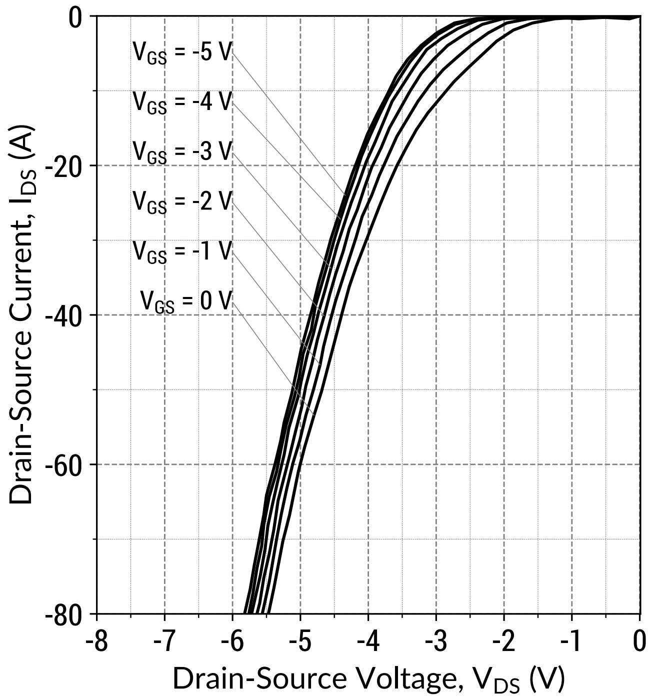
$P_D = f(T_C)$; $T_j \leq 175°C$

Figure 17: Body Diode Characteristics (T_j = 25°C)



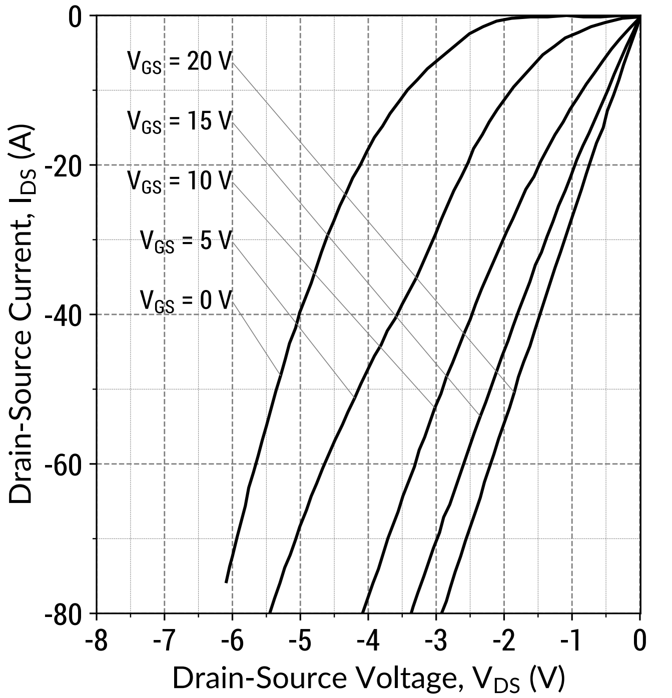
$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Figure 18: Body Diode Characteristics (T_j = 175°C)



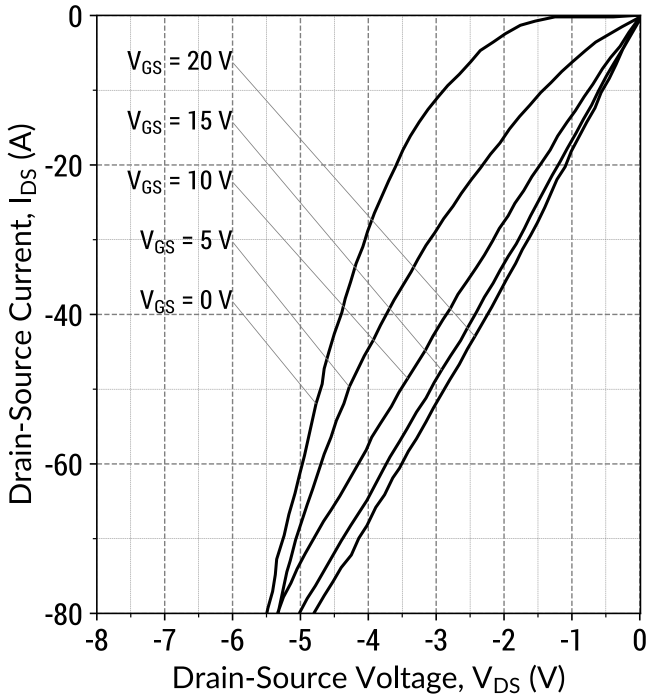
$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Figure 19: Third Quadrant Characteristics (T_j = 25°C)



$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

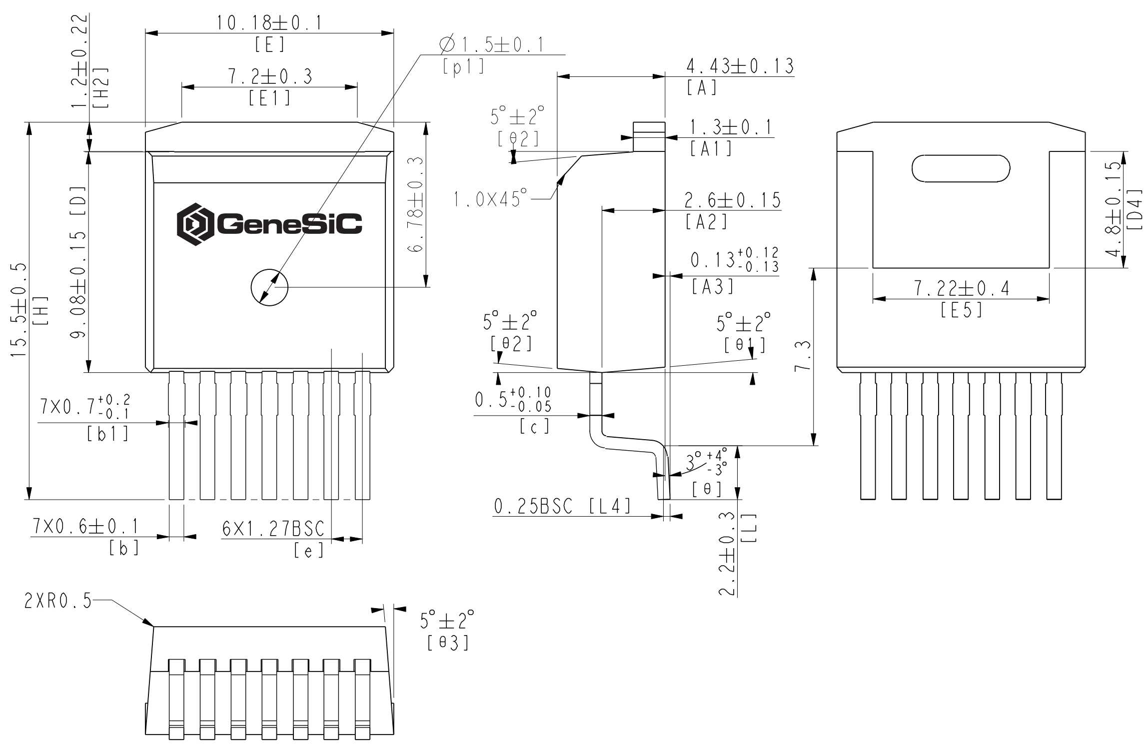
Figure 20: Third Quadrant Characteristics (T_j = 175°C)



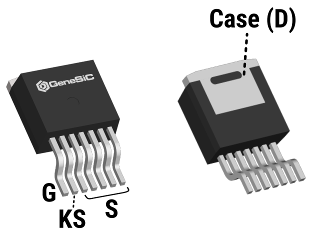
$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Package Dimensions

TO-263-7 Package Outline



Package View



NOTE

1. CONTROLLED DEIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS.

RoHS Compliance

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS 2), as adopted by EU member states on January 2, 2013 and amended on March 31, 2015 by EU Directive 2015/863. RoHS Declarations for this product can be obtained from your GeneSiC representative.

REACH Compliance

REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact a GeneSiC representative to insure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.

This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, or air traffic control systems.

GeneSiC disclaims all and any warranty and liability arising out of use or application of any product. No license, express or implied to any intellectual property rights is granted by this document.

Related Links

- SPICE Models: https://www.genesicsemi.com/sic-mosfet/G3R40MT12J/G3R40MT12J_SPICE.zip
- PLECS Models: https://www.genesicsemi.com/sic-mosfet/G3R40MT12J/G3R40MT12J_PLECS.zip
- CAD Models: https://www.genesicsemi.com/sic-mosfet/G3R40MT12J/G3R40MT12J_3D.zip
- Gate Driver Reference: https://www.genesicsemi.com/technical-support
- Evaluation Boards: https://www.genesicsemi.com/technical-support
- Reliability: https://www.genesicsemi.com/reliability
- Compliance: https://www.genesicsemi.com/compliance
- Quality Manual: https://www.genesicsemi.com/quality

www.genesicsemi.com/sic-mosfet/

Published by GeneSiC Semiconductor, Inc.
43670 Trade Center Place Suite 155, Dulles, VA 20166; USA