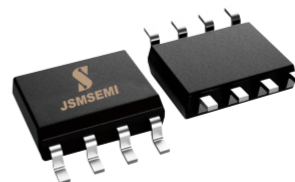


Description:

This N-Channel MOSFET uses advanced trench technology and

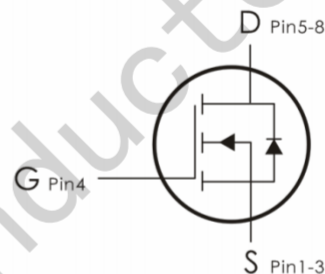
design to provide excellent $R_{DS(on)}$ with low gate charge.

It can be used in a wide variety of applications.



Features:

- 1) $V_{DS}=30V, I_D=20A, R_{DS(on)} < 6.5m\Omega @ V_{GS}=10V$
- 2) Low gate charge.
- 3) Green device available.
- 4) Advanced high cell density trench technology for ultra low $R_{DS(on)}$.
- 5) Excellent package for good heat dissipation.



Absolute Maximum Ratings: ($T_J=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current – Continuous ($T_A=25^\circ C$)	20	A
	Drain Current – Continuous ($T_A=75^\circ C$)	15.2	
	Drain Current – Pulsed① ($T_A=25^\circ C$)	76	
I_{DM}	Drain Current – Pulsed① ($T_A=25^\circ C$)	76	
I_S	Diode continuous forward current($T_A=25^\circ C$)	5	
P_D	Power Dissipation ($T_A=25^\circ C$)	3.1	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-50 to +150	$^\circ C$

Thermal Characteristics:

Symbol	Parameter	Max	Units
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	40	$^\circ C/W$

Electrical Characteristics: ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μ A	30	---	---	V
I _{DSS}	Drain-Source Leakage Current(T _A =25℃)	V _{DS} =30V , V _{GS} =0V	---	---	1	μA
	Drain-Source Leakage Current(T _A =125℃)	V _{DS} =24V , V _{GS} =0V	---	---	100	μA
I _{GSS}	Gate-Source Leakage Current	V _{GS} = ± 20V, V _{DS} =0V	---	---	±100	nA
On Characteristics						
V _{GS(th)}	GATE-Source Threshold Voltage	V _{GS} =V _{DS} , I _D =250 μ A	1	1.6	2.5	V
R _{DS(ON)}	Static Drain-Source On Resistance②	V _{GS} =10V, I _D =15A	---	5.2	6.5	m Ω
		V _{GS} =4.5V, I _D =8A	---	7.5	9.5	m Ω
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	1320	---	pF
C _{oss}	Output Capacitance		---	205	---	
C _{rss}	Reverse Transfer Capacitance		---	135	---	
R _g	Gate Resistance	f=1MHz	---	4.4	---	Ω
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} =15V, I _D =3A R _G =3.3 Ω , V _{GS} =10V	---	11	---	ns
t _r	Rise Time		---	30	---	ns
t _{d(off)}	Turn-Off Delay Time		---	24	---	ns
t _f	Fall Time		---	8	---	ns
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =15A	---	23.5	---	nC
Q _{gs}	Gate-Source Charge		---	3.3	---	nC
Q _{gd}	Gate-Drain “Miller” Charge		---	4.8	---	nC
Drain-Source Diode Characteristics						
V _{SD}	Source-Drain Diode Forward Voltage②	V _{GS} =0V, I _{SD} =12A	---	0.81	1.2	V

Trr	Body Diode Reverse Recovery Time	$I_{SD}=10A, V_{GS}=0V$	---	31	---	Ns
Qrr	Body Diode Reverse Recovery Charge	$di/dt=100A/\mu s$	---	20	---	Nc

Notes:

- ① Pulse width limited by maximum allowable junction temperature
- ② Pulse width $\leq 300 \mu s$; duty cycle $\leq 2\%$.

Typical Characteristics: ($T_C=25^\circ C$ unless otherwise noted)

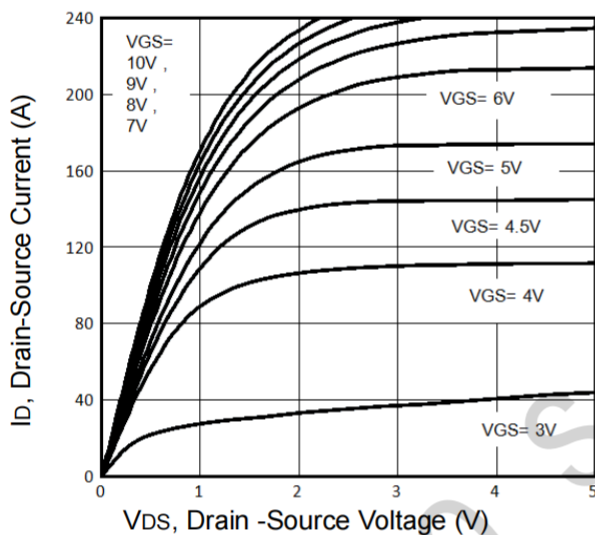


Fig1. Typical Output Characteristics

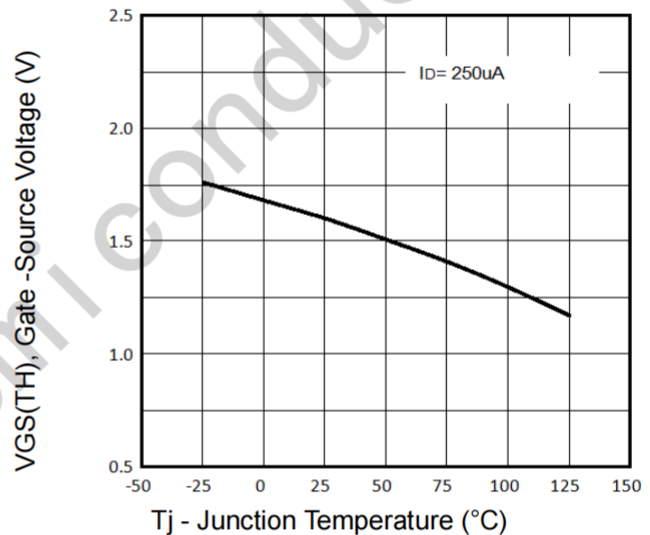


Fig2. VGS(TH) Voltage Vs. Temperature

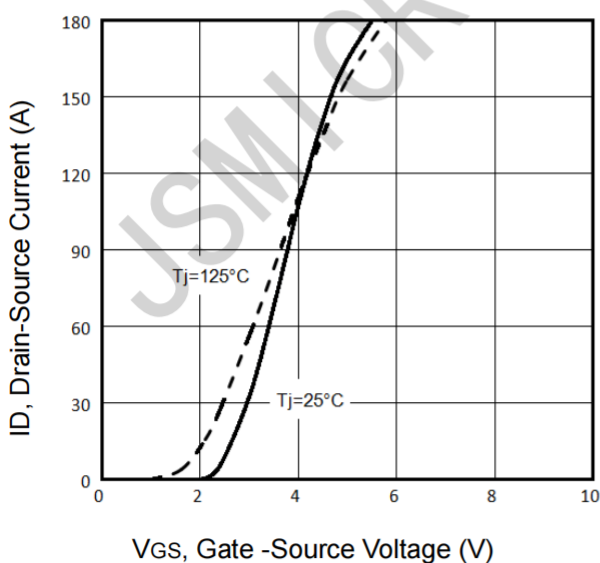


Fig3. Typical Transfer Characteristics

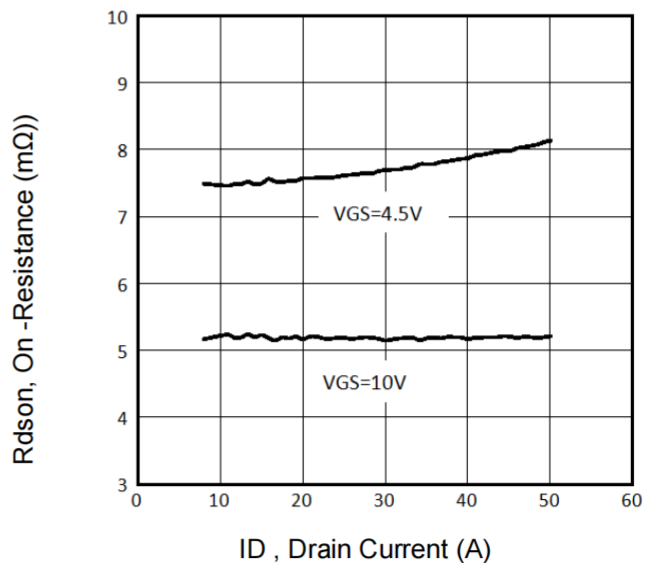


Fig4. On-Resistance vs. Drain Current and Gate Voltage

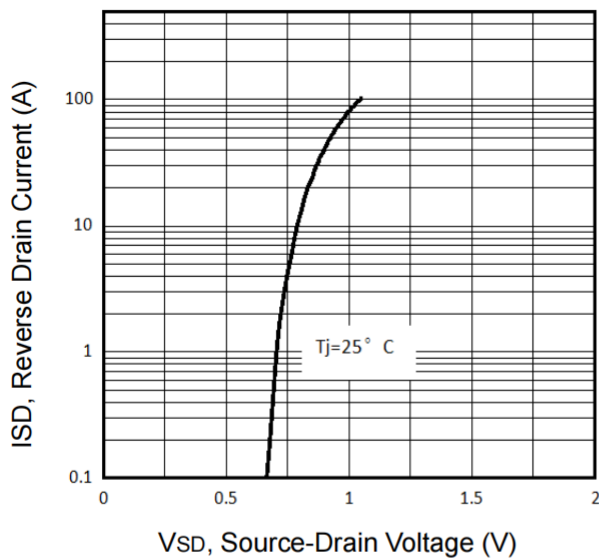


Fig5. Typical Source-Drain Diode Forward Voltage

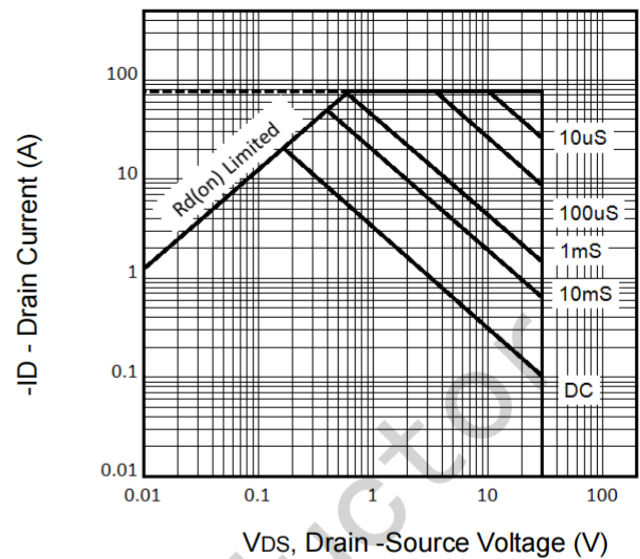


Fig6. Maximum Safe Operating Area

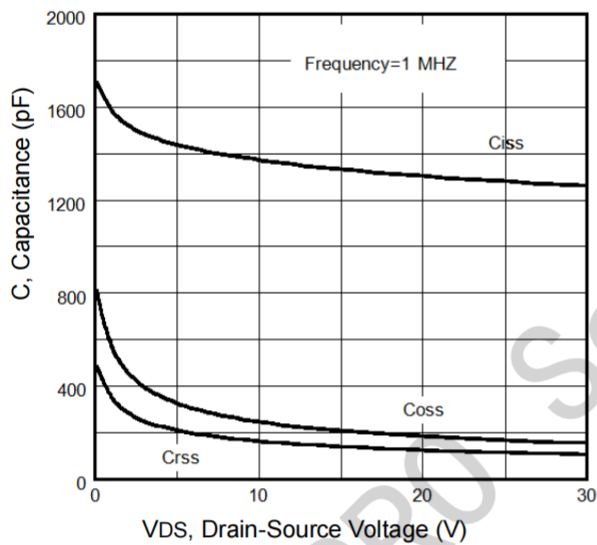


Fig7. Typical Capacitance Vs. Drain-Source Voltage

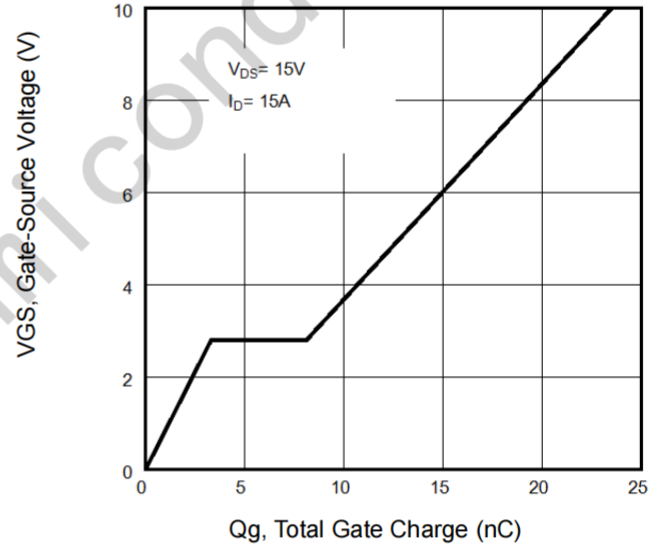


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

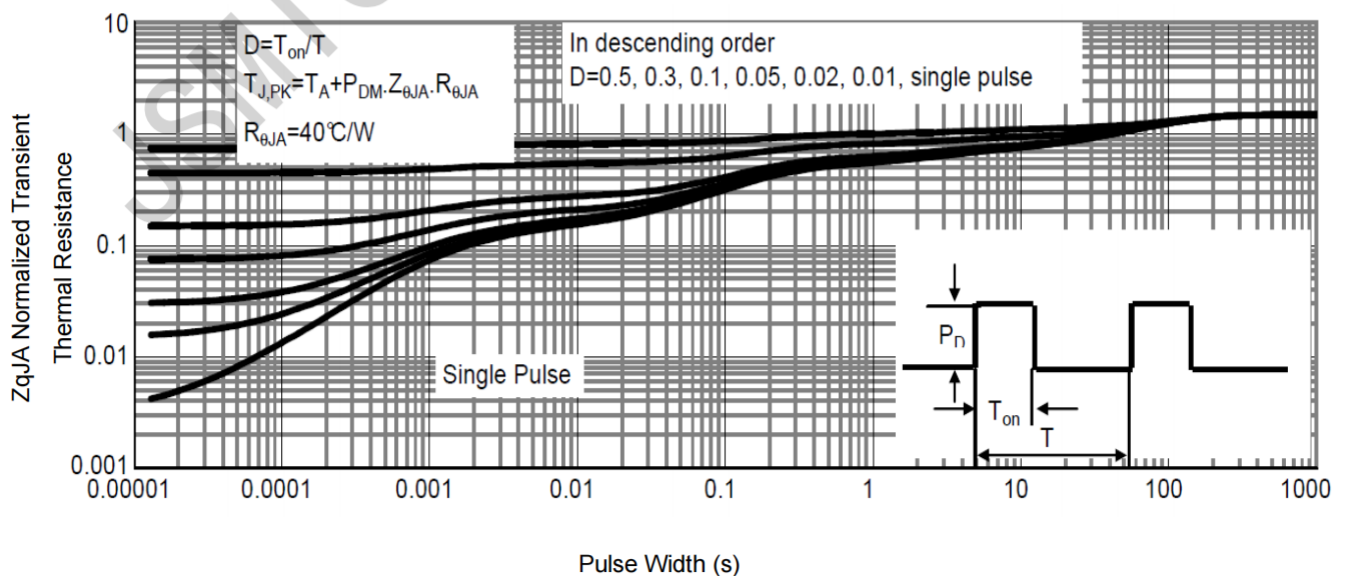
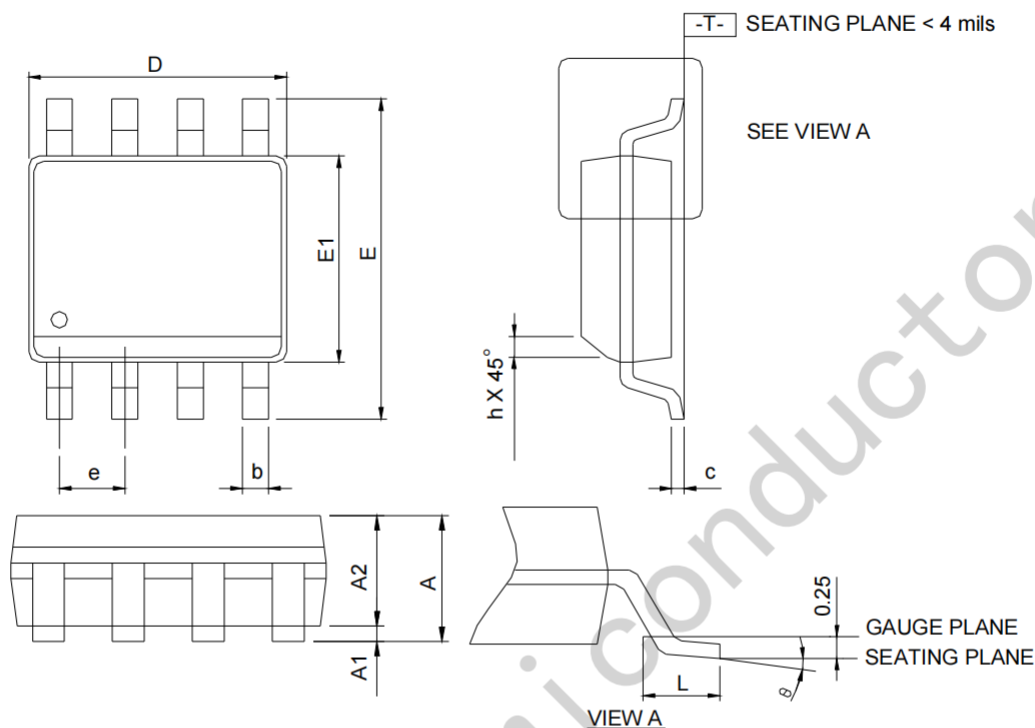


Fig9. Normalized Maximum Transient Thermal Impedance

Package Information

SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

RECOMMENDED LAND PATTERN

