Low EMI, 3.2W Dual Mode Mono Audio Amplifier with NCN

Features

- Supply Voltage from 2.5V to 6.0V
- 3.2W@10% THD Output with a 4Ω Load at 5V Supply
- High Efficiency Up to 90% @1W with an 8Ω Speaker
- None Clipping at Large Signal
- Support Class AB Output
- Shutdown Current <1μA
- Superior Low Noise without Input
- EMI Suppressing by Soft-Driving
- Short Circuit Protection
- Thermal Shutdown
- Available in Space Saving SOP8 and MSOP8 Pb-Free Package

Application

- Speakers
- Shared-Bikes
- POS
- Telephone Watches
- IPCs
- Portable Devices

Description

The TMS8010 is a mono filter-less class-D amplifier with high SNR and differential input that eliminate noise. With an alternative option between Class-D and Class-AB output, which makes the device very ideal for efficiency-EMI compatible applications.

Features like higher than 90% efficiency and small PCB area make the TMS8010 class-D amplifier ideal for portable devices. The filter-less architecture requires no external output filter, fewer external components, less PCB area and lower system costs, and simplifies application design.

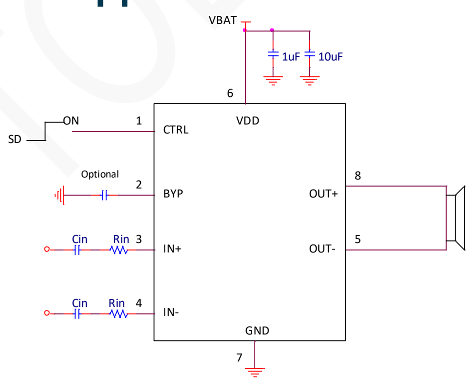
Integrated NCN non-clipping technology suppresses output automatically improving the sound quality and helping to protect the speakers.

With the soft-driving technology, the edge of the PWM at output stage is very flat which is very useful for EMI suppressing.

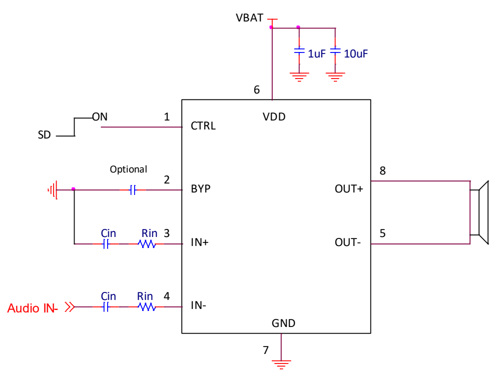
The TMS8010 features short circuit protection, thermal shutdown and under voltage lock-out.

The TMS8010 is available in SOP8L and MSOP8 packages.

Typical Application



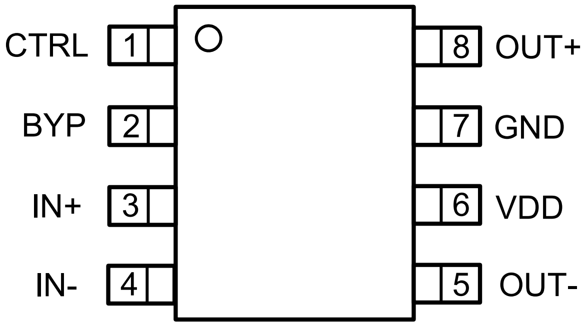
Differential Input



Single-end Input

Figure 1. TMS8010 Typical Application Circuit

Package

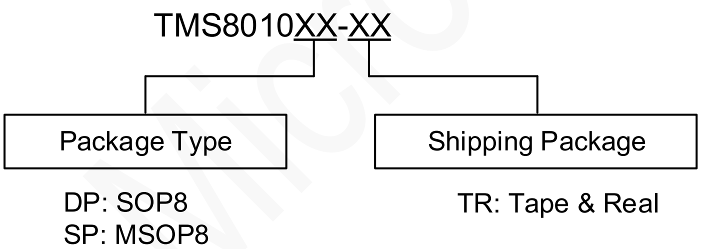


SOP8/MSOP8(Top View)

Order Information

Part Number	Package	Top Marking	Quantity/ Reel
TMS8010DP-TR	SOP8	T8010DP XXXXX	3000
TMS8010SP-TR	MSOP8	T8010SP XXXXX	3000

TMS8010 devices are Pb-free and RoHS compliant.



Pin Functions

Pin	Name	Description
1	CTRL	Control Terminal
2	BYP	Internal Reference Voltage Bypass Pin; Connect a 1.0uF Capacitance from Thins Pin to GND
3	IN+	Positive Differential Input
4	IN-	Negative Differential Input
5	OUT-	Negative BTL Output
6	V_{DD}	Power Supply
7	GND	Ground
8	OUT+	Positive BTL Output

Absolute Maximum Ratings

Items	Rating	Unit
Supply Voltage (V_{DD})	6.5	V
Minimum Output Impedance	3.0	Ω
Input Voltage (IN+, IN-, CTRL)	-0.3 to V_{DD}+0.3	V
Storage Temperature	-65 to 150	°C
Maximum Junction Temperature	150	°C

Recommended Operating Conditions

Items	Min	Max	Unit
Supply Voltage (V_{DD})	2.5	6.0	V
Operating Ambient Temperature Range，T_A	-25	85	V
Junction Temperature Range. (T_J)	-40	125	°C

ESD Rating

Items	Description	Value	Unit
V_{ESD_HBM}	Human Body Model	±4000	V
V_{ESD_CDM}	Charge Device Model	±750	V

Electrical Characteristics

T_A=25°C, V_{DD}=5V, R_{IN}=33kΩ, C_{IN}=0.22μF, R_L=L(33μH)+R+L(33μH), unless otherwise noted.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
Class D Mode							
Po	Output Power	THD+N=10%, f=1kHz, R_L=4Ω	V_{DD}=5.0V		3.2		W
			V_{DD}=3.7V		1.75		
		THD+N=1%, f=1kHz, R_L =4Ω	V_{DD}=5.0V		2.6		W
			V_{DD}=3.7V		1.5		
		THD+N=10%, f=1kHz, R_L =8Ω	V_{DD}=5.0V		1.75		W
			V_{DD}=3.7V		0.95		
		THD+N=1%, f=1kHz, R_L =8Ω	V_{DD}=5.0V		1.50		W
			V_{DD}=3.7V		0.8		
THD+N	Total Harmonic Distortion Plus Noise	V_{DD}=5.0V, Po=0.25W	f=1kHz, R_L =8Ω		0.035		%
		V_{DD}=3.7V, Po=0.25W			0.04		
		V_{DD}=5.0V, Po=0.5W	f=1kHz, R_L =4Ω		0.04		%
		V_{DD}=3.7V, Po=0.5W			0.045		
PSRR	Power Supply Ripple Rejection	V_{DD}=5V, Inputs AC-Grounded	f=217Hz		-65		dB
			f=1kHz		-65		
SNR	Signal-to-Noise Ratio	V_{DD}=5V, THD=1%, f=1kHz	A-weighting		95		dB
Vn	Output Noise	Inputs AC-Grounded, G_V=6dB	No A-weighting		120		μV
			A-weighting		65		
G_V	Closed-loop Gain	V_{DD}= 5V			310K /Rin		V/V
fsw	Switching Frequency	V_{DD}= 5V			350		kHz
η	Efficiency	R_L=8Ω, THD=10%	f=1kHz		93		%
		R_L=4Ω, THD=10%			86		
I_Q	Quiescent Current	V_{DD}=5V	No Load		10		mA
Class AB Mode							
Po	Output Power	THD+N=10%, f=1kHz, R_L =4Ω	V_{DD}=5.0V		3		W
			V_{DD}=3.7V		1.7		
THD+N	Total Harmonic Distortion Plus Noise	V_{DD}=5.0V, Po=0.25W, R_L =8Ω	f=1kHz		0.25		%
		V_{DD}=3.7V, Po=0.25W, R_L =8Ω			0.2		
Vn	Output Noise	Inputs AC-Grounded, G_V=6dB	No A-weighting		60		μV
			A-weighting		110		
I_Q	Quiescent Current	V_{DD}=5V	No Load		12		mA

Electrical Characteristics

T_A=25°C, V_{DD}=5V, R_{IN}=33kΩ, C_{IN}=0.22μF, R_L=L(33μH)+R+L(33μH), unless otherwise noted.

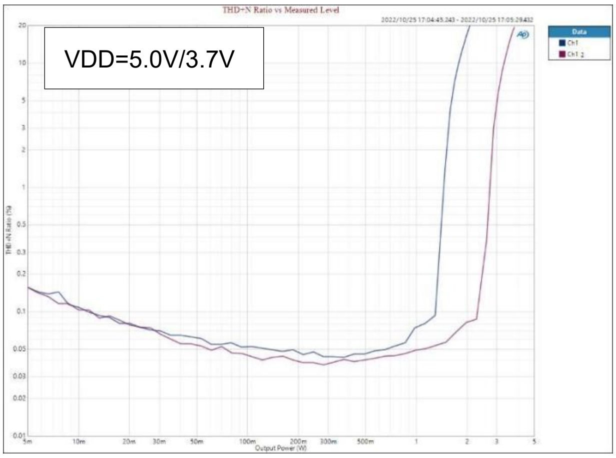
Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
DC Parameters							
I_{SD}	Shutdown Current	V_{DD}=2.8V to 5V	CTRL=0V			1	μA
R_{SDON}	Static Drain-to Source On-state Resistor	High Side + Low Side	V_{DD}=5.0V, I=500mA		355		mΩ
T_{ON}	Turn On Time	V_{DD}= 5V			30		ms
V_{OS}	Output Offset Voltage	Input AC-Ground, V_{DD}=5V			10		mV
V_{IH}	Input High Voltage	V_{DD}=5V		1.4			V
V_{IL}	Input Low Voltage	V_{DD}=5V				1.0	V

Performance Characteristics

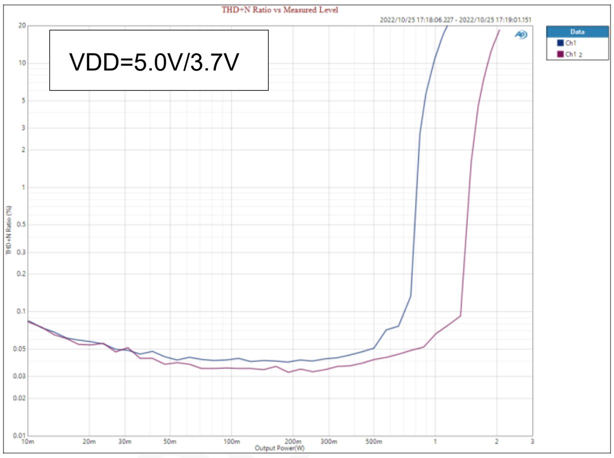
T_A=25°C, V_{DD}=5V, R_{IN}=33kΩ, C_{IN}=0.22μF, R_L=L(33μH)+R+L(33μH), unless otherwise noted.

Class D Mode

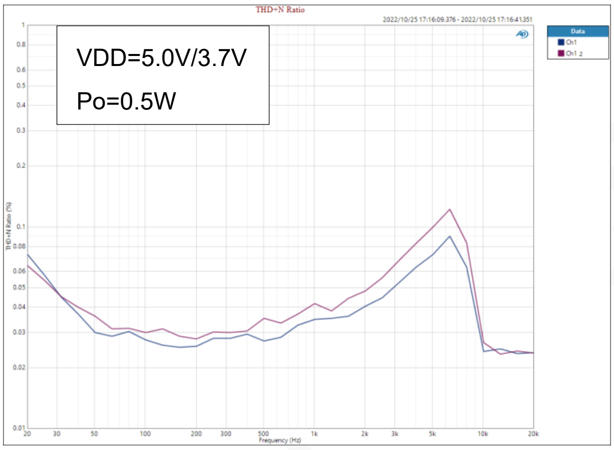
THD+N Vs. Output Power (R_L=4Ω)



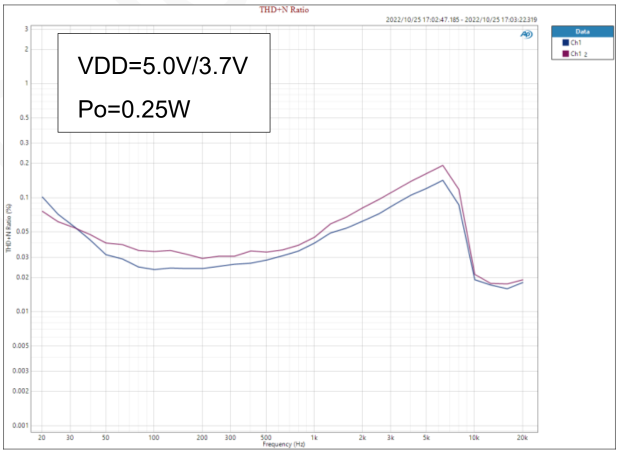
THD+N Vs. Output Power (R_L=8Ω)



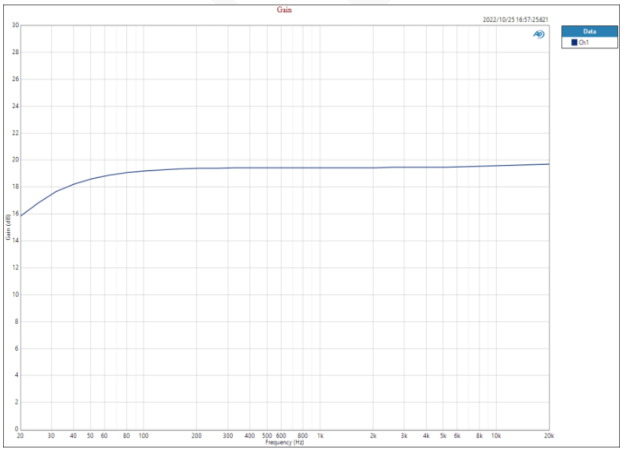
THD+N Vs. Frequency (RL=4Ω)



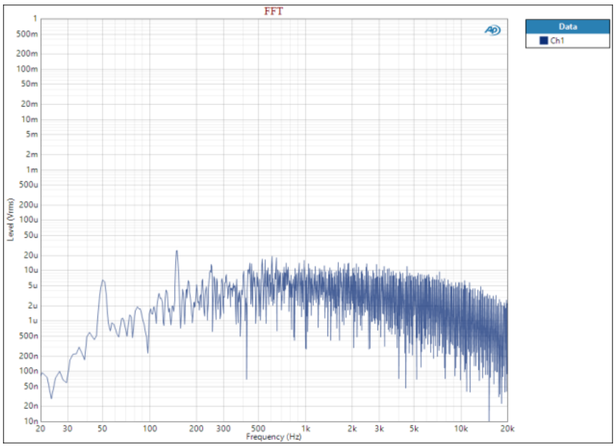
THD+N Vs. Frequency (RL=8Ω)



Frequency Response



Noise Floor

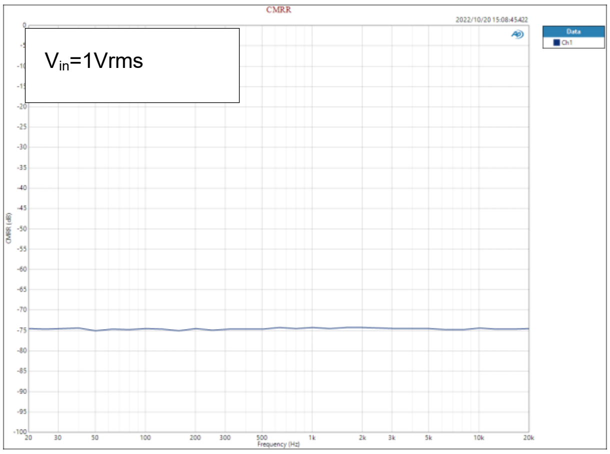


Performance Characteristics

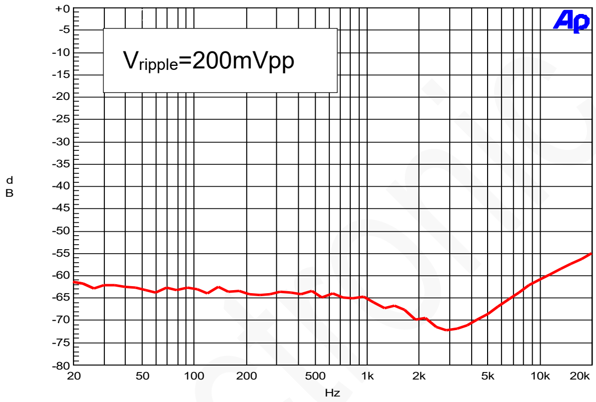
T_A=25°C, V_{DD}=5V, R_{IN}=33kΩ, C_{IN}=0.22μF, R_L=L(33μH)+R+L(33μH), unless otherwise noted.

Class D Mode

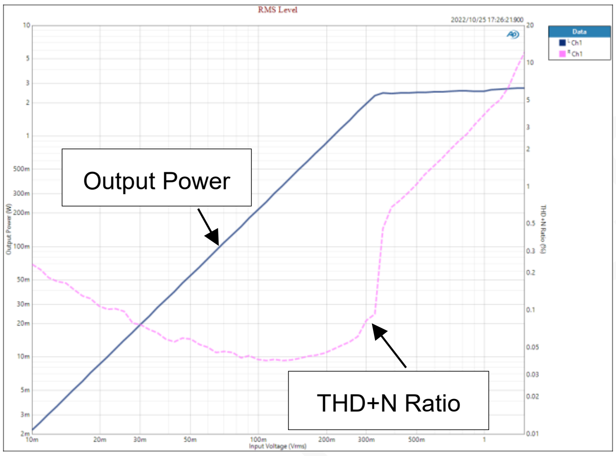
CMRR



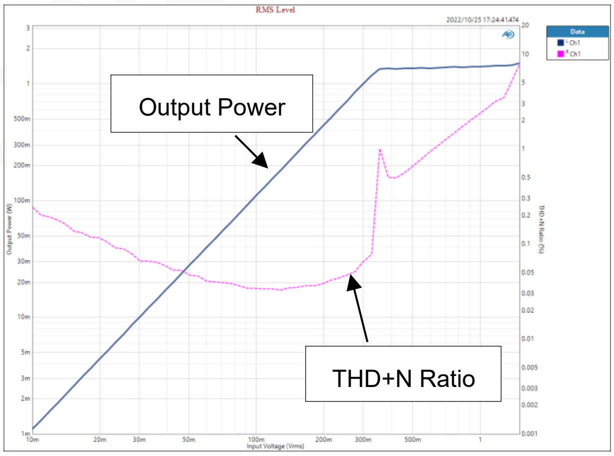
PSRR



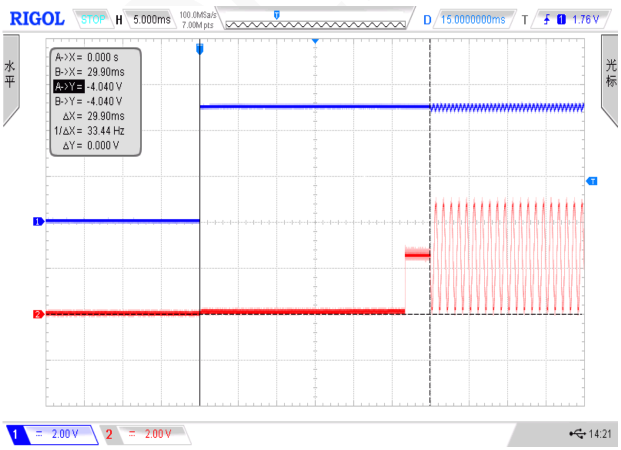
NCN1 Characteristics (RL=4Ω)



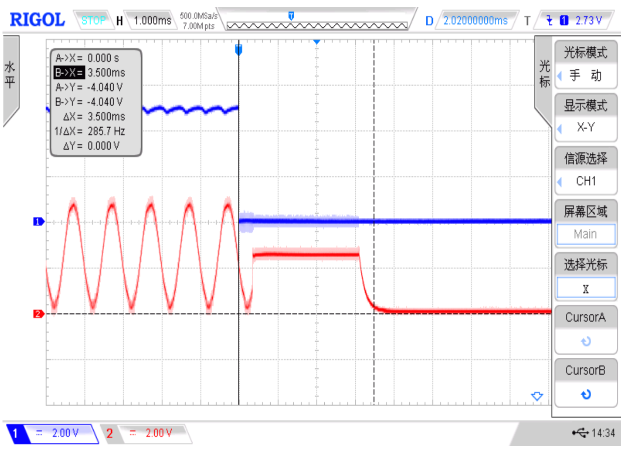
NCN1 Characteristics (RL=8Ω)



Start-up Response



Shutdown Response

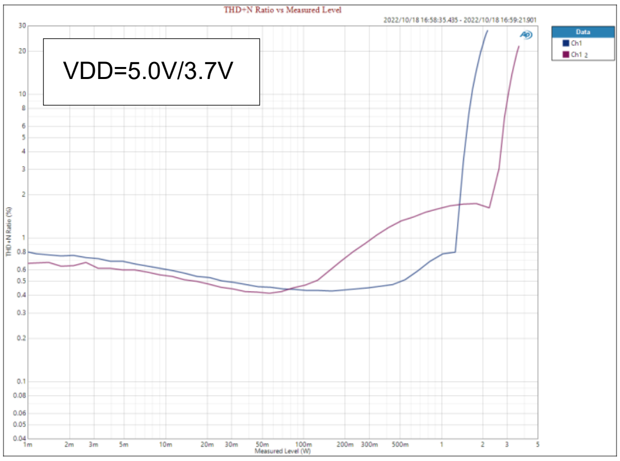


Performance Characteristics

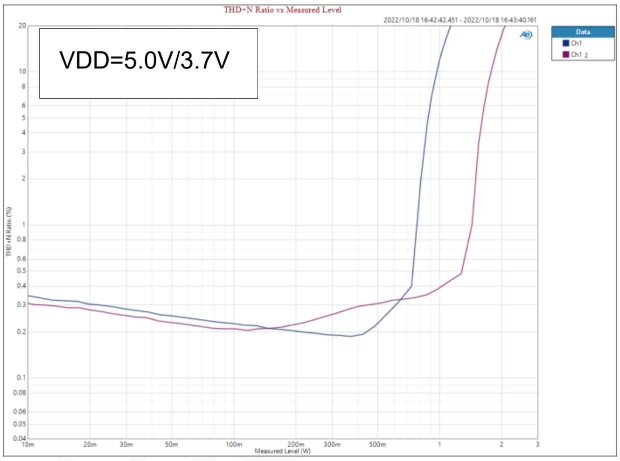
T_A=25°C, V_{DD}=5V, R_{IN}=33kΩ, C_{IN}=0.22μF, unless otherwise noted.

Class AB Mode

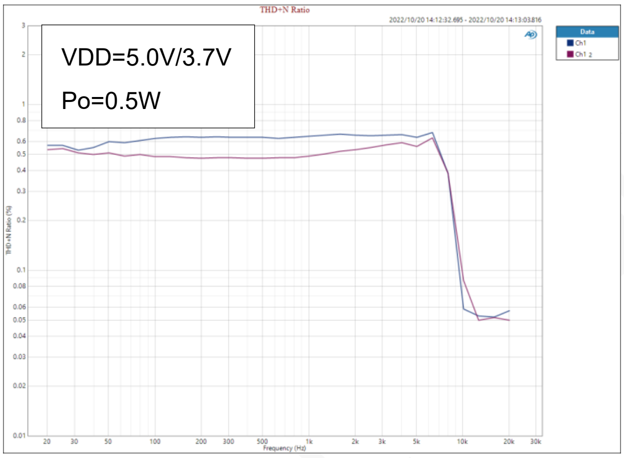
THD+N Vs. Output Power (RL=4Ω)



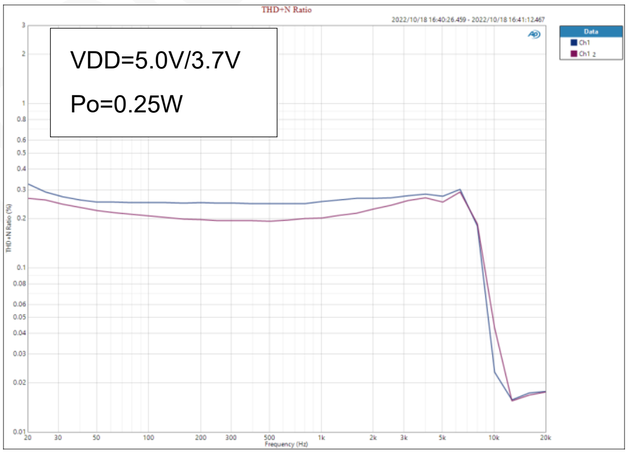
THD+N Vs. Output Power (RL=8Ω)



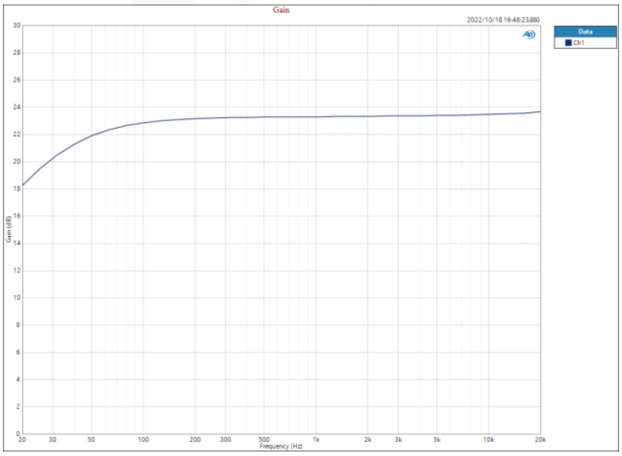
THD+N Vs. Frequency (RL=4Ω)



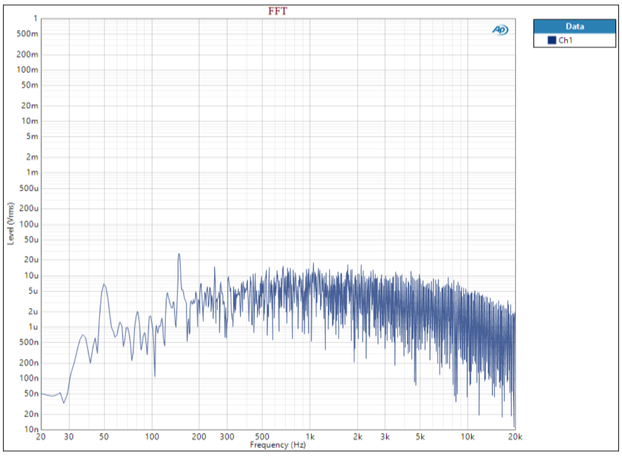
THD+N Vs. Frequency (RL=8Ω)



Frequency Response



Noise Floor



Block Diagram

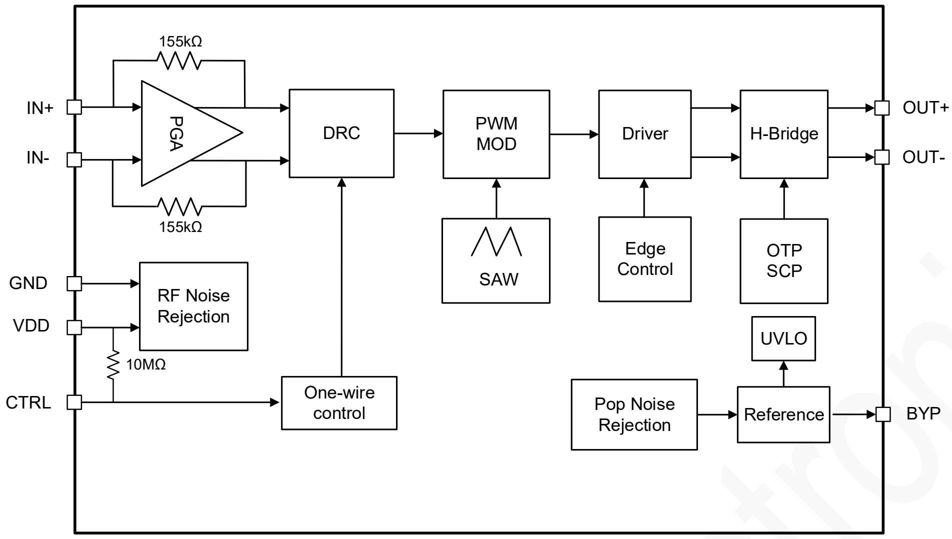


Figure 2: TMS8010 Block Diagram

Application Information

Input Resistor (Ri) and Gain Setting

The input resistors (Ri) and feedback resistors (155kΩ refer to block diagram) internally set the gain of the amplifier according to the following equation.

$$\text{Gain}=\frac{2*155k}{Ri}\ (V/V)$$

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%. Place the input resistors very close to the TMS8010 to limit noise injection on the high-impedance nodes. For optimal performance, the gain should be set to 2V/V or lower. Lower gain allows the TMS8010 to operate at its best, and keeps a high voltage at the input making the inputs less susceptible to noise.

Input Capacitors (Ci)

In the typical application, an input capacitor, Ci, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, Ci and the minimum input impedance Ri form is a high-pass filter with the corner frequency determined in the follow equation:

$$f_C=\frac{1}{(2\pi RiCi)}$$

It is important to consider the value of Ci as it directly affects the low frequency performance of the circuit. For example, when Ri is 150kΩ and the specification calls for a flat bass response are down to 150Hz. Equation is reconfigured as followed:

$$Ci = \frac{1}{(2\pi R_i f_c)}$$

When input resistance variation is considered, the Ci is 7nF, so one would likely choose a value of 10nF. A further consideration for this capacitor is the leakage path from the input source through the input network (Ci, Ri + Rf) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level is held at VDD/2, which is likely higher than the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Decoupling Capacitor (CS)

The TMS8010 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) as low as possible. Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low Equivalent-Series-Resistance (ESR) ceramic capacitor, typically 1μF, is placed as close as possible to the device VDD pin for the best operation. For filtering lower frequency noise signals, a large ceramic capacitor of 10μF or greater placed near the audio power amplifier is recommended.

Analog Reference Bypass Capacitor (C_{BYP})

Analog Reference Bypass Capacitor (C_{BYP}) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the internal analog reference to the amplifier, which appears as degraded PSRR and THD+N. A 1μF capacitance is recommended.

How to Reduce EMI

Most applications require a ferrite bead filter for EMI elimination shown at Figure 3. The ferrite filter reduces EMI around 1MHz and higher. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

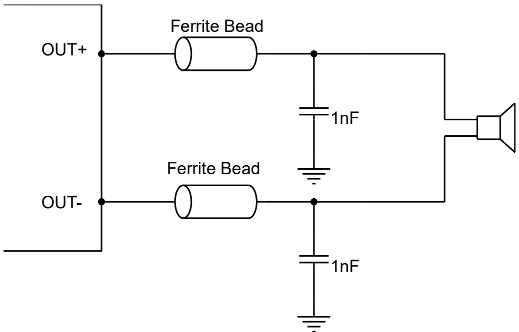


Figure 3: Ferrite Bead Filter to Reduce EMI

Under Voltage Lock-out (UVLO)

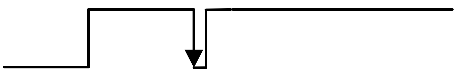
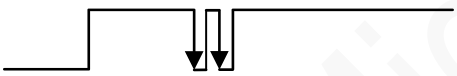
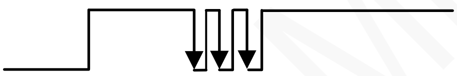
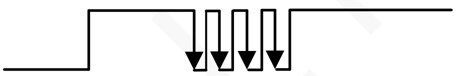
The TMS8010 incorporates circuitry designed to detect low supply voltage. When the supply voltage drops to 2.4V or below, the TMS8010 goes into a state of shutdown, and the device comes out of its shutdown state and restore to normal function only when VDD higher than 2.5V.

Short Circuit Protection (SCP)

The TMS8010 has short circuit protection circuitry on the outputs to prevent the device from damage when output-to-output shorts or output-to-GND shorts occur. When a short circuit occurs, the device immediately goes into shutdown state. Once the short is removed, the device will be reactivated.

CTRL Pin Function

CTRL pin features multi functions.
To achieve high sound quality, the TMS8010 works at non-clipping mode 1(NCN1) once pull CTRL pin voltage to high (power on default), and the chip works at other modes when the serial pulses(one-wire-control) applied to the CTRL pin. Below table shows the TMS8010 behaviors versus CTRL Pin waveform.

CTRL Waveform	TMS8010 Behavior	Note
	Class D with NCN1	Power on default
	Class D with NCN1	One falling edge
	Class D with NCN2	Two falling edges
	Class D without NCN	Three falling edges
	Class AB without NCN	Four falling edges

In order to reduce power consumption while not in use, the TMS8010 contains shutdown circuitry amplifier off when logic low(t_{SD}>10ms) is placed on the CTRL pin. By switching the CTRL pin connected to logic low, the TMS8010 supply current draw will be minimized in idle mode.
Timing of the one-wire-control for the CTRL:

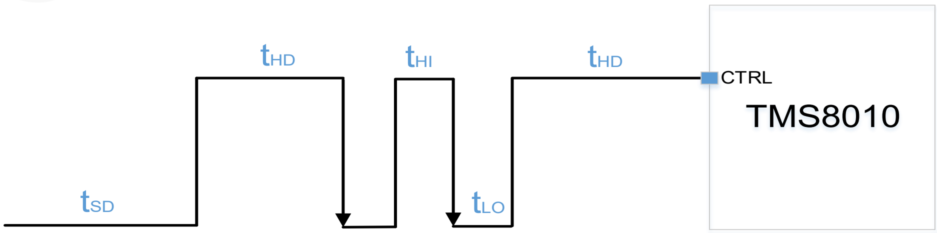


Figure 4: CTRL Pin Timing

a, Hold time t_{HD}>10ms
b, High level time: 20μs <t_{HI}<100μs;

c, Low level time: 20μs <t_{HI}<100μs;

d, Chips shutdown when the t_{LO} more than 10ms(t_{SD});

Non-Clipping Output (NCN)

The TMS8010 provides auto non-clipping control, and the range is from 24dB (Rin=20kΩ) to 9dB. When the output reaches the maximum power value, the internal Programmable Gain Amplifier (PGA) will decrease the gain to prevent the output waveform clipping. This feature prevents the audio sound to be distorted and protects speaker damage from being overstressed. Using the CTRL pin to set the non-clipping Mode 1(NCN1:20ms attack time) and non-clipping Mode 2(NCN2:40ms attack time).

Over Temperature Protection (OTP)

Thermal protection on the TMS8010 prevents the device from damage when the internal die temperature exceeds 150°C. There is a 15°C tolerance on this trip point from device to device. Once the die temperature exceeds the set point, the device will enter the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die decreased by 40°C. This large hysteresis will prevent motor boating sound well and the device begins normal operation at this point with no external system interaction.

POP and Click Circuitry

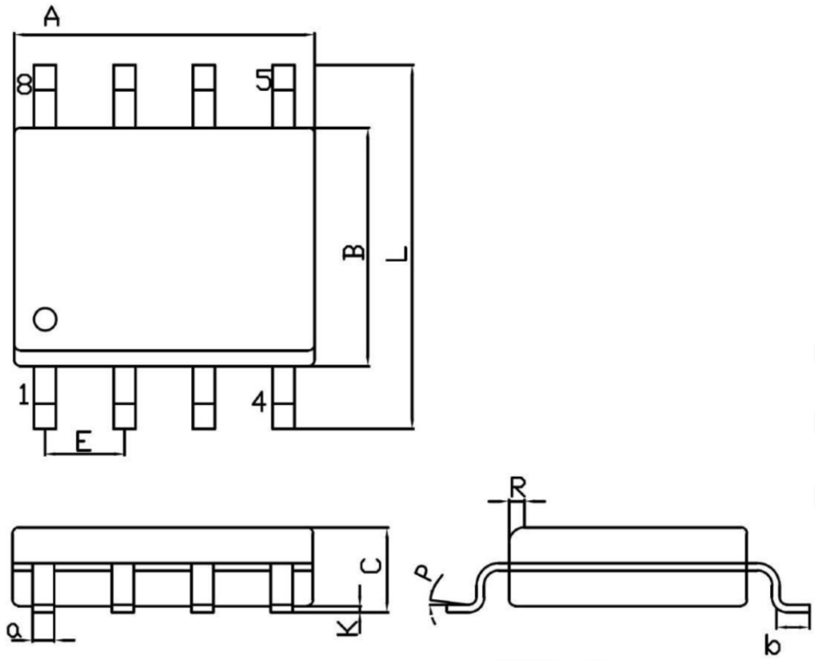
The TMS8010 contains circuitry to minimize turn-on and turn-off transients or “click and pops”, where turn-on refers to either power supply turn-on or device recover from shutdown mode. When the device is turned on, the amplifiers are internally muted. An internal current source ramps up the internal reference voltage. The device will remain in mute mode until the reference voltage reach half supply voltage, 1/2 VDD. As soon as the reference voltage is stable, the device will begin full operation. For the best power-off pop performance, the amplifier should be set in shutdown mode prior to removing the power supply voltage.

Class AB Mode

The chip will operation at Class AB mode to avoid any RF interference when apply serial pulse applied to the CTRL pin. (Please see the CTRL Pin Function)

Tape And Reel Information

Package: SOP8



Unit: mm

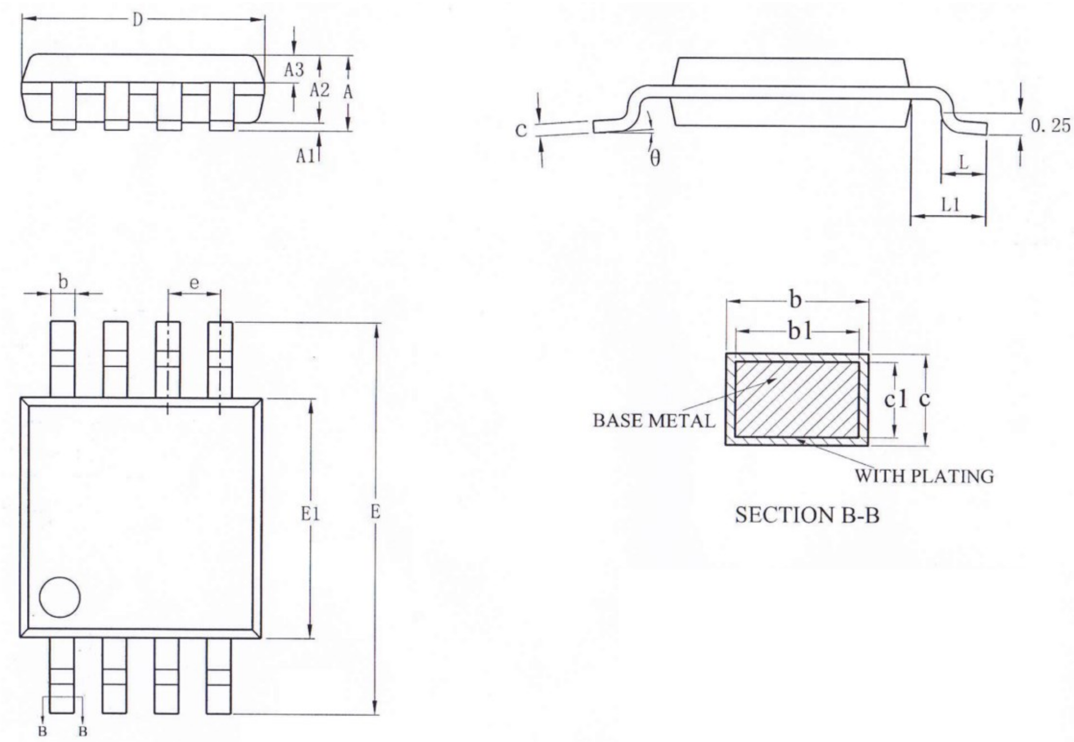
Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min	Max		Min	Max
A	4.70	5.10	C	1.35	1.75
B	3.70	4.10	a	0.35	0.49
L	6.00	6.40	R	0.30	0.60
E	1.27 BSC		P	0°	7°
K	0.12	0.22	b	0.40	1.25

Note:

1) All dimensions are in millimeters.
2) Package length does not include mold flash, protrusion or gate burr.
3) Package width does not include inter lead flash or protrusion.
4) Lead popularity (bottom of leads after forming) shall be 0.10 millimeters max.
5) Pin 1 is lower left pin when reading top mark from left to right.

Tape And Reel Information

Package: MSOP8



Unit: mm

Symbol	Dimensions In Millimeters			Symbol	Dimensions In Millimeters		
	Min	Type	Max		Min	Type	Max
A	-	-	1.10	c1	0.14	0.15	0.16
A1	0.05	-	0.15	D	2.90	3.00	3.10
A2	0.75	0.85	0.95	E	4.70	4.90	5.10
A3	0.30	0.35	0.40	E1	2.9	3.00	3.10
b	0.28	-	0.36	e	0.65 BSC		
b1	0.27	0.30	0.33	L	0.40	-	0.70
c	0.15	-	0.19	L1	0.95 REF		
θ	0	-	8°				

Note:

1) All dimensions are in millimeters.
2) Package length does not include mold flash, protrusion or gate burr.
3) Package width does not include inter lead flash or protrusion.

Important Notification

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