PRIMARY-SIDE REGULATED FLYBACK 80V DCDC CONVERTER

Features

- Supports Primary-Side Regulated Flyback without Opto-Coupler Feedback
- Integrated 160V Switching Power MOSFET
- Internal 80V Start-Up Circuit
- Up to 3A Programmable Current Limit
- Discontinuous Conduction Mode
- OLP, OVP, Open-Circuit, and Thermal Protection
- Flexible Self-Power or External VCC Power
- TMI97153B supports flyback mode with ESOP8 package

Application

- VoIP Telephones
- Security Camera Systems
- WLAN Access Points
- General Flyback Converters

Description

The TMI97153B is a monolithic flyback dc-dc converter with a 160V power switch that targets isolated 13W PoE applications. It supports both primary-side regulated flyback applications. TMI97153B uses fixed peak current and variable frequency discontinuous conduction mode (DCM) to regulate constant output voltage. The primary-side regulation without opto-coupler feedback in flyback mode simplifies the design and saves BOM cost. A 160V integrated power MOSFET optimizes the device for various wide voltage applications. The TMI97153B protection features include overload protection, over-voltage protection, open-circuit protection, and thermal shutdown. The TMI97153B is available in ESOP8 package.

Typical Application

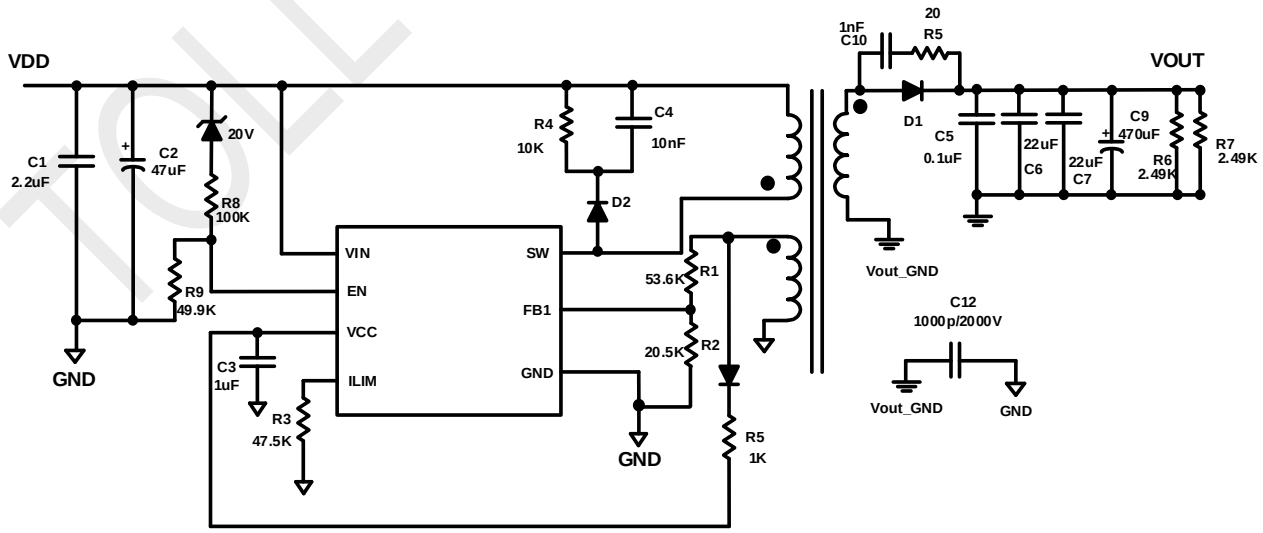


Figure 1. TMI97153B Typical Application Circuit

Absolute Maximum Ratings (Note 1)

Items	Min	Max	Unit
VIN	-0.3	100	V
SW	-0.7	160	V
FB1 (Note 2)	-0.7	5.5	V
All other pins (Note 3)	-0.3	+5.5	V
VCC sinking current (Note 4)		5	mA
FB1 sinking current (Note 2)	-1	1	mA
EN sinking current (Note 5)		1	mA
Continuous power dissipation (TA = +25°C) (Note 6)		2.5	W
Junction Temperature		150	°C
Lead Temperature		260	°C
Storage Temperature	-65	150	°C

Recommended Operating Conditions (Note 7)

Items	Min	Max	Unit
Supply Voltage (V_{IN})	14	80	V
Switching voltage (V_{SW})	-0.5	150	V
Maximum VCC sinking current (Note 4)		3	mA
Maximum FB1 sinking current (Note 2)	-0.5	0.5	mA
Maximum EN sinking current (Note 5)		0.5	mA
Maximum switching frequency		200	kHz
Maximum current limit		3	A
Switching junction temp (T_J)	-40	125	°C

ESD Rating

Items	Description	Value	Unit
$V_{(ESD-HBM)}$	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2017 Classification, Class: 2	±2000	V
$V_{(ESD-CDM)}$	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2018 Classification, Class: C3	±1000	V
$I_{LATCH-UP}$	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±200	mA

JEDEC specification JS-001

Thermal Resistance (Note 8)

Items	Description	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	50	°C/W
θ_{JC}	Junction-to-case(top) thermal resistance	10	°C/W

Notes 1: Exceeding these ratings may damage the device.

Notes 2: Refer to the “Output Voltage Setting” section.

Notes 3: V_{CC} and EN voltage can be pulled higher than this rating, but the external pull-up current should be limited. Refer to “V_{CC} sinking current” and “EN sinking current” ratings to the left.

Notes 4: Refer to the “V_{CC} Power Supply Setting” section.

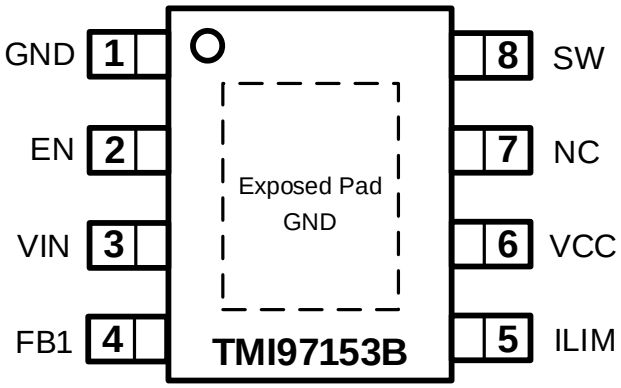
Notes 5: Refer to the “EN Control Setting” section.

Notes 6: The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Notes 7: The device is not guaranteed to function outside of its operating conditions.

Notes 8: Measured on JESD51-7, 4-layer PCB.

Package



ESOP-8

Top Marking: T97153B/XXXXX (T97153B: Device Code, XXXXX: Inside Code)

Order Information

Part Number	Package	Top Marking
TMI97153B	ESOP-8	T97153B XXXXX

TMI97153B devices are Pb-free and RoHS compliant.

Pin Functions

Pin	Name	Function
1	GND	Switching converter power return.
2	EN	Regulator on/off control input. EN can program VIN UVLO start-up through a Zener diode and a resistor divider.
7	NC	No connection. NC is not connected internally. Float NC or connect to GND in layout
3	VIN	Positive power supply terminal.
4	FB1	Feedback for flyback solution.
5	ILIM	IC switching current limit program pin. Connect ILIM to GND through a resistor to program the peak current limit.
6	VCC	Supply bias voltage pin, powered through internal LDO from VIN. It is recommended to connect a capacitor (no less than 1μF) between VCC and GND.
8	SW	Drain of converter switching MOSFET.

Electrical Characteristics

V_{IN} = 48V, V_{EN} = 5V, V_{OUT} = 12V, T_J = -40°C to 125°C, typical value is tested at 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power supply and UVLO						
V_{IN} UVLO rising threshold	V_{IN-R}	V_{IN} rising	10.5	11.5	12.8	V
V_{IN} UVLO falling threshold	V_{IN-F}	V_{IN} falling	7.4	8.1	9	V
V_{CC} regulation (Note9)	V_{CC}	Load = 0 mA to 10 mA	4.3	4.5	4.7	V
V_{CC} UVLO rising threshold (Note9)	V_{CC-R}	V_{IN} is higher than UVLO, V_{CC} rising	3.4	3.6	3.8	V
V_{CC} UVLO falling threshold	V_{CC-F}	V_{IN} is higher than UVLO, V_{CC} falling		3.5		V
Quiescent current	I_Q	V_{FB1} = 2.2V, V_{FB2} =VIN		380		μA
EN high-level voltage			1.7	2	2.35	V
EN low-level voltage				0.9	1.45	V
EN input current				6	8	μA
Voltage feedback						
FB1 reference voltage	V_{REF1}	Respect to GND, T_J = 25°C	1.94	1.99	2.04	V
		Respect to GND, T_J = -40°C to +125°C	1.93	1.99	2.05	V
FB1 leakage current	I_{FB1}	Respect to GND, V_{FB1} = 2V		10	50	nA
Flyback mode DCM detect threshold on FB1	V_{DCM1}	Respect to GND	25	50	75	mV
FB1 open-circuit threshold	$V_{FB1OPEN}$		-80	-50	-20	mV
FB1 OVP threshold	V_{FB1OVP}		120%	125%	130%	V_{REF1}
Minimum diode conduction time for FB1 sample	T_{SAMPLE}		1.4	2.2	3	μs
Switching power device						
On Resistance	R_{ON-SW}	V_{CC} = 4.5V		1		Ω
Current sense						
Current limit	I_{LIMIT}	R_{ILIM} = 51.6 kΩ, L = 47μH		2.3		A
Current leading-edge Blanking time	T_{LEB}			280		ns

Electrical Characteristics

V_{IN} = 48V, V_{EN} = 5V, V_{OUT} = 12V, T_J = -40°C to 125°C, typical value is tested at 25°C, unless otherwise noted.

DCDC converter thermal shutdown						
Thermal Shutdown temperature (Note10)	T_{SD}			160		°C
Thermal Shutdown Hysteresis (Note10)	T_{HYS}			30		°C

Notes 9: The maximum VCC UVLO rising threshold is higher than the minimum VCC regulation in the EC table due to production distribution. However, for one unit, VCC regulation is higher than the VCC UVLO rising threshold. The VCC UVLO rising threshold is about 87 percent of the VCC regulation voltage, and the VCC UVLO falling threshold is about 83 percent of the VCC regulation voltage in one unit.

Notes 10: Guaranteed by design.

Block Diagram

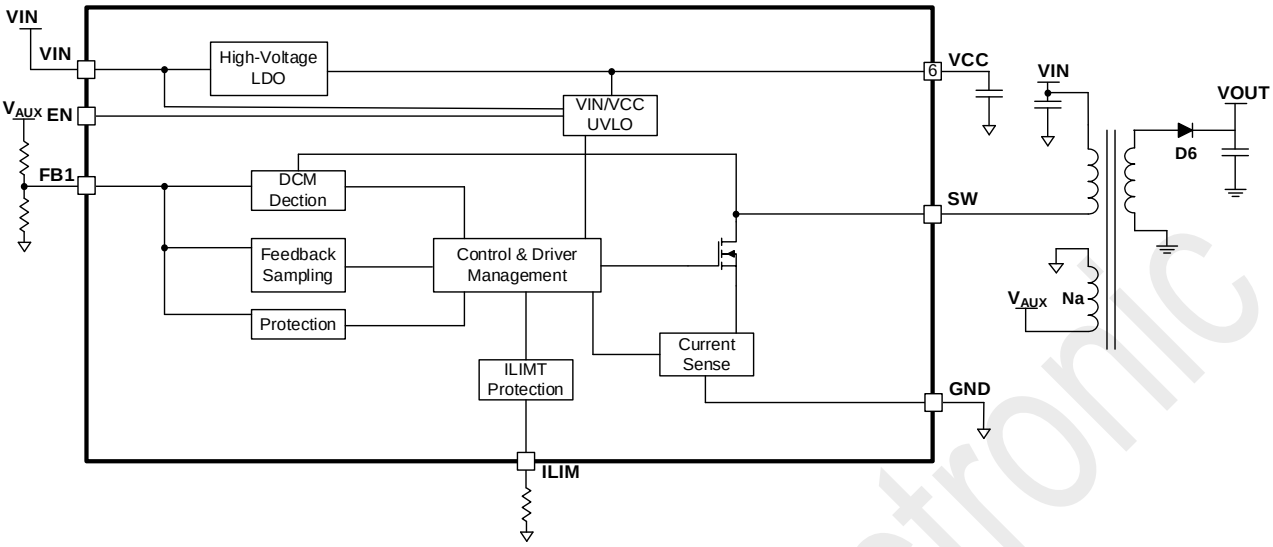


Figure 1. TMI97153B Block Diagram

Operation Description

Start-Up and Power Supply

TMI97153B features an 80V start-up circuit. When V_{IN} is higher than 3.4V, the capacitor at V_{CC} is charged through the internal LDO. Normally V_{CC} is regulated at 4.5V (if VIN is high enough), and the V_{CC} UVLO is 3.6V, typically. With the exception of V_{CC} UVLO, the TMI97153B has an additional 11.5V V_{IN} UVLO. When V_{IN} is higher than the 11.5V UVLO, V_{CC} is charged higher than the 3.6V UVLO, and EN pin is high, TMI97153B starts switching.

V_{CC} can be powered from the transformer auxiliary winding to save IC power loss. Refer to the "V_{CC} Power Supply Setting" section for more details.

Switching Work Principle

After start-up, TMI97153B works in discontinuous conduction mode (DCM). The second switching cycle will not start until the inductor current drops to 0A. In each cycle, the internal MOSFET is turned on, and the current-sense circuit senses the current $I_{P(t)}$ internally.

Use Equation (1) to calculate the rate at which the current rises linearly:

$$\frac{dI_{P(t)}}{dt} = \frac{V_{IN}}{L_M} \quad \text{Equation (1)}$$

When $I_{P(t)}$ rises up to I_{PK}, the internal MOSFET turns off (see Figure 3). The energy stored in the primary-side inductance transfers to the secondary-side through the transformer.

The primary-side inductance (L_M) stores energy in each cycle as a function of Equation (2):

$$E = \frac{1}{2} L_M I_{PK}^2 \quad \text{Equation (2)}$$

Calculate the power transferred from the input to the output with Equation (3):

$$E = \frac{1}{2} L_M I_{PK}^2 F_S \quad \text{Equation (3)}$$

Where F_S is the switching frequency. When I_{PK} is constant, the output power depends on F_S and L_M.

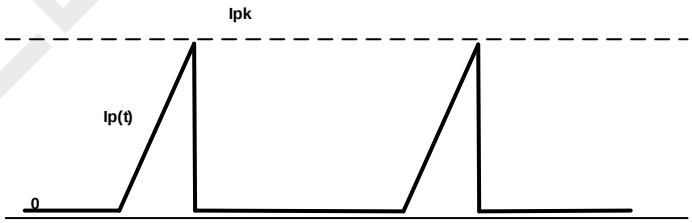


Figure 3 Primary-side current

Light-Load Control

If the load decreases, TMI97153B stretches down the frequency automatically to reduce the power transferring while keeping the same I_{PK} in each cycle. An approximate 10kHz minimum frequency is applied to detect the output voltage even at a very light load. During this condition, the switching I_{PK} jumps between 20 percent of the normal I_{PK} and 100 percent of the normal I_{PK} to reduce the power transferring. The TMI97153B still transfers some energy to the output even if there is no load on the output due to the 20kHz minimum frequency. This means that some load is required to maintain the output voltage, or else VOUT will rise and trigger an OVP.

Frequency Control

By monitoring the auxiliary winding voltage, the TMI97153B detects and regulates the inductor current in DCM. The frequency is controlled by the peak current, the current ramp slew rate, and the load current. The maximum frequency occurs when the TMI97153B runs in critical conduction mode, providing the maximum load power. The TMI97153B switching frequency should be lower than 200kHz in the design.

Voltage Control

The TMI97153B detects the auxiliary winding voltage from FB1 during the secondary-side diode conduction period. Assume the secondary winding is the master, and the auxiliary winding is the slave. When the secondary-side diode conducts, the FB1 voltage is calculated with Equation (4):

$$V_{FB1} = \frac{N_A}{N_S} \times (V_{OUT} + V_F) \times \frac{R_2}{R_1 + R_2} \quad \text{Equation (4)}$$

Where:

V_F is the output diode forward-drop voltage.

V_{OUT} is the output voltage.

N_A and N_S are the turns of the auxiliary winding and the secondary-side winding, respectively.

R1 and R2 are the resistor dividers for sampling.

The output voltage differs from the secondary winding voltage due to the current-dependant diode forward voltage drop. If the secondary winding voltage is always detected at a fixed secondary current, the difference between the output voltage and the secondary-winding voltage is a fixed V_{D1F}. TMI97153B starts sampling the auxiliary-winding voltage after the internal power MOSFET turns off for 0.7μs and finishes the sampling after the secondary-side diode conducts for 3μs. This provides good regulation when the load changes. However, the secondary diode conducting period must be longer than 3μs in each cycle, and the FB1 signal must be smooth in 0.7μs after the switch turns off.

Programming the Switching Current Limit

The TMI97153B current limit is set by an external resistor (R3) from I_{LIM} to ground. The value of R3 can be estimated with Equation (5):

$$I_{LIM} = \frac{110}{R_3} + \frac{V_L \times 0.016}{L} \quad \text{Equation (5)}$$

Where I_{LIM} is the current limit in A, V_L is the voltage applied on the inductor when the MOSFET turns on, R6 is the setting resistor in kΩ, and L is the inductor in μH.
The current limit cannot be programmed higher than 3A.

Leading-Edge Blanking

Transformer parasitic capacitance induces a current spike on the switching power FET when the power switch turns on. The TMI97153B includes a 280ns leading-edge blanking period to avoid falsely terminating the switching pulse. During this blanking period, the current sense comparator is disabled, and the gate driver cannot switch off.

DCM Detection

The TMI97153B regulator operates in discontinuous conduction mode in flyback. The TMI97153B detects the falling edge of the FB1 voltage in each cycle. The second cycle switching will not start unless the chip detects a 50mV falling edge on FB1.

Over-Voltage & Open-Circuit Protection

The TMI97153B includes over-voltage protection (OVP) and open-circuit protection. If the voltage at FB1 exceeds 125 percent of V_{REF1}, or FB1's -60mV falling edge cannot be detected because the feedback resistor is removed, immediately the TMI97153B shuts off the driving signal and enters hiccup mode by re-charging the internal capacitor. The TMI97153B resumes normal operation when the fault is removed.

Over-Load Protection

TMI97153B will always work in DCM mode for any condition. The secondary-side diode conduction duty cycle is limited to about 80 percent. In an over-load condition, the output energy is limited by I_{PK} and F_S. With a heavier load, the output drops and the diode conduction period become longer. This causes the switching frequency to drop so that the output energy can be limited. The TMI97153B has same protection logic for an over-load/output-short condition.

Thermal Shutdown

When the junction temperature exceeds 160°C, the TMI97153B shuts down. Once the temperature drops below 130°C, the part re-starts automatically.

APPLICATION INFORMATION

EN Control Setting

TMI97153B turns on when EN goes high, and it turns off when EN goes low. EN is pulled low internally by an approximate 0.9MΩ resistor.

The maximum on time is limited at about 8μs. The secondary-side rectifier diode conduction time should be longer than 3μs for FB1 feedback sampling. If V_{IN} decreases and the inductor current cannot ramp the I_{PK} to setting value within the maximum on time, the diode conduction time decreases to less than 3μs, causing FB1 feedback sample failure. The TMI97153B treats this failure as a V_{OUT} drop and generates more pulses, causing V_{OUT} to overshoot.

In this condition, EN can be used to program V_{IN} UVLO and shuts down the part before V_{IN} drops (triggering the maximum on time). Since the EN high-level voltage is 2V and the low-level voltage is 0.9V, it is hard to program the V_{IN} UVLO with a small hysteresis. In this condition, one resistor divider and one Zener diode is recommended (see Figure 4).

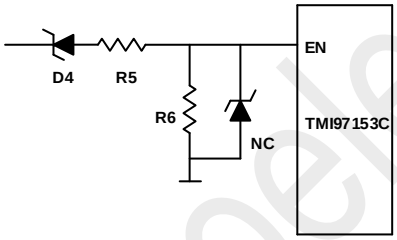


Figure 4. V_{IN} UVLO setting with EN control

For example, the TMI97153B should be turned on before V_{IN} rises to 36 V and shut down before V_{IN} drops to 20V. One 20V Zener diode (D4) and a resistor divider (R5 = 100kΩ/R6 = 49.9kΩ) can be selected to program the V_{IN} UVLO. The programmed VIN rising threshold can be calculated with Equation (6):

$$V_{IN\_R} < 20V + \frac{100k\Omega+49.9k\Omega}{49.9k\Omega} \times 1.7 = 25.1V \quad \text{Equation (6)}$$

The programmed V_{IN} falling threshold is calculated with Equation (7):

$$V_{IN\_F} > 20V + \frac{100k\Omega+49.9k\Omega}{49.9k\Omega} \times 1.45 = 24.3 \quad \text{Equation (7)}$$

If using a resistor divider (see Figure 4) and VEN is higher than 5.5V, there should be place a Zener diode on EN pin, which clamps the EN voltage to prevent runaway.

V_{CC} Power Supply Setting

The V_{CC} voltage is charged through the internal LDO by VIN. Normally, V_{CC} is regulated at 5.4V, typically. A capacitor no less than 1μF is recommended for decoupling between V_{CC} and GND. In flyback mode, V_{CC} can be powered from the transformer auxiliary winding to save the high voltage LDO power loss. The auxiliary winding supply voltage can be calculated with Equation (8):

$$V_{CC} = \frac{N_A}{N_S} \times (V_{OUT} + V_{D1F}) - V_{D3F} \quad \text{Equation (8)}$$

Where N_A and N_S are the turns of the auxiliary winding and the output winding, V_{D1F} is the output rectifier diode voltage drop, and V_{D3F} is the D3 voltage drop in Figure 5.

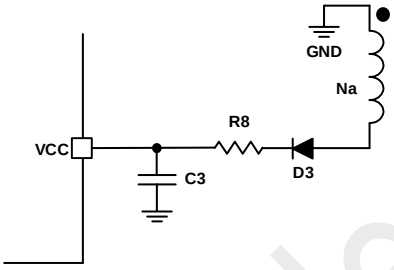


Figure 5 Supply V_{CC} from auxiliary winding

V_{CC} voltage is clamped at about 5V by one internal Zener diode. The clamp current capability is about 3mA. If the auxiliary winding power voltage is higher than 5.5V (especially in a heavy-load condition), a series resistor (R8) is necessary to limit the current to V_{CC}. For simple application, supply the V_{CC} power through the internal LDO directly.

Output Voltage Setting

The converter detects the auxiliary winding voltage from FB1. R1 and R2 are the resistor dividers for the feedback sampling (see Figure 6).

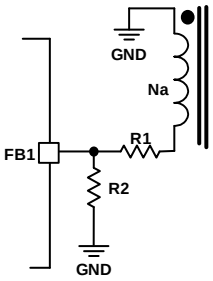


Figure 6 Feedback in isolation application

When the primary-side power MOSFET turns off, the auxiliary-winding voltage is sampled.
The output voltage is estimated Equation (9) :

$$V_{OUT} = \frac{V_{REF1} \times (R_1 + R_2)}{R_2} \times \frac{N_S}{N_A} - V_{D1F} \qquad \text{Equation (9)}$$

Where, N_S is the transformer secondary-side winding turns.
N_A is the transformer auxiliary winding turns.
V_{D1F} is the rectifier diode forward drop.
V_{REF1} is the reference voltage of FB1 (1.99V, typically).
When the primary-side power MOSFET turns on, the auxiliary winding forces a negative voltage to FB1. The FB1 voltage is clamped to less than -0.7V internally, but the clamp current should be limited to less than -0.5mA by R1. For example, if the auxiliary winding forces -11V to R1, to make the current flowing from FB1 to R1 lower than -0.5mA, R1 resistance must be higher than 22kΩ (if ignoring R2 current). Generally, select R2 with a 10kΩ to 50kΩ resistor to limit noise and provide an appropriate R1 for the -0.5mA negative current limit.

Maximum Switching Frequency

When TMI97153B works in DCM, the frequency reaches its maximum value during a full-load condition. The maximum frequency is affected by the peak current limit, the inductance, and the input/output voltage. Generally, design the maximum frequency must be lower than 200kHz.

Design the maximum frequency with the minimum input voltage and the maximum load condition. Calculate the frequency with Equation (10):

$$F_{SW} \le \frac{1}{T_{ON} + T_{CON} + T_{DELAY}} \quad \text{Equation (10)}$$

Where:

T_{ON} is the MOSFET one pulse turn-on time determined with Equation (11):

$$T_{ON} = \frac{I_{LIM} \times L_M}{V_{IN}} \quad \text{Equation (11)}$$

L_M is the transformer primary-winding inductance.

T_{CON} is the rectifier diode current conducting time and can be calculated Equation(12):

$$T_{CON} = \frac{N_S \times I_{LIM} \times L_M}{N_P \times (V_{OUT} + V_{D1F})} \quad \text{Equation (12)}$$

Where, N_S is the transformer secondary-side winding turns. N_P is the transformer primary side winding turns.

T_{DELAY} is the resonant delay time from the rectifier diode current drop to 0A to the auxiliary-winding voltage drop to 0V. The resonant time can be tested on the board (estimate around 0.5μs).

The DCDC converter samples the feedback signal within 3μs after the primary- side MOSFET turns off. The secondary-side diode conduction time in Equation (12) should be higher than 3μs. This time period, combined with the duty cycle, determines the maximum frequency.

Input Capacitor Selection

An input capacitor is required to supply the AC ripple current to the inductor while limiting noise at the input source. A low ESR capacitor is required to keep the noise to the IC at a minimum. Ceramic capacitors are preferred, but tantalum or low ESR electrolytic capacitors will suffice. For ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The ripple will be the worst at light load. The required input capacitance can be estimated (13):

$$C_1 = \frac{0.5 \times I_{LIM} \times T_{ON}}{V_{INP\_P}} \quad \text{Equation (13)}$$

Where C1 is the DCDC converter input bulk capacitor value, V_{INP-P} is the expected input ripple, and T_{ON} is the MOSFET turn-on time.

In an isolated application, T_{ON} is calculated Equation (14):

$$T_{ON} = \frac{I_{LIM} \times L_M}{V_{IN}} \quad \text{Equation (14)}$$

Output Capacitor Selection

The output capacitor maintains the DC output voltage. For best results, use ceramic capacitors or low ESR capacitors to minimize the output voltage ripple. For ceramic capacitors, the capacitance dominates the impedance at the switching frequency.

In flyback application, the worst output ripple occurs under a light-load condition; the worst output ripple can be estimated (15):

$$V_{OUTP\_P} = \frac{0.5 \times N_P \times I_{LIM} \times T_{CON}}{N_S \times C2} \quad \text{Equation (15)}$$

Where, C2 is the output capacitor value. V_{OUTP-P} is the output ripple.

Normally, a 44μF or higher ceramic capacitor is recommended as the output capacitor. This allows a small Vo ripple and stable operation.

Leakage Inductance

The transformer's leakage inductance decreases system efficiency and affects the output current and voltage precision. Optimize the transformer structure to minimize the leakage inductance. Aim for a leakage inductance less than 3 percent of the primary winding inductance.

RCD Snubber for Flyback

The transformer leakage inductance causes spikes and excessive ringing on the MOSFET drain voltage waveform, affecting the output voltage sampling 0.7μs after the MOSFET turns off. The RCD snubber circuit limits the SW voltage spike (see Figure 7).

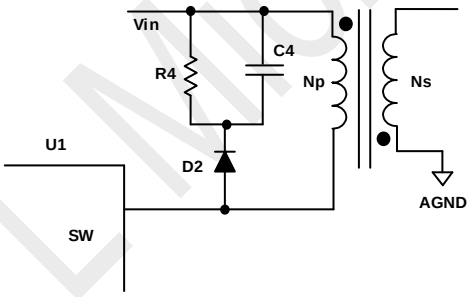


Figure 7 RCD snubber

The power dissipation in the snubber circuit is estimated with Equation (16):

$$P_{SN} = \frac{1}{2} \times L_K \times I_{LIM}^2 \times F_S \quad \text{Equation (16)}$$

Where, L_K is the leakage inductance.

Since R4 consumes the majority of the power, R4 is estimated with Equation (17):

$$R_4 = \frac{V_{SN}^2}{P_{SN}} \quad \text{Equation (17)}$$

Where, V_{SN} is the expected snubber voltage on C4.

The snubber capacitor C4 can be designed to get appropriate voltage ripple on the snubber using Equation (18):

$$\Delta V_{SN} = \frac{V_{SN}}{R_4 \times C_4 \times F_S}$$ Equation (18)

Generally, a 15 percent ripple is acceptable.

Converter Output Diode Selection

The output rectifier diode supplies current to the output capacitor when the internal MOSFET is off. Use a schottky diode to reduce loss due to the diode forward voltage and recovery time.
In isolation application, the diode should be rated for a reverse voltage greater than Equation (19):

$$V_{D1} = V_{OUT} + \frac{V_{IN} \times N_S}{N_P} + V_{PD1}$$ Equation (19)

V_{PD1} can be selected at 40 percent to 100 percent of V_{OUT} + V_{IN} x N_S/N_P. An RCD snubber circuit for the output diode D1 is recommended. The current rating should be higher than the maximum output current.

Dummy Load

When the system operates without a load in flyback mode, the output voltage rises above the normal operation voltage because of the minimum switching frequency limitation. Use a dummy load for good load regulation. A large dummy load decreases efficiency, so the dummy load is a tradeoff between efficiency and load regulation.

PCBoard Layout Consideration

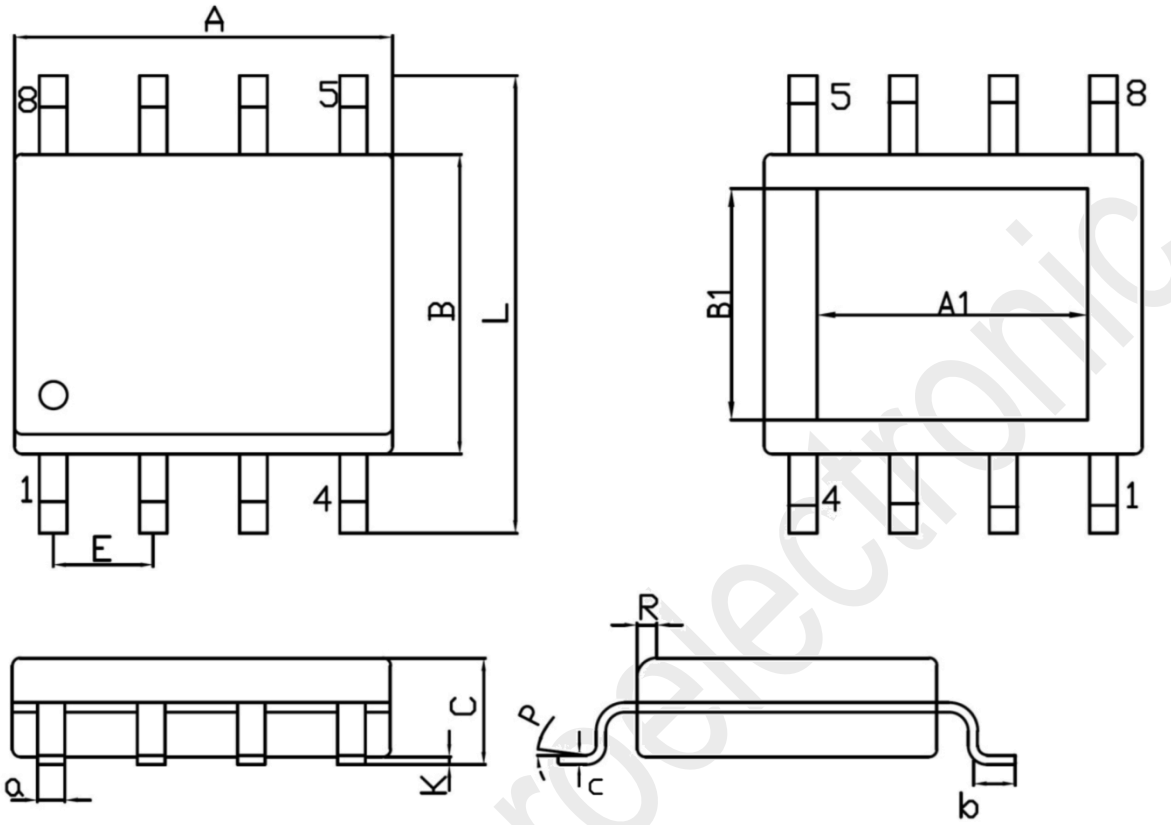
Efficient PCB layout for high-frequency switching power supplies is critical. Poor layout may result in reduced performance, excessive EMI, resistive loss, and system instability.

For flyback application:

1. Keep the input loop as short as possible between the input capacitor, transformer, SW, and GND plane for minimal noise and ringing.
2. Keep the output loop between the rectifier diode, the output capacitor, and the transformer as short as possible.
3. Keep the clamp loop circuit between Diode, Capacitor, and the transformer as small as possible.
4. Place the V_{CC} capacitor close to V_{CC} for the best decoupling. The current setting resistor R3 should be placed as close to I_{LIM} and AGND as possible.
5. Keep the feedback trace far away from noise sources (such as SW). The trace connecting FB1 should be short.
6. Use a single point connection between power GND and signal GND. Vias around GND and the thermal pad are recommended to lower the die temperature.

Tape And Reel Information

ESOP-8



Unit: mm

Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min	Max		Min	Max
A	4.70	5.10	C	1.30	1.75
B	3.70	4.10	a	0.35	0.49
L	5.80	6.40	R	0.30	0.60
E	1.27 BSC		P	0°	7°
K	0.02	0.15	b	0.40	1.25
A1	3.1	3.5	B1	2.2	2.6
			c	0.203	0.243

Note:

1) All dimensions are in millimeters.

2) Package length does not include mold flash, protrusion or gate burr.

3) Package width does not include inter lead flash or protrusion.

Important Notification

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