24V, 8A High Efficiency Synchronous Step-down Converter

Features

- Wide Input Voltage Range: 4.5V to 24V
- Integrated 20mΩ and 10mΩ MOSFETs
- 8A Output Current Capability
- Advanced ACOT Control Architecture for Fast Transient Response
- ±1% Reference Voltage Accuracy
- 500kHz Switching Frequency
- Adjustable Output Voltage Application
- PFM/FPWM Selectable Light Load Operation Mode
- Output Discharge Function
- Power Good Indicator
- Cycle-by-cycle Valley and Peak Current Limit Protection
- Auto-recovery Mode Output OV、UV and OT Protections
- Available in QFN2.5x2.5-16 Package

Application

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Notebook
- Hight Power AP

Description

The TMI3388A is a high integrated synchronous step-down converter with up to 8A output current capability and input voltage range from 4.5V to 24V. TMI3388A adopts advance ACOT control architecture, which provides stable operation and has fast transient response performance without complex compensation and low ESR ceramic capacitors.

TMI3388A's output voltage can be adjusted by configuring a divider resistor in the FB pin to meet different output requirements. In addition, TMI3388A integrates very low $R_{DS(ON)}$ MOSFETs and provide excellent efficiency over a range of applications, especially for low output voltages and low duty cycles.

TMI3388A also integrates a bypass switch which allows the IC to be powered by external DC source to reduce power consumption. Robust protections are integrated in TMI3388A including cycle-by-cycle current limit, internal soft-start, output OVP and UVP, input UVLO and OTP functions.

TMI3388A is available in QFN2.5x2.5-16 package.

Typical Application

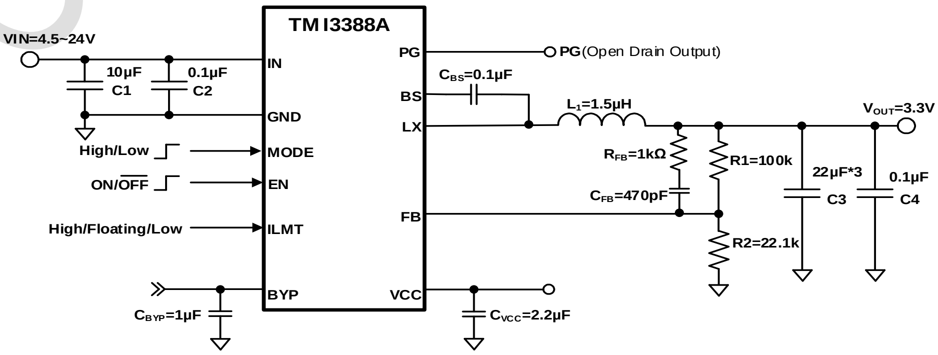
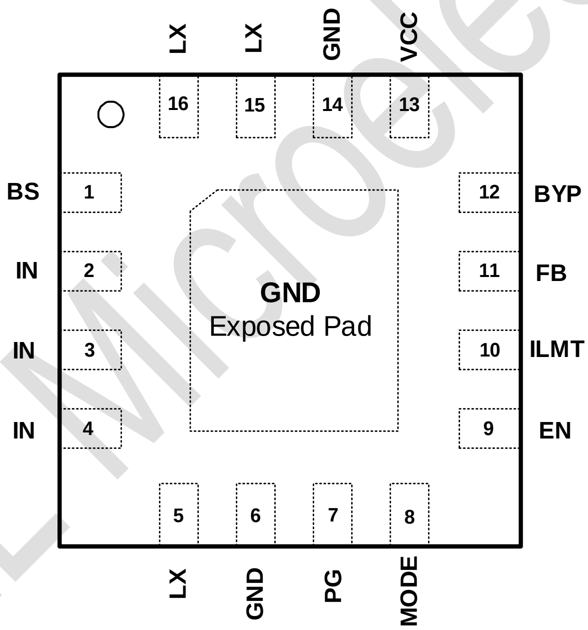


Figure 1. TMI3388A Typical Application Circuit

Absolute Maximum Ratings (Note 1)

Parameter	Min	Max	Unit
Input Supply Voltage	-0.3	26	V
LX, PG, EN, MODE Voltage	-0.3	26	V
LX Voltages (<10ns transient)	-5	28	V
LX Voltages (<30ns transient)	-1	28	V
BS to LX, VCC Voltage	-0.3	6	V
FB, BYP, ILMT Voltage	-0.3	6	V
Storage Temperature Range	65	150	°C
Junction Temperature (Note2)	40	150	°C
Power Dissipation	-	3	W
Lead Temperature (Soldering, 10s)	-	260	°C

Package



Top View

QFN2.5x2.5-16

Top Marking: TA8/XXX (TA8: Device Code, XXX: Inside Code)

Order Information

Part Number	Package	Top Marking	Quantity/Reel
TMI3388A	QFN2.5x2.5-16	TA8 XXX	3000

TMI3388A devices are Pb-free and RoHS compliant.

Pin Functions

Pin	Name	Function
1	BS	Bootstrap. A 0.1µF capacitor connected between LX and BS pins is required to form a floating supply across the high-side switch driver.
2, 3, 4	IN	Input power supply pins. The decoupling ceramic capacitors should be placed as close as possible from this pin to GND for better noise rejection.
5, 15, 16,	LX	Switching pins. Connect to the power inductor.
6, 14	GND	Power ground pins.
7	PG	Power good indicator output pin. Open drain output when the output voltage is within 83% to 120% of the regulation.
8	MODE	Operating mode selection under light load. Pull this pin low for PFM operating and pull this pin high for FPWM operation. Do not leave this pin floating.
9	EN	Drive this pin to a logic-high to enable the Buck regulator. Pull this pin to high to turn on the Buck. Do not leave this pin floating.
10	ILMT	Output current limit threshold selection.
11	FB	Output feedback pin. Connect to the center point of resistor divider.
12	BYP	External 5V bypass power supply input. Decouple this pin to GND with a 1µF ceramic capacitor. Leave this pin floating if it is not used.
13	VCC	Internal 5V LDO output. Power supply for internal analog circuits and driving circuit. Decouple this pin to GND with a 2.2µF ceramic capacitor.
Exposed Pad	GND	Power ground pin.

ESD Rating (Note3)

Items	Description	Value	Unit
V_{ESD_HBM}	Human Body Model for all pins	±2000	V
V_{ESD_CDM}	Charged Device Model for all pins	±500	V

JEDEC specification JS-001

Recommended Operating Conditions

Items	Description	Min	Max	Unit
Voltage Range	IN	4.5	24	V
T_J	Operating Junction Temperature	-40	125	°C
T_A	Operating Ambient Temperature	-40	85	°C

Thermal Resistance (Note4)

Items	Description	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	33	°C/W
θ_{JC}	Junction-to-case(top) thermal resistance	5.5	°C/W
ψ_{JC}	Junction-to-case(top) characterization parameter	0.5	°C/W

Electrical Characteristics

V_{IN}=12V, V_{OUT}=3.3V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Range		4.5		24	V
V_{UVLO}	Input UVLO Threshold	V_{IN} rising			4.5	V
V_{UVLO_HYS}	UVLO Hysteresis			500		mV
I_Q	Quiescent Current	PFM, I_{OUT}=0A, V_{OUT}=V_{SET}×105%		140		μA
I_{SHDN}	Shutdown Current	EN=0V		4	10	μA
V_{REF}	Feedback Reference Voltage		0.594	0.600	0.606	V
I_{FB}	FB Input Current	V_{FB}=1V	-50		50	nA
$R_{DS(ON)1}$	Top FET $R_{DS(ON)}$			20		mΩ
$R_{DS(ON)2}$	Bottom FET $R_{DS(ON)}$			10		mΩ
I_{DIS}	Output Discharge Current	V_{OUT}=5V		100		mA
I_{LMT_TOP}	Top FET Current Limit		16			A
I_{LMT_BOT}	Bottom FET Current Limit	ILMT=Low	8			A
		ILMT=Floating	12			A
		ILMT=High	16			A
I_{LMT_RVS}	Bottom FET Reverse Current Limit	FPWM mode		4.4		A
t_{SS}	Soft-start Time	V_{OUT} from 0% to 100% V_{SET}		1.2		ms
V_{EN_H}	EN Input Voltage High		0.8			V
V_{EN_L}	EN Input Voltage Low				0.4	V
V_{MODE_PFM}	MODE Voltage for PFM Mode		0		0.4	V
V_{MODE_FPWM}	MODE Voltage for FPWM Mode		1		V_{IN}	V
$I_{EN/MODE}$	EN/MODE Input Current	V_{EN}/V_{MODE}=3.3V			1	μA
F_{SW}	Switching Frequency	V_{OUT}=5V, CCM	400	500	600	kHz
t_{ON_MIN}	Min ON Time	V_{IN}=V_{IN_MAX}(Note 5)		50		ns
t_{OFF_MIN}	Min OFF Time			150		ns
V_{CC}	VCC Output Voltage	VCC adds 1mA load	4.8	5	5.2	V
V_{OVP}	Output OVP Threshold	V_{FB} rising	117	120	123	%V_{REF}
t_{OVP_DLY}	Output OVP Delay	(Note 5)		40		μs
V_{UVP}	Output UVP Threshold	V_{FB} falling	55	60	65	%V_{REF}
t_{UVP_DLY}	Output UVP Delay	(Note 5)		300		μs
V_{PG}	Power Good Threshold	V_{FB} falling (Not good)	80	83	86	%V_{REF}
V_{PG_HYS}	Power Good Hysteresis	V_{FB} rising (Good)		7		%V_{REF}
t_{PG_R}	Power Good Delay	Low to High(Note 5)		200		μs
t_{PG_F}		High to Low(Note 5)		40		μs
V_{PG_LOW}	Power Good Low Voltage	V_{FB}=0V, I_{PG}=5mA			0.45	V
$R_{DS(ON)\_BYP}$	LDO Output Current Limit			1.2		Ω
V_{BYP}	Bypass Switch Turn-on Voltage Bypass Switch Hysteresis		4.5	4.7	4.9	V

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{BYP_HYS}	Bypass Switch Turn-on Voltage Bypass Switch Hysteresis			0.2		V
V_{BYP_OVP}	Bypass Switch OVP Voltage	V_{OUT} sweeps	114	120	126	%V_{LDO}
T_{OTP}	Buck OTP Threshold	T_J rising		160		°C
T_{HYS}	Buck OTP Hysteresis	T_J falling		25		°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + P_D \times \theta_{JA}$.

Note 3: Devices are ESD sensitive. Handling precaution is recommended.

Note 4: Measured on a four-layer TOLL Evaluation Board.

Note 5: Guaranteed by design.

Block Diagram

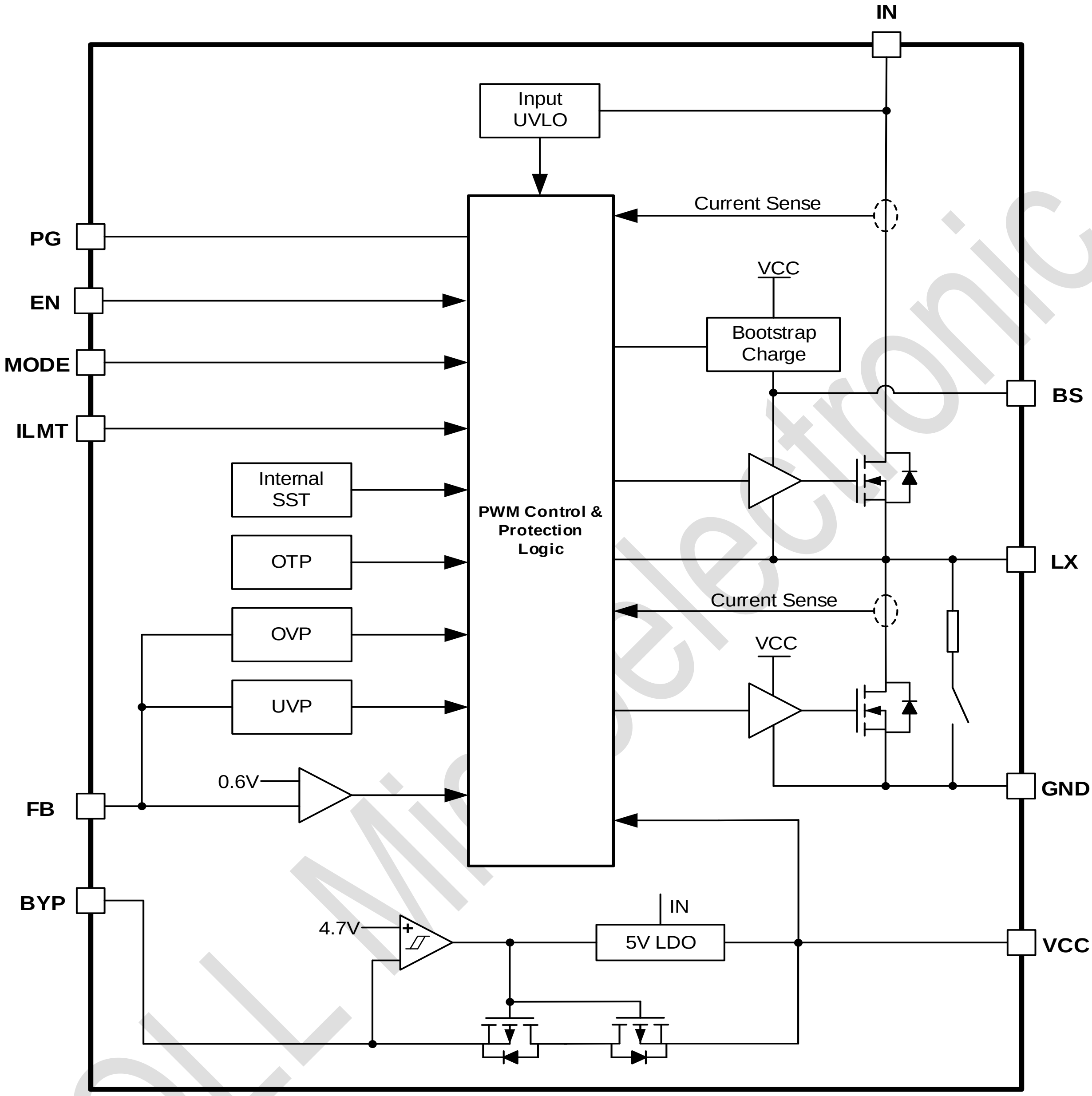


Figure 2. TMI3388A Block Diagram

Operation Description

Overall

The TMI3388A is a high integrated synchronous step-down converter which can operate from 4.5V to 24V input voltage, that can deliver up to 8A output current capability. It has 20mΩ and 10mΩ integrated MOSFETs. The low RDS(ON) MOSFETs that enable high efficiency, and offers high accurate reference voltage. The TMI3388A adopts advance COT control mode and has fast transient response performance that could reduce external component count, save the PCB size. The control topology provides seamless transition between FPWM operating mode at higher load condition and PFM operation at lighter load condition. At light load, PFM operation allows the TMI3388A to maintain high efficiency.

Light Load Operation Mode Selection

TMI3388A has a MODE pin which can setup two different modes of operation for light load. Pull MODE pin low for PFM operation, and pull this pin high for FPWM operation.

Soft Start

The TMI3388A has an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft-start, it clamps the ramping of internal reference voltage which is compared with FB signal. The typical soft-start duration is 1.2ms.

Over Current Protection (OCP)

The TMI3388A has cycle-by-cycle valley current limit function. When the inductor current valley value is larger than the valley current limit during low side MOSFET on state, the device enters into valley over current protection mode and low side MOSFET keeps on state until inductor current drops down to the value equal or lower than the valley current limit, and then on time pulse could be generated and high side MOSFET could turn on again.
If the output is short to GND and the output voltage drop until feedback voltage V_{FB} is below the output under-voltage V_{UV} threshold which is typically 60% of V_{REF}, TMI3388A enters into hiccup mode to periodically disable and restart switching operation. The hiccup mode helps to reduce power dissipation and thermal rise during output short condition.

Output UVP and OVP

When the output voltage falls below Output UVP Threshold (V_{UVP}), the UVP comparator detects it and the device will enter into hic-cup protection mode, If the output fault conditions are removed, the device will go back to normal operation in the nearest hic-cup on time. When the output voltage over Output OVP Threshold (V_{OVP}), the internal feedback voltage rises above the internal reference voltage, the high-side power switch naturally remains off.

Power Good

The Power Good (PG) pin is an open drain output. The power-good function is activated after soft-start is finished and is controlled by the reference signal V_{REF}. When the V_{REF} voltage is between 83% and 120% of the internal reference voltage, the PG is be in high impedance.

Output Discharge

When the shuts down action is triggered, the output discharge function will turn on the internal MOSFET between VOUT and GND, so that achieve rapid discharge of the output capacitor.

VCC Linear Regulator

The TMI3388A has a 5.0V internal VCC. The 5.0V VCC can power the internal gate drivers, PWM logic, analog circuitry and other blocks. A 2.2μF low ESR ceramic capacitor is connected from VCC pin to GND.

BYP Input

The control and drive circuit can also be powered by external 5V power supply. When a 5V external power supply is connected to the BYP pin, the VCC LDO is turned off and the switch between BYP and VCC is turned on. The overall efficiency may be improved by connecting the BYP pin to external 5V switching power supply. Connect a 1μF low ESR ceramic capacitor from BYP pin to GND when BYP is supplied by 5V external power. Leave BYP pin floating if this feature is not used.

Over Temperature Protection (OTP)

Instant-PWM includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

Application information

Selecting the Inductor

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage, A DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. Inductance value is related to inductor ripple current value, input voltage, output voltage setting and switching frequency. The inductor value can be derived from the following equation:

$$L=\frac{V_{OUT}\times(V_{IN}-V_{OUT})}{V_{IN}\times\Delta I_L\times f_S}$$

Where ΔI_L is peak-to-peak inductor ripple current. Large value inductors result in lower ripple current and small value inductors result in high ripple current, so inductor value has effect on output voltage ripple value. DC resistance of inductor which has impact on efficiency of DC/DC converter should be taken into account when selecting the inductor. The maximum inductor peak current is:

$$I_{L(MAX)}=I_{LOAD}+\frac{\Delta I_L}{2}$$

Under light load conditions, larger inductance is recommended for improved light load efficiency.

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_S\times L}\times\left[1-\frac{V_{OUT}}{V_{IN}}\right]\times\left[R_{ESR}+\frac{1}{8\times f_S\times C_2}\right]$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{8\times f_S^2\times L\times C_2}\times\left[1-\frac{V_{OUT}}{V_{IN}}\right]$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_S\times L}\times\left[1-\frac{V_{OUT}}{V_{IN}}\right]\times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The TMI3388A can be optimized for a wide range of capacitance and ESR values.

PCB Layout Guide

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines.

1) Keep the path of switching current short and minimize the loop area formed by Input capacitor, IN pin and GND.

2) Bypass ceramic capacitors are suggested to be put close to the IN Pin.

3) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the chip as possible.

4) VOUT, LX away from sensitive analog areas such as FB.

5) Connect IN, LX, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

6) VCC output capacitors should be small to the ground loop, keep minimize the loop area.

Top Layer **Bottom Layer**

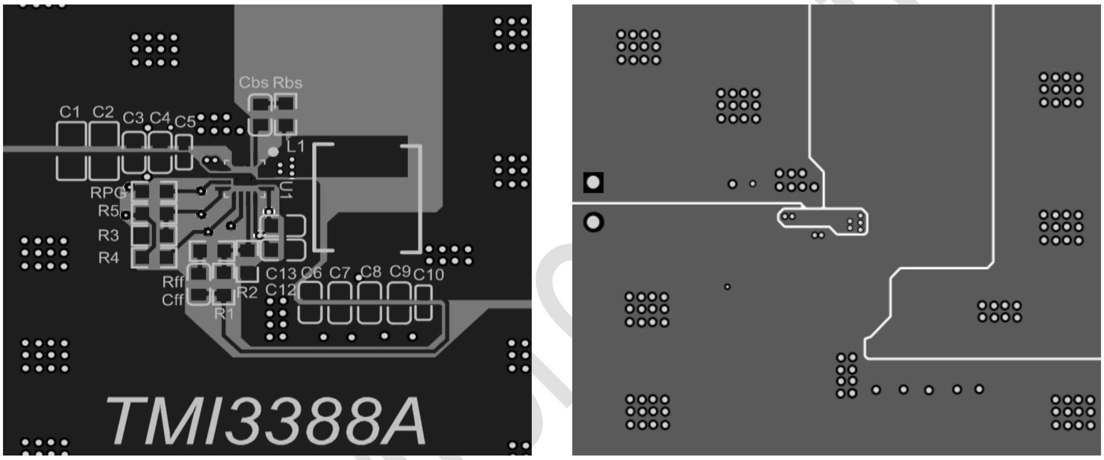
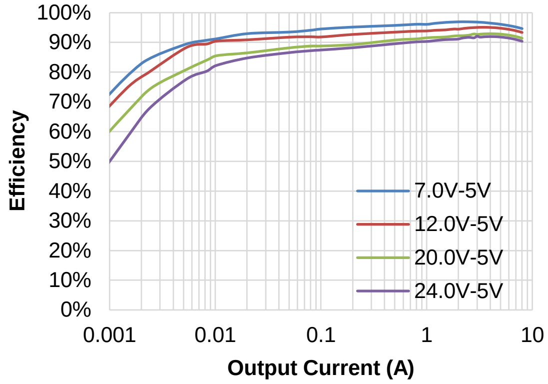


Figure 3. Sample of PCB Layout

Typical Performance Characteristics

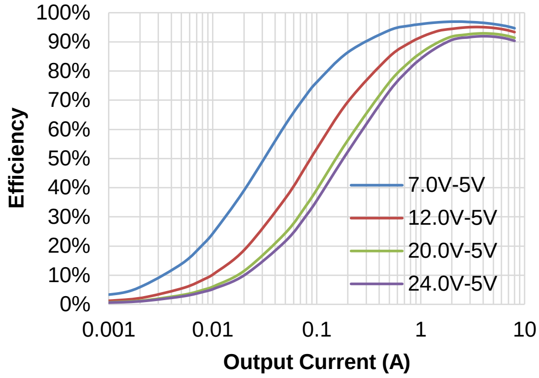
Efficiency vs. Output Current

V_{OUT}=5V, Mode=PFM, L=1.5µH



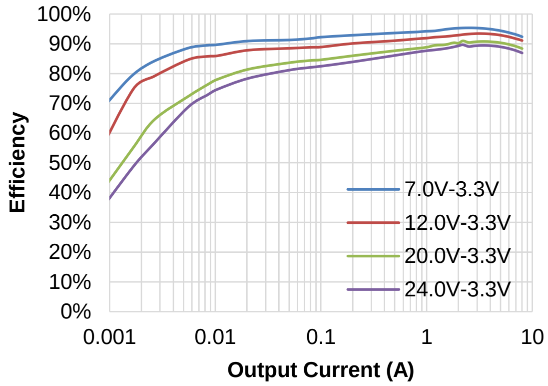
Efficiency vs. Output Current

V_{OUT}=5V, Mode=FPWM, L=1.5µH



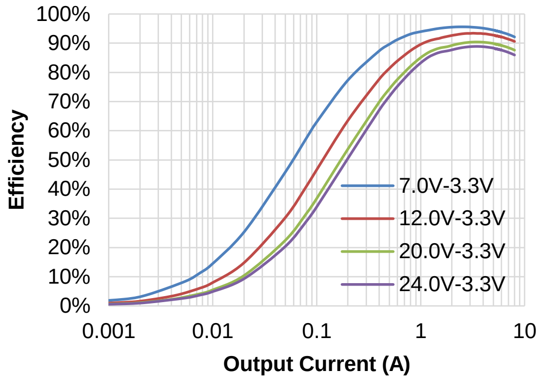
Efficiency vs. Output Current

V_{OUT}=3.3V, Mode=PFM, L=1.5µH



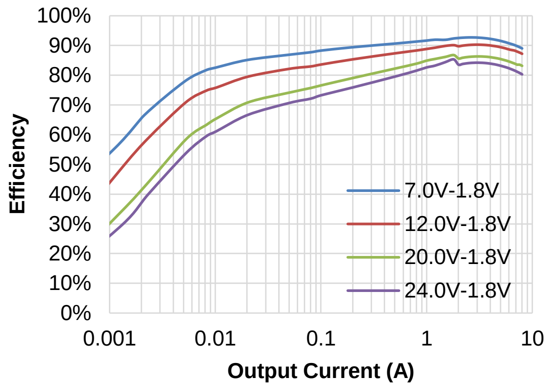
Efficiency vs. Output Current

V_{OUT}=3.3V, Mode=FPWM, L=1.5µH



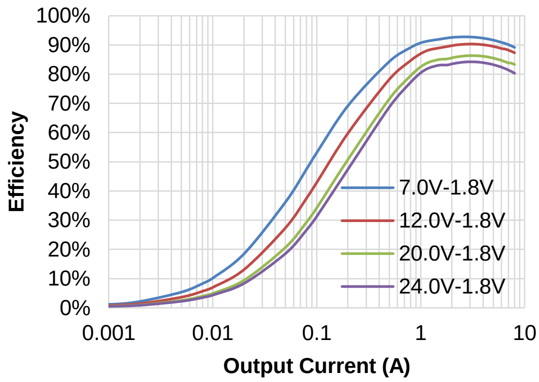
Efficiency vs. Output Current

V_{OUT}=1.8V, Mode=PFM, L=1.5µH



Efficiency vs. Output Current

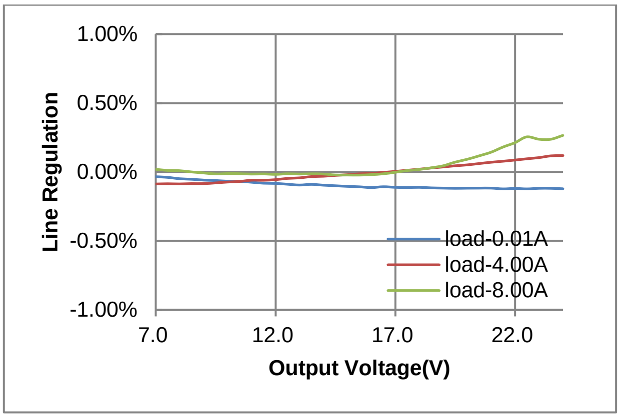
V_{OUT}=1.8V, Mode=FPWM, L=1.5µH



Typical Performance Characteristics(continued)

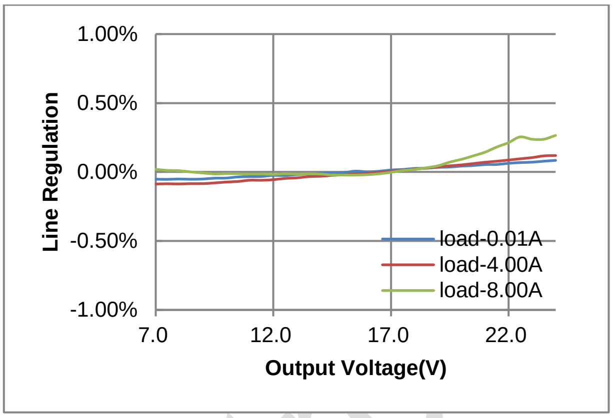
Load Regulation

V_{OUT}=3.3V, Mode=PFM, T_A=25°C



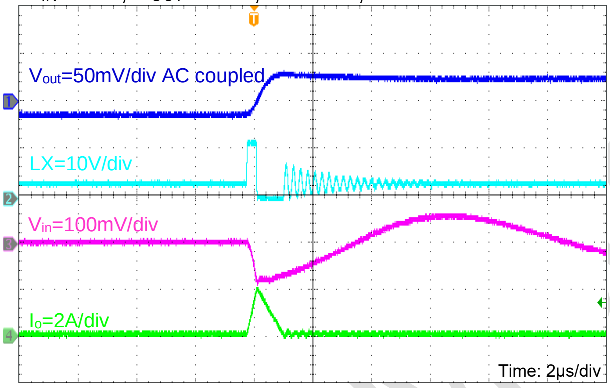
Line Regulation

V_{OUT}=3.3V, Mode=FPWM ,T_A=25°C



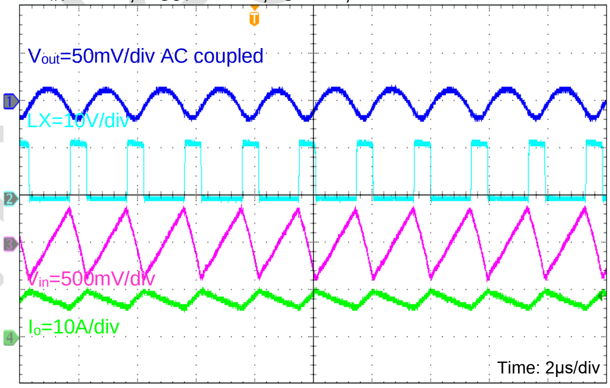
Steady State Operation

V_{IN} =12V, V_{OUT} =3.3V, No Load, Mode=PFM



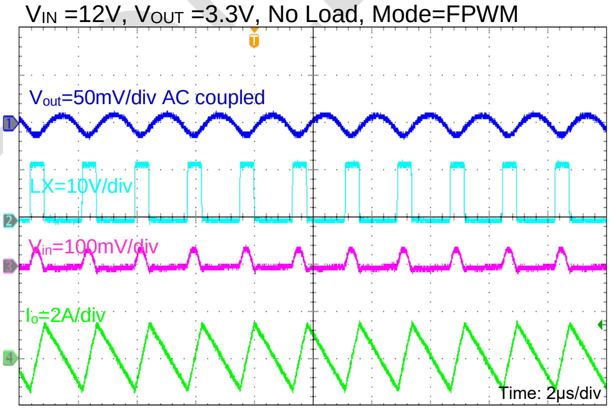
Steady State Operation

V_{IN} =12V, V_{OUT} =3.3V, Io =8A, Mode=PFM



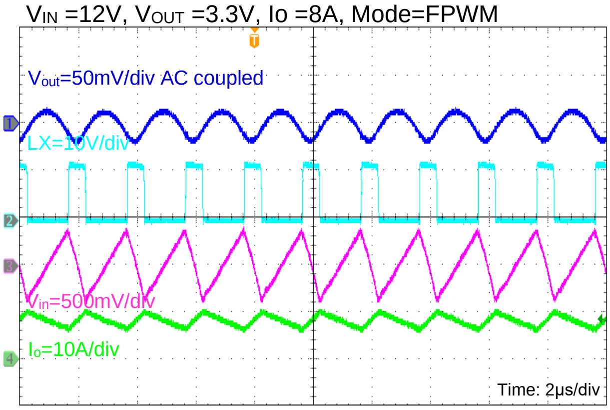
Steady State Operation

V_{IN} =12V, V_{OUT} =3.3V, No Load, Mode=FPWM



Steady State Operation

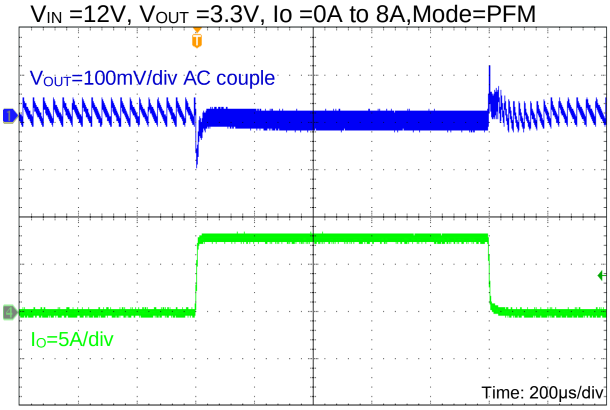
V_{IN} =12V, V_{OUT} =3.3V, Io =8A, Mode=FPWM



Typical Performance Characteristics(continued)

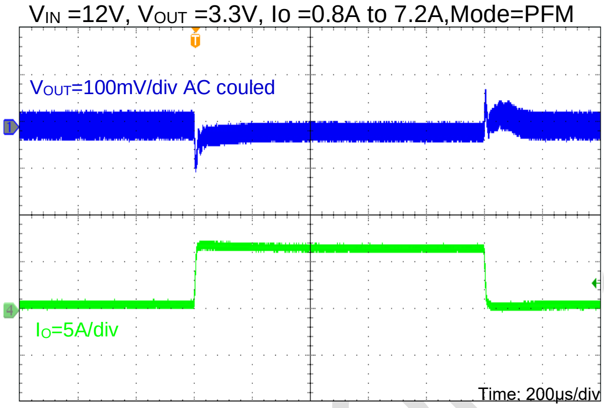
Load Transient

V_{IN} =12V, V_{OUT} =3.3V, Io =0A to 8A,Mode=PFM



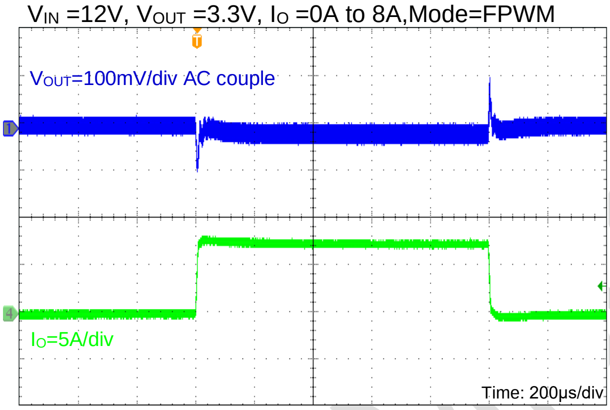
Load Transient

V_{IN} =12V, V_{OUT} =3.3V, Io =0.8A to 7.2A,Mode=PFM



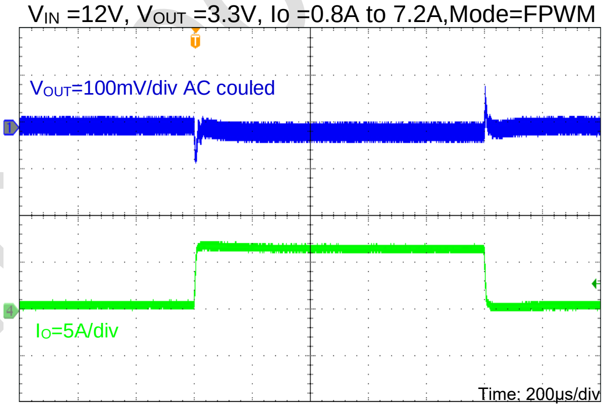
Load Transient

V_{IN} =12V, V_{OUT} =3.3V, I_O =0A to 8A,Mode=FPWM



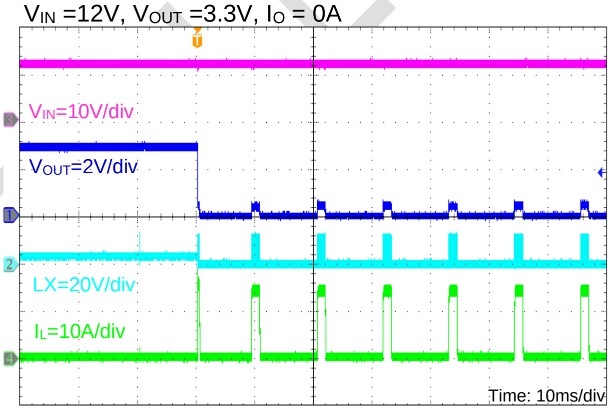
Load Transient

V_{IN} =12V, V_{OUT} =3.3V, Io =0.8A to 7.2A,Mode=FPWM



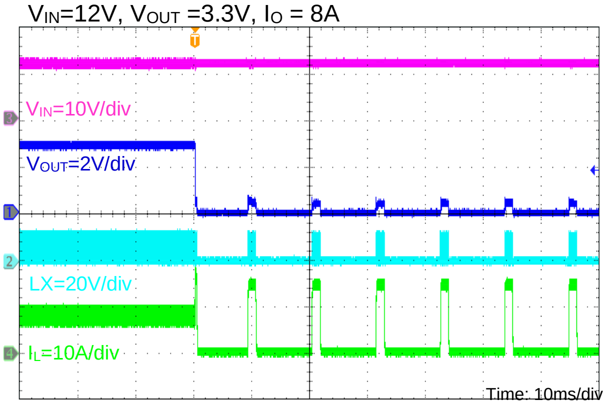
Output Short Entry

V_{IN} =12V, V_{OUT} =3.3V, I_O = 0A



Output Short Entry

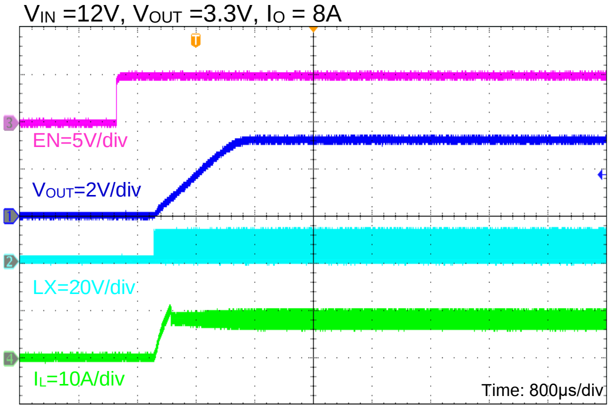
V_{IN}=12V, V_{OUT} =3.3V, I_O = 8A



Typical Performance Characteristics(continued)

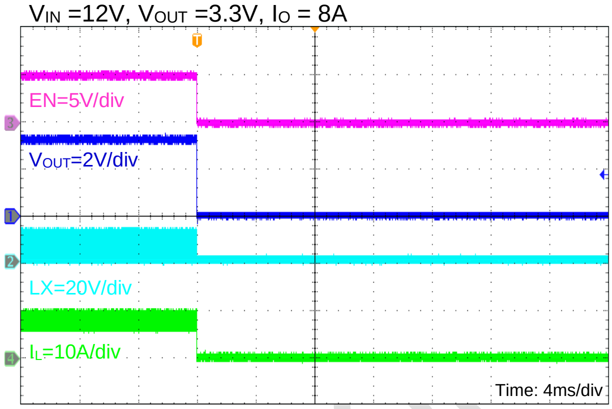
EN Enable

V_{IN} =12V, V_{OUT} =3.3V, I_O = 8A



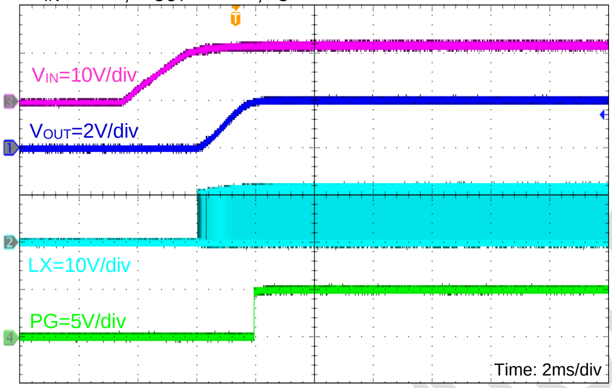
EN Disable

V_{IN} =12V, V_{OUT} =3.3V, I_O = 8A



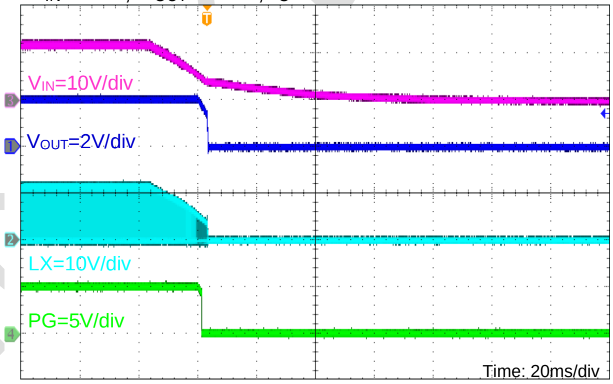
Input Power On

V_{IN} =12V, V_{OUT} =3.3V, I_O = 8A



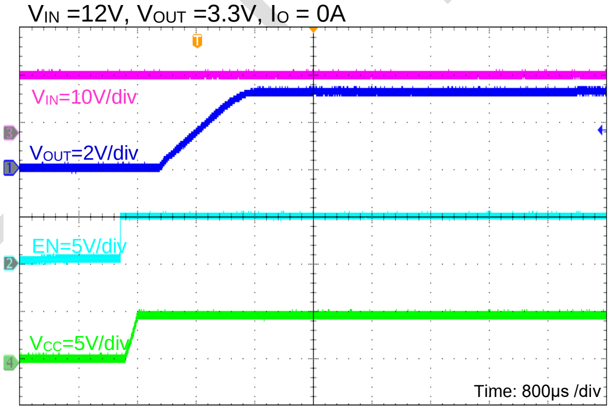
Input Power Down

V_{IN} =12V, V_{OUT} =3.3V, I_O = 8A



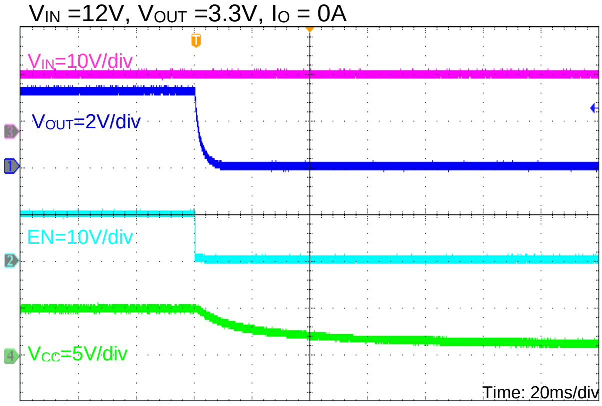
Power On sequence

V_{IN} =12V, V_{OUT} =3.3V, I_O = 0A



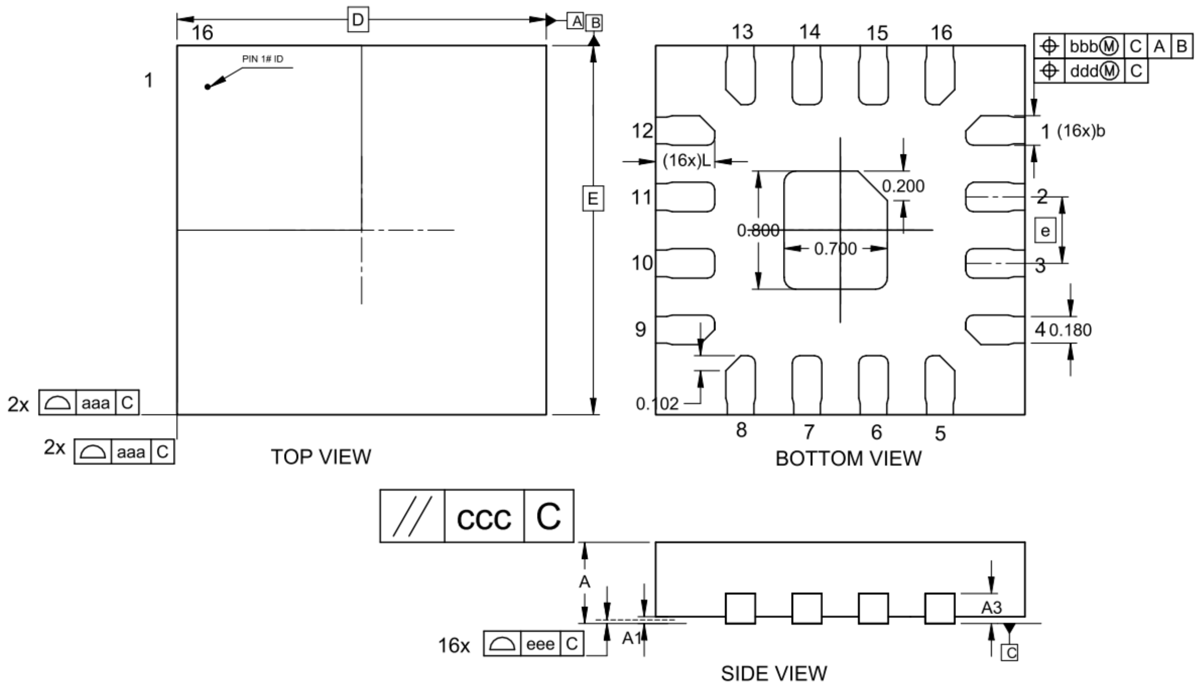
Power Off sequence

V_{IN} =12V, V_{OUT} =3.3V, I_O = 0A



Package Information

QFN2.5x2.5-16



Unit: mm

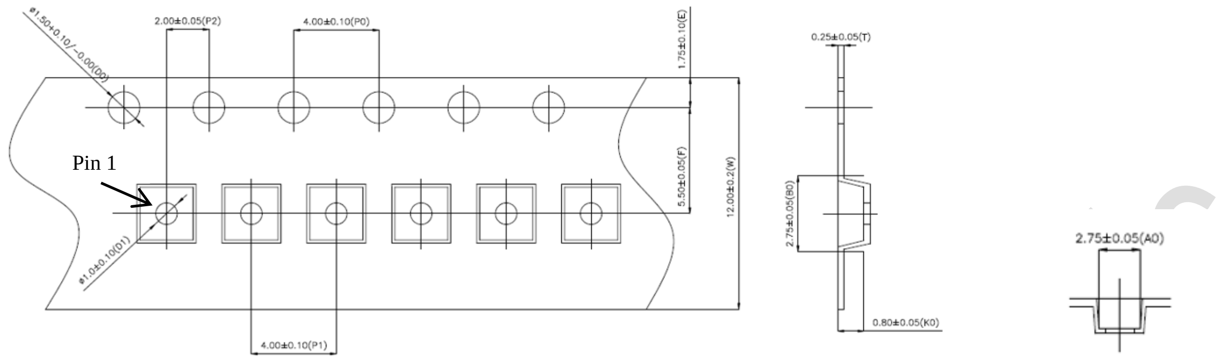
Symbol	Dimensions In Millimeters			Symbol	Dimensions In Millimeters		
	Min	Nom	Max		Min	Nom	Max
A	0.50	0.55	0.60	L	0.35	0.40	0.45
A1	-	0.02	0.05	aaa	0.15		
A3	-	0.152REF	-	bbb	0.10		
b	0.15	0.20	0.25	ccc	0.10		
D	2.50BSC			ddd	0.05		
E	2.50BSC			eee	0.08		
e	0.45BSC						

Note:

1. Dimensioning and tolerancing confirm to Y14.5M-1994.
2. All demensions are in millimeters, angles are in degree.
3. Unilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.
4. Simension b applies to metallized terminal and is measured between 0.150mm to 0.30mm from the terminal TIP.dimension b shoule not be measured in radius area.
5. All spec take JEDEC MO-220 for reference.

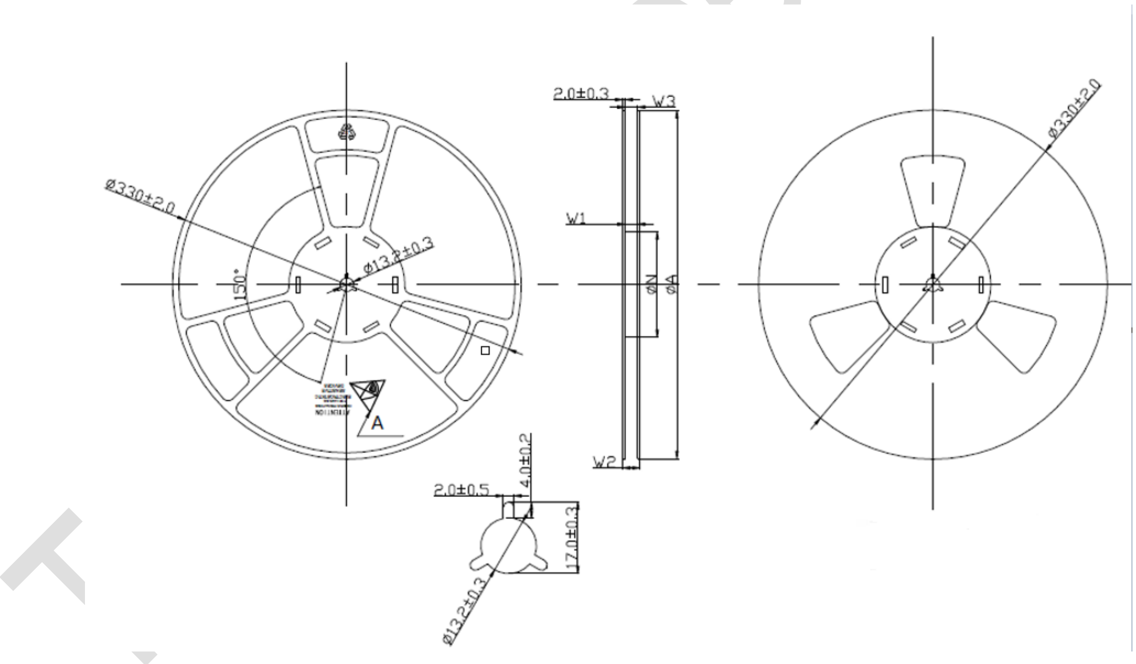
Tape And Reel Information

TAPE DIMENSIONS: QFN2.5*2.5-16



Symbol	P0	P1	P2	D0	A0	D1	B
Dimension (mm)	4.00±0.1	4.00±0.1	2.00±0.05	$1.5^{+0.10}_{0}$	2.75±0.05	1.00±0.1	2.70±0.1
Symbol	E	F	W	K0	B0	T	
Dimension (mm)	1.75±0.1	5.50±0.05	$12^{+0.30}_{-0.10}$	0.80±0.05	2.75±0.05	0.25±0.05	

REEL DIMENSIONS: QFN2.5*2.5-16



TYPE WIDTH	ØA	ØN	W1 (+2/0)	W2 (MAX)	W3 (MAX)
12MM	330±2.0	100±1.0	12.4	18.4	11.9/15.4

Note:

1) All Dimensions are in Millimeter
2) Quantity of Units per Reel is 3000
3) MSL level is level 2.

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