# 3A, 6.5V, Ultra Low Noise, Ultra Low Dropout Linear Regulator

## Features

- Input Voltage Range: 1.1V to 6.5V
- Two Output Voltage Modes
  0.5V to 5.5V (Set by Resistive Divider)
  0.5V to 3.65V (Set VOUT Select Pin, No External Resistor Required)
- Accurate Output Voltage Accuracy (±1%) Over Line, Load and Temperature
- Ultra-high PSRR: 30dB at 500kHz
- Excellent Noise Immunity:
  8μ$V_{RMS}$ at 0.5V Output
  13μ$V_{RMS}$ at 3.3V Output
- Ultra Low Dropout Voltage: 180mV at 3A
- Enable Control
- Programmable Soft-Start Output
- Stable with 10μF or larger Output Ceramic Capacitor
- Support Power-Good Indicator Function
- RoHS Compliant and Halogen Free

## Description

The TMI6013 is a high output current (3A), ultra-low noise, high accuracy, low dropout linear regulator (LDO), and is capable of sourcing 3A with extremely low dropout. The device output voltage can be set by pin-selectable (up to 3.65V) using a PCB layout without the need of external resistors, thus reducing overall component count, meanwhile, the device can be set with higher output voltage by external resistor divider. The device supports single input supply voltage as low as 1.1V that makes it easy to use.

The low noise, high PSRR, and high output current capability make the TMI6013 ideal to power noise-sensitive devices such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and RF components. To reduce inrush current with very high accuracy, remote sensing, and soft-start capabilities, the TMI6013 is ideal for powering digital loads such as FPGAs, DSPs, and ASICs.

The device is offered in a QFN3.5x3.5-20 package.

## Application

- Portable Electronic Devices
- Wireless Infrastructure: FPGA, DSP
- RF, IF Components: VCO, ADC, DAC, LVDS

## Typical Application

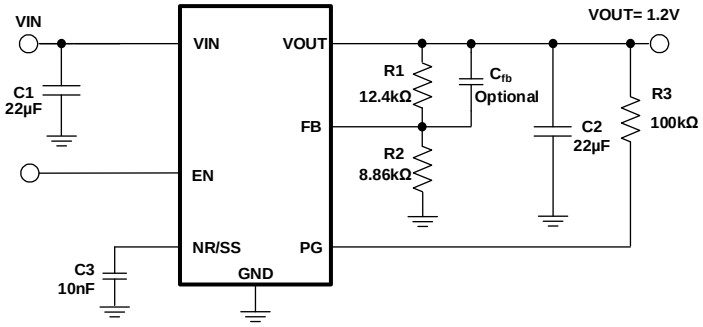



**Figure 1. TMI6013 Typical Application Circuit for VOUT Adjusted by a Resistive Divider**

**Table 1. Recommended Feedback-Resistor Values**

| Output Voltage (V) | External Restive Divider Combinations | |
|---|---|---|
| | R1(kΩ) | R2(kΩ) |
| 0.7 | 12.4 | 31 |
| 1 | 12.4 | 12.4 |
| 1.2 | 12.4 | 8.86 |
| 1.5 | 12.4 | 6.2 |
| 1.8 | 12.4 | 4.77 |
| 2.5 | 12.4 | 3.1 |
| 3.3 | 12.4 | 2.21 |
| 4.5 | 12.4 | 1.55 |
| 5 | 12.4 | 1.38 |

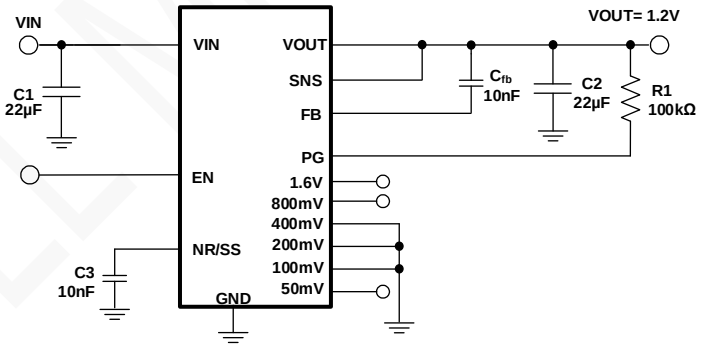



**Figure 2. TMI6013 Typical Application Circuit for VOUT Adjusted by Select Pin Settings**

# Typical Application

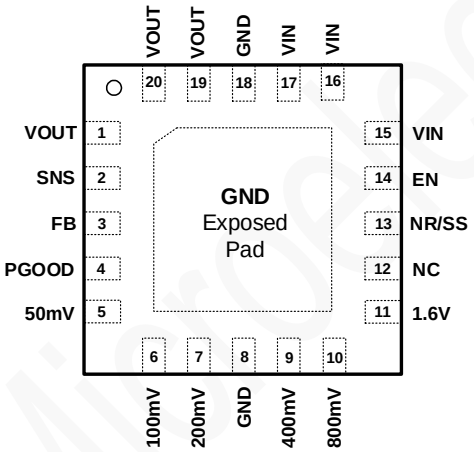
**Table 2. VOUT Select Pin Settings**

| $V_{OUT}$(V) | 50mV | 100mV | 200mV | 400mV | 800mV | 1.6V | $V_{OUT}$(V) | 50mV | 100mV | 200mV | 400mV | 800mV | 1.6V |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **0.5** | Open | Open | Open | Open | Open | Open | **2.1** | Open | Open | Open | Open | Open | GND |
| **0.55** | GND | Open | Open | Open | Open | Open | **2.15** | GND | Open | Open | Open | Open | GND |
| **0.6** | Open | GND | Open | Open | Open | Open | **2.2** | Open | GND | Open | Open | Open | GND |
| **0.65** | GND | GND | Open | Open | Open | Open | **2.25** | GND | GND | Open | Open | Open | GND |
| **0.7** | Open | Open | GND | Open | Open | Open | **2.3** | Open | Open | GND | Open | Open | GND |
| **0.75** | GND | Open | GND | Open | Open | Open | **2.35** | GND | Open | GND | Open | Open | GND |
| **0.8** | Open | GND | GND | Open | Open | Open | **2.4** | Open | GND | GND | Open | Open | GND |
| **0.85** | GND | GND | GND | Open | Open | Open | **2.45** | GND | GND | GND | Open | Open | GND |
| **0.9** | Open | Open | Open | GND | Open | Open | **2.5** | Open | Open | Open | GND | Open | GND |
| **0.95** | GND | Open | Open | GND | Open | Open | **2.55** | GND | Open | Open | GND | Open | GND |
| **1.0** | Open | GND | Open | GND | Open | Open | **2.6** | Open | GND | Open | GND | Open | GND |
| **1.05** | GND | GND | Open | GND | Open | Open | **2.65** | GND | GND | Open | GND | Open | GND |
| **1.1** | Open | Open | GND | GND | Open | Open | **2.7** | Open | Open | GND | GND | Open | GND |
| **1.15** | GND | Open | GND | GND | Open | Open | **2.75** | GND | Open | GND | GND | Open | GND |
| **1.2** | Open | GND | GND | GND | Open | Open | **2.8** | Open | GND | GND | GND | Open | GND |
| **1.25** | GND | GND | GND | GND | Open | Open | **2.85** | GND | GND | GND | GND | Open | GND |
| **1.3** | Open | Open | Open | Open | GND | Open | **2.9** | Open | Open | Open | Open | GND | GND |
| **1.35** | GND | Open | Open | Open | GND | Open | **2.95** | GND | Open | Open | Open | GND | GND |
| **1.4** | Open | GND | Open | Open | GND | Open | **3.0** | Open | GND | Open | Open | GND | GND |
| **1.45** | GND | GND | Open | Open | GND | Open | **3.05** | GND | GND | Open | Open | GND | GND |
| **1.5** | Open | Open | GND | Open | GND | Open | **3.1** | Open | Open | GND | Open | GND | GND |
| **1.55** | GND | Open | GND | Open | GND | Open | **3.15** | GND | Open | GND | Open | GND | GND |
| **1.6** | Open | GND | GND | Open | GND | Open | **3.2** | Open | GND | GND | Open | GND | GND |
| **1.65** | GND | GND | GND | Open | GND | Open | **3.25** | GND | GND | GND | Open | GND | GND |
| **1.7** | Open | Open | Open | GND | GND | Open | **3.3** | Open | Open | Open | GND | GND | GND |
| **1.75** | GND | Open | Open | GND | GND | Open | **3.35** | GND | Open | Open | GND | GND | GND |
| **1.8** | Open | GND | Open | GND | GND | Open | **3.4** | Open | GND | Open | GND | GND | GND |
| **1.85** | GND | GND | Open | GND | GND | Open | **3.45** | GND | GND | Open | GND | GND | GND |
| **1.9** | Open | Open | GND | GND | GND | Open | **3.5** | Open | Open | GND | GND | GND | GND |
| **1.95** | GND | Open | GND | GND | GND | Open | **3.55** | GND | Open | GND | GND | GND | GND |
| **2.0** | Open | GND | GND | GND | GND | Open | **3.6** | Open | GND | GND | GND | GND | GND |
| **2.05** | GND | GND | GND | GND | GND | Open | **3.65** | GND | GND | GND | GND | GND | GND |

## Absolute Maximum Ratings (Note 1)

| Parameter | Min | Max | Unit |
|---|---|---|---|
| VIN, PGOOD, EN | -0.3 | 7 | V |
| VOUT | -0.3 | $V_{IN}$+0.3 | V |
| NR/SS,FB | -0.3 | 3.6 | V |
| All Other Pins | -0.3 | $V_{IN}$+0.3 | V |
| Storage Temperature Range | -65 | 150 | °C |
| Junction Temperature | 150 | | °C |
| Power Dissipation, $P_D$ @$T_A$=25°C | 3.5 | | W |
| Lead Temperature (Soldering, 10s) | 260 | | °C |

## Package




**QFN3.5x3.5-20**

**Top Marking: T6013/XXXXX (T6013: Device Code, XXXXX: Inside Code)**

## Order Information

| Part Number | Package | Top Marking | Quantity/Reel |
|---|---|---|---|
| TMI6013 | QFN3.5x3.5-20 | T6013<br>XXXXX | 3000 |

TMI6013 devices are Pb-free and RoHS compliant.

## Pin Functions

| Pin | Name | Function |
|---|---|---|
| 1,19,20 | VOUT | LDO output pins. A 10μF or larger ceramic capacitor (4.7μF or greater of effective capacitance) is required for stability. Place the output capacitor as close to the device as possible and minimize the impedance between the VOUT pin and load. |
| 2 | SNS | Output voltage sense input pin. Connect this pin only when setting the VOUT voltage by using PCB layout (No external resistor required). Keep SNS pin floating if the VOUT voltage is set by external resistor. |
| 3 | FB | Feedback voltage input. This pin is used to set the desired output voltage via an external resistive divider. The feedback reference voltage is 0.5V typically |
| 4 | PGOOD | Power good indicator output. It's an open-drain output and is active high when the output voltage reaches 88% of the target. The pin is pulled to ground when the output voltage is lower than its specified threshold, EN shutdown, OCP and OTP. |
| 5,6,7,9, 10,11 | 50mV, 100mV, 200mV, 400mV, 800mV, 1.6V | Output voltage setting pins. Connect these pins to ground or leave floating. Connecting these pins to ground increases the output voltage by the value of the pin name. Multiple pins can be simultaneously connected to GND to select the desired output voltage. Leave these pins floating (open) if the VOUT voltage is set by external resistor. |
| 8,18, Exposed Pad | GND | Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum the power dissipation. |
| 12 | NC | No internal connection. |
| 13 | NR/SS | Noise-reduction and soft-start pin. Decouple this pin to GND with an external capacitor $C_{NR/SS}$ can not only reduce output noise to very low levels but also slow down the VOUT rise like a soft-start behavior. For low noise applications, a 10nF to 1μF CNR/SS is suggested. |
| 14 | EN | Enable control input. Connecting this pin to logic high enables the regulator or driving this pin low make the device enters shutdown mode. The device can operate with $V_{IN}$ and $V_{EN}$ sequenced in any order. Mostly, enabling the device after $V_{IN}$ is present can achieve precise timing control. |
| 15,16,17 | VIN | Supply input. A minimum of 22μF ceramic capacitor should be placed as close as possible to this pin for better noise rejection. |

## ESD Rating (Note3)

| Items | Description | Value | Unit |
|---|---|---|---|
| $V_{ESD\_HBM}$ | Human Body Model for all pins | ±2000 | V |
| $V_{ESD\_CDM}$ | Charged Device Model for all pins | ±1000 | V |

JEDEC specification JS-001

## Recommended Operating Conditions (Note4)

| Items | Description | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage Range | VIN | 1.1 | 6.5 | V |
| $T_J$ | Junction Temperature Range | -40 | 125 | °C |

## Thermal Resistance (Note2)

| Items | Description | Value | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 28.5 | °C/W |
| $\theta_{JC}$ | Junction-to-case(top) thermal resistance | 7.2 | °C/W |

## Electrical Characteristics

**$T_A$ = 25°C, 1.1V≤$V_{IN}$<6.5V and $V_{IN}$≥$V_{OUT(TARGET)}$ + 0.3V, $V_{OUT(TARGET)}$ = 0.5V, $V_{OUT}$ connected to 50Ω to GND, $V_{EN}$ = 1.1V, $C_{IN}$ = 10μF, $C_{OUT}$ = 22μF, $C_{NR/SS}$= 10nF, $C_{fb}$= 10nF, and PGOOD pin pulled up to $V_{IN}$ with 100kΩ, unless otherwise noted.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Operating Input Voltage Range | $V_{IN}$ | | 1.1 | | 6.5 | V |
| Feedback Reference Voltage | $V_{REF}$ | | 0.495 | 0.5 | 0.505 | V |
| NR/SS Pin Voltage | $V_{NR/SS}$ | | | 0.5 | | V |
| Under-Voltage Lockout Threshold | $V_{UVLO}$ | VIN rising | | 1.04 | 1.09 | V |
| | $\Delta V_{UVLO}$ | Hysteresis | | 185 | | mV |
| Output Voltage Range | | Using voltage setting pins (50mV, 100mV,200mV, 400mV, 800mV, and 1.6V) | 0.5 | | 3.65 | V |
| | | Using external resistors | 0.5 | | 5.5 | V |
| Output Voltage Accuracy | $V_{OUT}$ | $V_{IN}$=$V_{OUT}$ + 0.3V, 0.5V≤$V_{OUT}$≤5.5V, 5mA≤$I_{OUT}$≤3A | -1 | | 1 | % |
| Line Regulation | $\Delta V_{OUT}/\Delta V_{IN}$ | $I_{OUT}$= 5mA, 1.4V≤$V_{IN}$≤6.5V | | 0.05 | | %/V |
| Load Regulation | $\Delta V_{OUT}/\Delta I_{OUT}$ | 5mA≤$I_{OUT}$≤3A | | 0.08 | | %/A |
| Dropout Voltage | $V_{DROP}$ | $V_{IN}$=1.1V to 6.5V, $I_{OUT}$ = 3A, $V_{FB}$= 0.5V - 3% | | 110 | 180 | mV |
| Output Current Limit | $I_{LIM}$ | $V_{OUT}$=90% $V_{OUT(TARGET)}$, $V_{IN}$=$V_{OUT(TARGET)}$ + 400mV | 3.5 | 4.2 | 4.7 | A |
| Ground Pin Current | $I_{GND}$ | Minimum load, $V_{IN}$=6.5V, $I_{OUT}$=5mA | | 2.2 | 3.1 | mA |
| | | Maximum load, $V_{IN}$=1.4V, $I_{OU}$ =3A | | 3.5 | 4.3 | |
| | | Shutdown, PGOOD=Open, $V_{IN}$=6.5V, $V_{EN}$=0.5V | | | 25 | μA |
| EN Pin Current | $I_{EN}$ | $V_{IN}$=6.5V, $V_{EN}$= 0V and 6.5V | -0.1 | | 0.2 | μA |
| EN Pin High-Level Input Voltage | $V_{EN\_H}$ | Enable device | 1.1 | | 6.5 | V |
| EN Pin Low-Level Input Voltage | $V_{EN\_L}$ | Disable device | 0 | | 0.5 | V |
| PGOOD Pin Threshold | $V_{IT\_PGOOD}$ | For the direction PGOOD signal falling with decreasing $V_{OUT}$ | 0.86x $V_{out}$ | 0.88 x $V_{out}$ | 0.91 x $V_{out}$ | V |
| PGOOD Pin Hysteresis | $V_{PGOOD\_HYS}$ | For PGOOD signal rising | | 0.025 x$V_{out}$ | | V |
| PGOOD Pin Low-Level Output Voltage | $V_{PGOOD\_L}$ | $V_{OUT}$ < $V_{IT\_PGOOD}$, $I_{PGOOD}$ = 1mA (current into device) | | | 0.4 | V |
| Auoto-discharge Resistor | $R_{DIS}$ | | | 380 | | Ω |

## Electrical Characteristics

**$T_A$ = 25°C, 1.1V≤$V_{IN}$<6.5V and $V_{IN}$≥$V_{OUT(TARGET)}$ + 0.3V, $V_{OUT(TARGET)}$ = 0.5V, $V_{OUT}$ connected to 50Ω to GND, $V_{EN}$ = 1.1V, $C_{IN}$ = 10μF, $C_{OUT}$ = 22μF, $C_{NR/SS}$= 10nF, $C_{fb}$= 10nF, and PGOOD pin pulled up to $V_{IN}$ with 100kΩ, unless otherwise noted.**

| Parameter | Symbol | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| PGOOD Pin Leakage Current | $I_{PGOOD\_LK}$ | $V_{OUT}$ > $V_{IT\_PGOOD}$, $V_{PGOOD}$=6.5V | | | | 1 | μA |
| NR/SS Pin Charging Current | $I_{NR/SS}$ | $V_{NR/SS}$=GND, $V_{IN}$=6.5V | | 4.5 | 5.7 | 8.3 | μA |
| FB Pin Leakage Current | $I_{FB}$ | $V_{IN}$=6.5V | | -20 | | 20 | nA |
| Power Supply Rejection Ratio | PSRR | $I_{OUT}$=3A, $C_{NR/SS}$=100nF, $C_{FB}$=10nF, $C_{OUT}$=47μF//10μF//10μF | f=10kHz, $V_{OUT}$=0.5V, $V_{IN}$=1.2V | | 42 | | dB |
| | | | f=500kHz, $V_{OUT}$=0.5V, $V_{IN}$=1.2V | | 30 | | |
| | | | f=10kHz, $V_{OUT}$=5V, $V_{IN}$=5.5V | | 40 | | |
| | | | f=500kHz, $V_{OUT}$=5V, $V_{IN}$=5.5V | | 25 | | |
| Output Noise Voltage | | 10Hz to 100kHz, $I_{OUT}$=3A, $C_{NR/SS}$=100nF, $C_{FB}$=10nF, $C_{OUT}$=22μF | $V_{IN}$=1.1V, $V_{OUT}$=0.5V | | 8 | | $\mu V_{RMS}$ |
| | | | $V_{OUT}$=3.3V | | 13 | | |
| Thermal Shutdown Threshold | $T_{SD}$ | Temperature increasing | | | 160 | | °C |
| | | Temperature decreasing | | | 140 | | °C |

**Note 1**: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2**: $T_J$ is calculated from the ambient temperature $T_A$ and power dissipation $P_D$ according to the following formula: $T_J = T_A + P_D \times \theta_{JA}$.

**Note 3**: Measured on JESD51-7, 4-layer PCB.

**Note 4**: The dropout voltage is defined as $V_{IN}$-$V_{OUT}$, when $V_{OUT}$ is 97% of the normal value of $V_{OUT}$.

**Note 5**: Guaranteed by design.

## Block Diagram

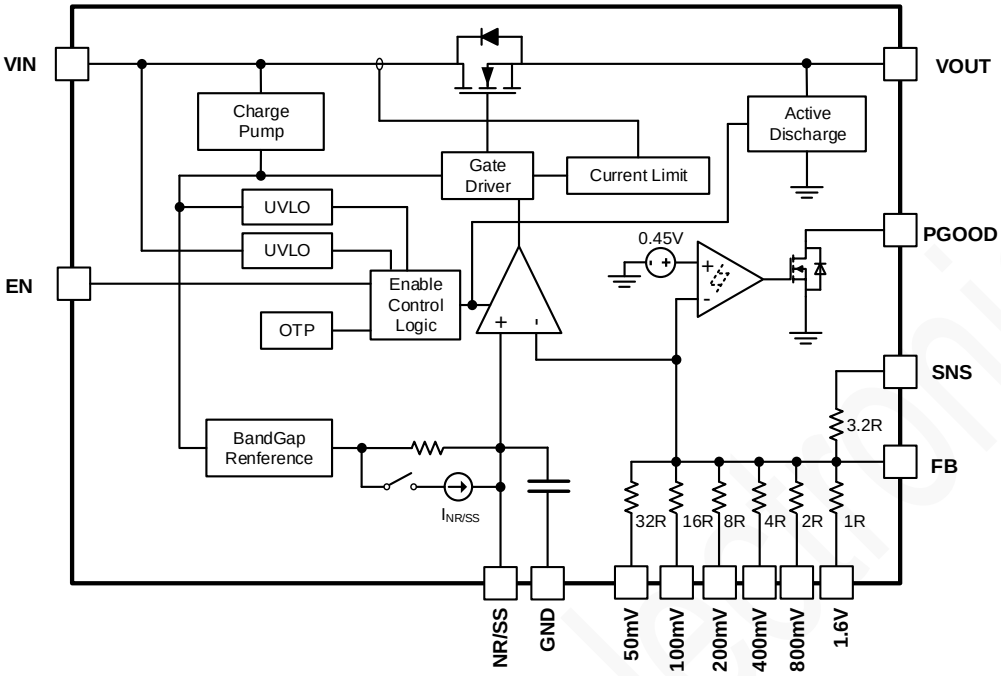



**Figure 3. TMI6013 Block Diagram**

## Operation Description

The TMI6013 operates with single supply input ranging from 1.1V to 6.5V and is capable to deliver 3A current to the output. The device features high PSRR and low noise providing a clean supply to the application.

A low-noise reference and error amplifier are included to reduce device noise. The NR/SS capacitor filters the noise from the reference and feed-forward capacitor filters the noise from the error amplifier. The high power-supply rejection ratio (PSRR) of the TMI6013 minimizes the coupling of input supply noise to the output.

### Enable and Shutdown

The TMI6013 provides an EN pin, as an external chip enable control, to enable or disable the device. The regulator is turned off and enters the shutdown mode when $V_{EN}$ is below 0.5V. When $V_{EN}$ is above 1.1V, the regulator is turned on. When the regulator is shut down, the ground current is reduced to a maximum of 25μA. If the enable timing control is not used, connect EN to the largest capacitance on the input as close as possible to prevent voltage droops on the $V_{IN}$ line from triggering the enable circuit.

### Soft-Start

The noise-reduction capacitor ($C_{NR/SS}$) accomplishes dual purpose of noise-reduction and programming the soft-start ramp time during turn-on. When EN and UVLO exceeds the respective threshold voltage, the TMI6013 activates a quick-start circuit to charge the noise reduction capacitor ($C_{NR/SS}$) and then the output voltage ramps up.

### Power Good

The power-good circuit monitors the feedback pin voltage to indicate the status of the output voltage. The open drain PGOOD pin requires an external pull-up resistor to an external supply, any downstream device can receive power-good as a logic signal that can be used for sequencing. The pull-up resistor from 10kΩ to 100kΩ is recommended. Make sure that the external pull-up supply voltage results in a valid logic signal for the receiving device or devices.

### Under-Voltage Lockout (UVLO)

The UVLO circuit monitors the input voltage to prevent the device from turning on before $V_{IN}$ rises above the $V_{UVLO}$ threshold. The UVLO circuit also disables the output of the device when $V_{IN}$ falls below the lockout voltage ($V_{UVLO} - \Delta V_{UVLO}$). The UVLO circuit is activated to disable the output of the device if $V_{IN}$ collapses.

### Current Limit (ILIM)

TheTMI6013 continuously monitors the output current to protect the pass transistor against abnormal operations. When an overload or short circuit is encountered, the current limit circuitry controls the pass transistor's gate voltage to limit the output within the predefined range.

By reason of the build-in body diode, the pass transistor conducts current when the output voltage exceeds input voltage. Since the current is not limited, external current protection should be added if the

device may work at reverse voltage state.

## Output Active Discharge

When the device is disabled, the TMI6013 discharges the LDO output through an internal several hundred ohms impedance to ground. Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. External current protection should be added if the device may work at reverse voltage state.

## VOUT Select Pins

The TMI6013 has built-in matched feedback resistor network to set output voltage. The output voltage can be programmed from 0.5V to 3.65V in 50mV steps when tying these select pins (Pin 5, Pin 6, Pin 7, Pin 9, Pin 10 and Pin 11) to ground. Tying any of the $V_{OUT}$ programming pins to SNS can lower the value of the upper resistor divider. Hence, the $V_{OUT}$ programming resolution is increased.

## Layout Considerations

For best performance of the TMI6013, the PCB layout suggestions below are highly recommended. All circuit components should be placed on the same side and as near to the respective LDO pin as possible. The ground return path connection should be placed to the input and output capacitor, and the ground plane should be connected by a wide copper surface for good thermal dissipation. Using vias and long power traces for the input and output capacitors connection is discouraged and has negatively effects on performance. Figure 4 shows an example for the layout reference that reduces conduction trace loop, helping to minimize inductive parasitic, and keep good circuit stability

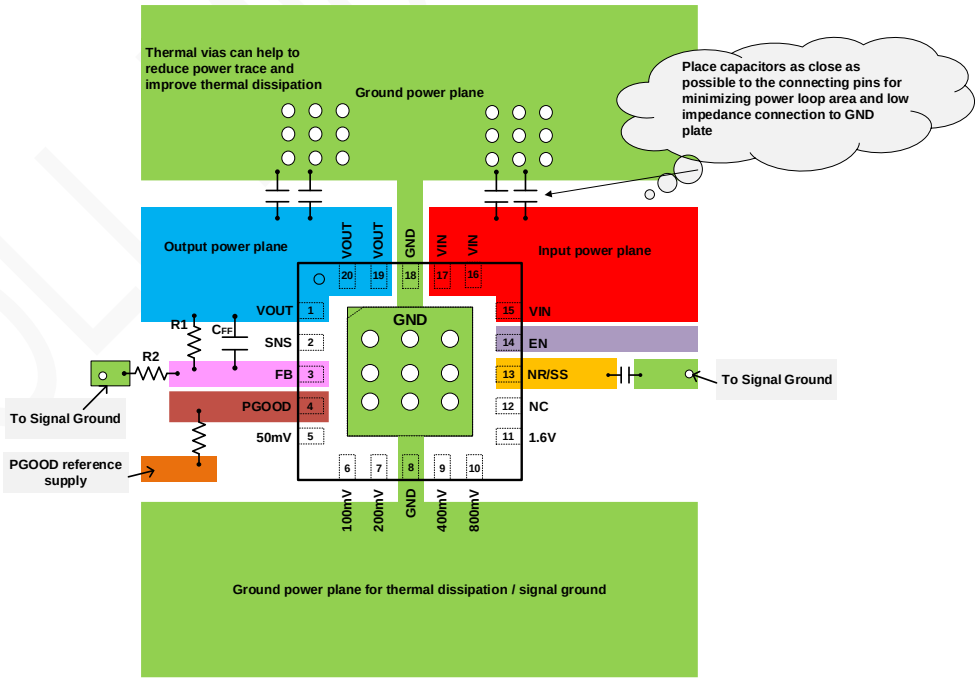
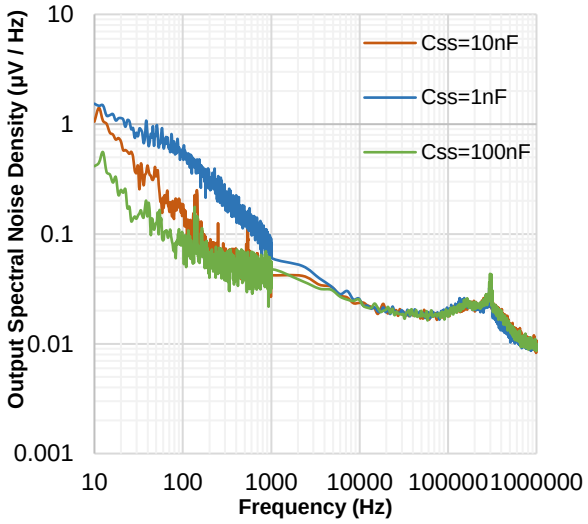



**Figure 4. TMI6013 Layout Recommendation**

## TYPICAL PERFORMANCE CHARACTERISTICS

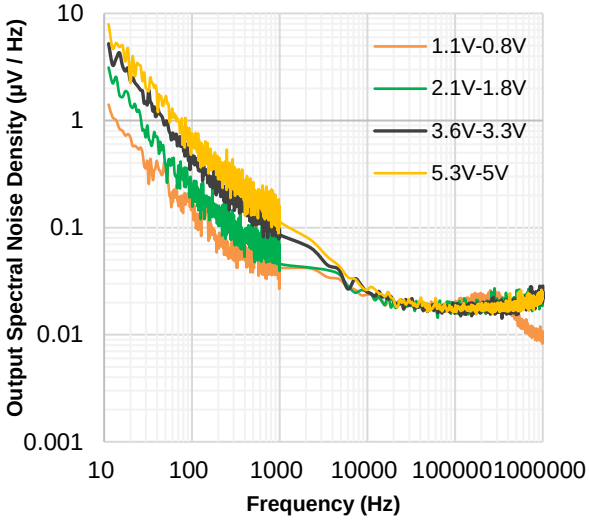
### Output Noise vs. Frequency and $C_{SS}$

$V_{IN}$=1.1V, $V_{OUT}$=0.8V, $I_{OUT}$ =1.5A



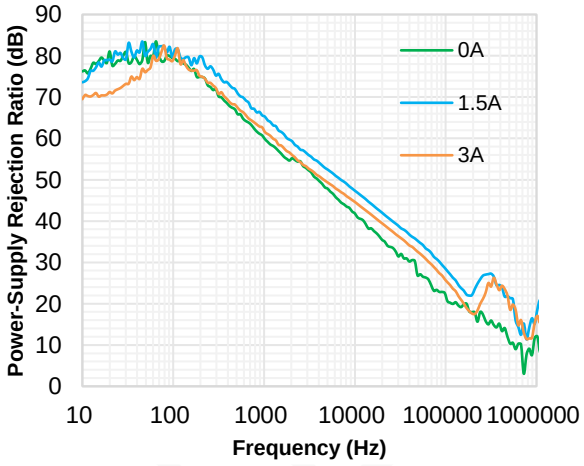

### Output Noise vs. Frequency and $V_{OUT}$

$C_{SS}$ = 10nF, $I_{OUT}$ =1.5A



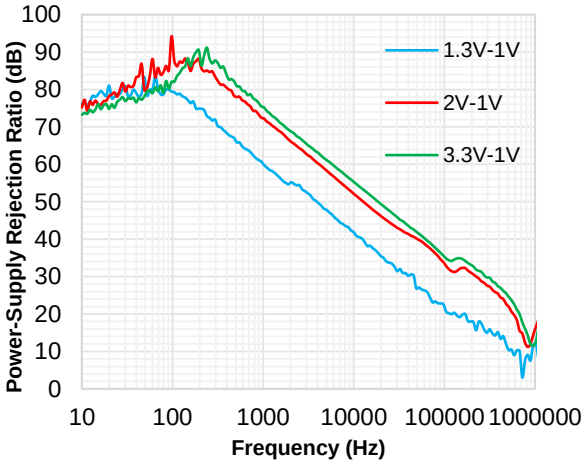

### PSRR vs. Frequency and IOUT

$V_{IN}$ =1.3V, $V_{OUT}$=1V, $C_{SS}$=10nF



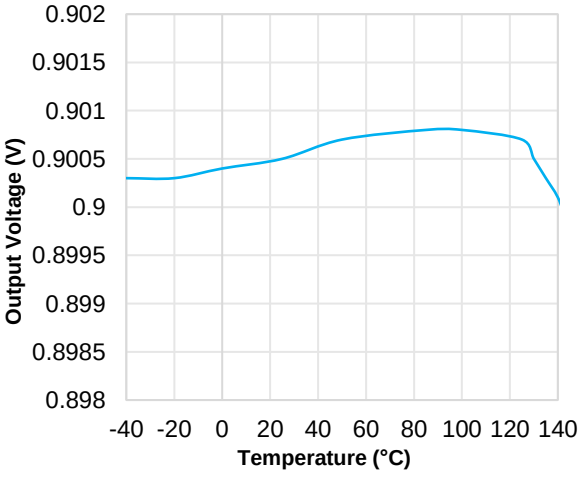

### PSRR vs. Frequency and $V_{IN}$

$V_{OUT}$=1V, $C_{SS}$=10nF



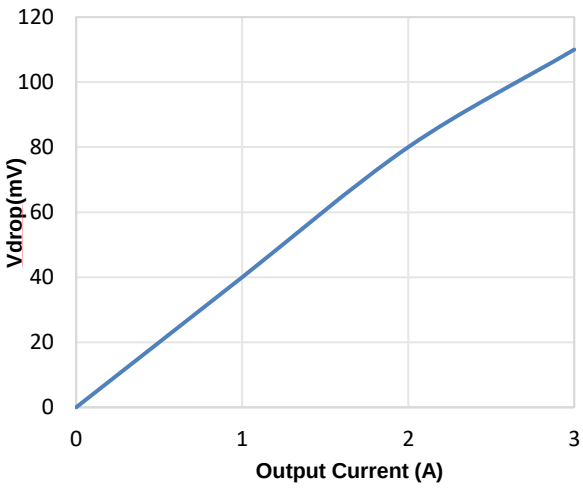

### Output Voltage Vs. Temperature

$V_{IN}$ =1.2V, $C_{SS}$ = 10nF, $I_{OUT}$=5mA




### Dropout Voltage Vs. Temperature

$V_{IN}$ =1.1V-6.5V

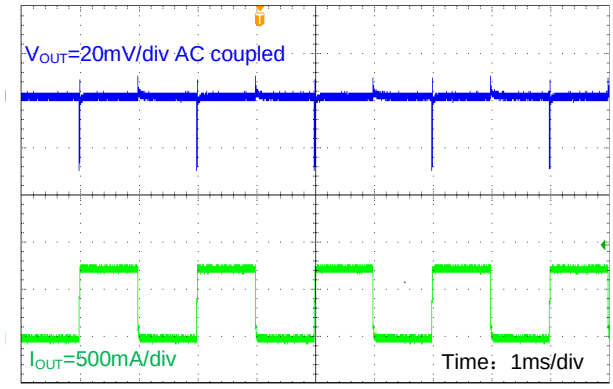


## Typical Performance Characteristics (continued)

**$C_{IN}$ = 47μF +10μF, $C_{OUT}$ = 47μF+10μF+10μF, $C_{NR/SS}$= 10nF, $C_{fb}$= 10nF**

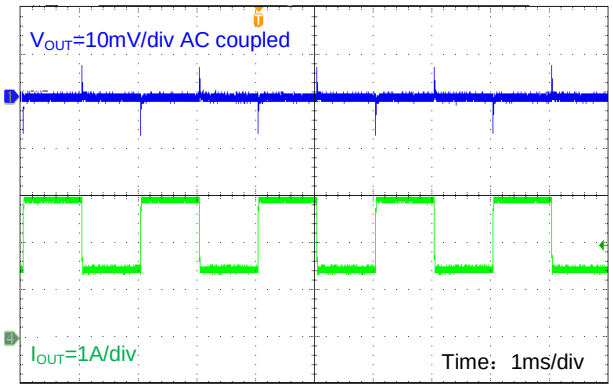
### load Transient

$V_{IN}$=2V, $V_{OUT}$=1V, $I_{OUT}$=0A to 1.5A



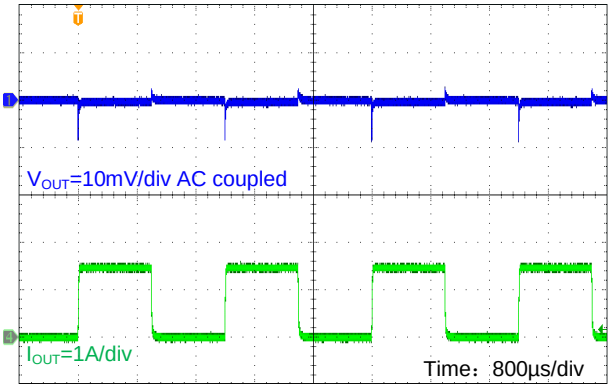

### load Transient

$V_{IN}$= 2V, $V_{OUT}$=1V, $I_{OUT}$=1.5A to 3A



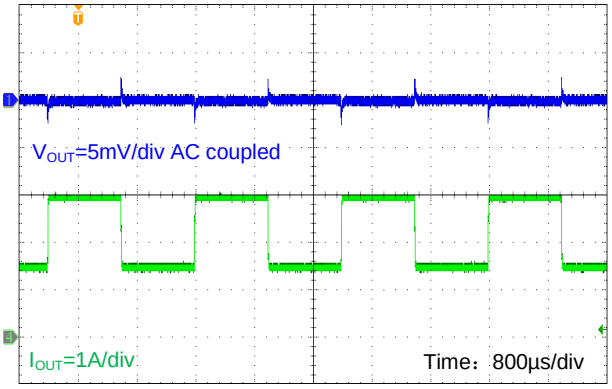

### load Transient

$V_{IN}$ =6V, $V_{OUT}$=5V, $I_{OUT}$=0A to 1.5A



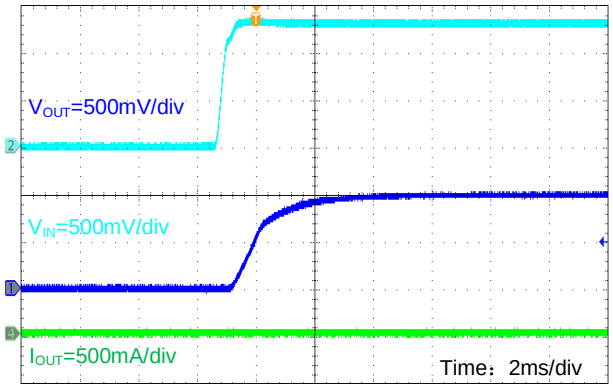

### load Transient

$V_{IN}$= 6V, $V_{OUT}$=5V, $I_{OUT}$=1.5A to 3A



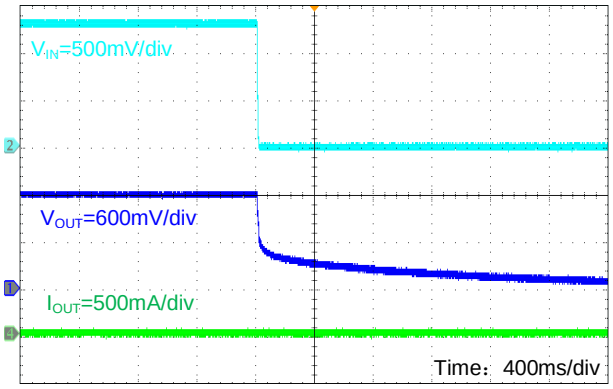

### Input Power On

$V_{IN}$=1.3V, $V_{OUT}$=1V, $V_{EN}$= $V_{IN}$, $I_{OUT}$=0mA




### Input Power Down

$V_{IN}$=1.3V, $V_{OUT}$=1V, $V_{EN}$= $V_{IN}$, $I_{OUT}$=0mA

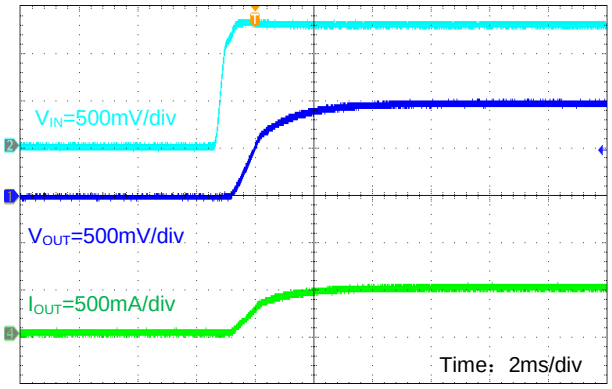


## Typical Performance Characteristics (continued)

**$C_{IN}$ = 47μF+10μF, $C_{OUT}$ = 47μF+10μF+10μF, $C_{NR/SS}$= 10nF, $C_{fb}$= 10nF**

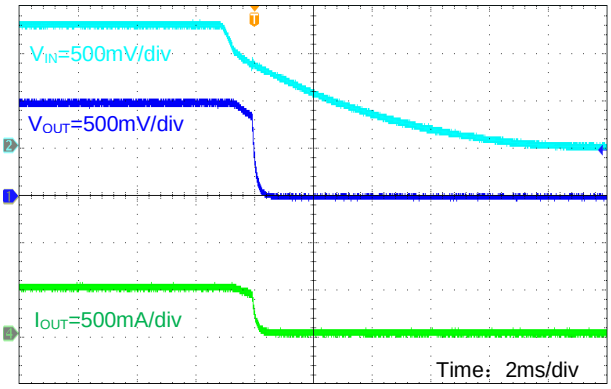
### Input Power On

$V_{IN}$=1.3V, $V_{OUT}$=1V, $V_{EN}$= $V_{IN}$, $I_{OUT}$=500mA



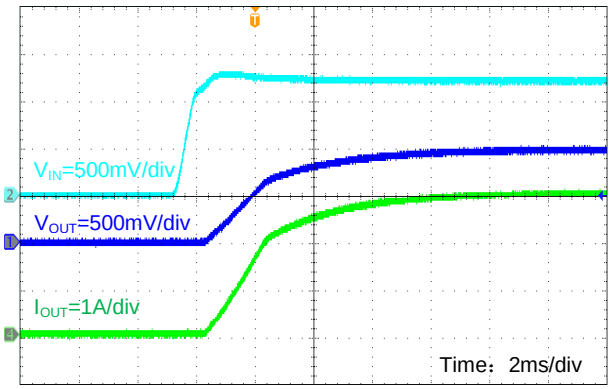

### Input Power Down

$V_{IN}$=1.3V, $V_{OUT}$=1V, $V_{EN}$= $V_{IN}$, $I_{OUT}$=500mA



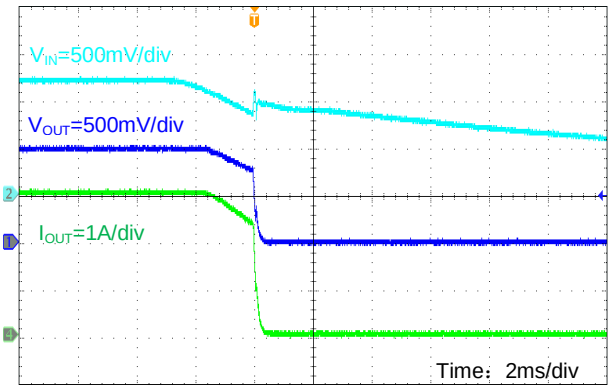

### Input Power On

$V_{IN}$=1.3V, $V_{OUT}$=1V, $V_{EN}$= $V_{IN}$, $I_{OUT}$=3A



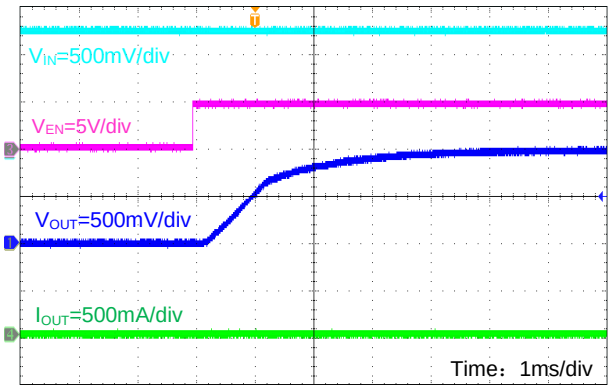

### Input Power Down

$V_{IN}$=1.3V, $V_{OUT}$=1V, $V_{EN}$= $V_{IN}$, $I_{OUT}$=3A



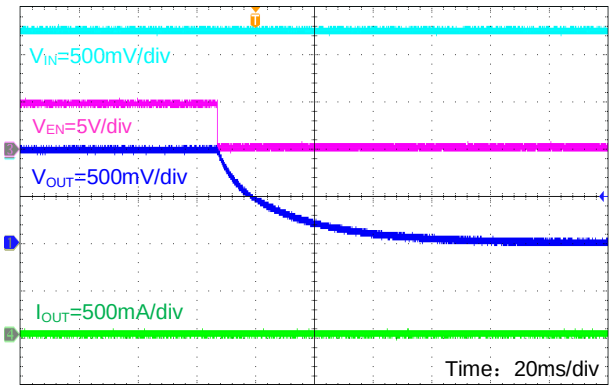

### EN Power On

$V_{IN}$=1.3V, $V_{OUT}$=1V, $V_{EN}$=5V, $I_{OUT}$=0A




### EN Power Down

$V_{IN}$=1.3V, $V_{OUT}$=1V, $V_{EN}$=5V, $I_{OUT}$=0A

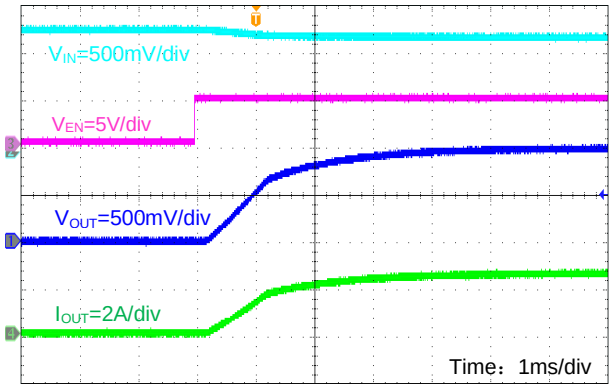


## Typical Performance Characteristics (continued)

**$C_{IN}$ = 47μF +10μF, $C_{OUT}$ = 47μF+10μF+10μF, $C_{NR/SS}$= 10nF, $C_{fb}$= 10nF**

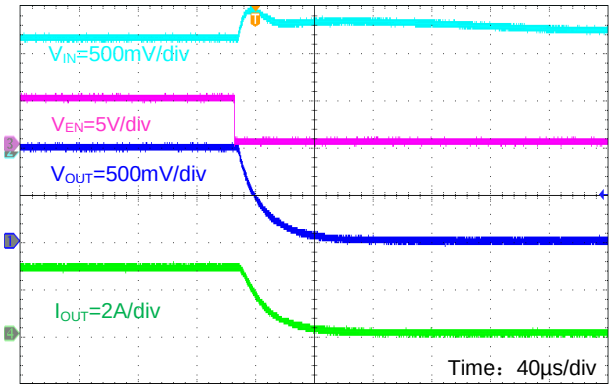
### EN Power On

$V_{IN}$=1.3V, $V_{OUT}$=1V, $V_{EN}$=5V, $I_{OUT}$=3A



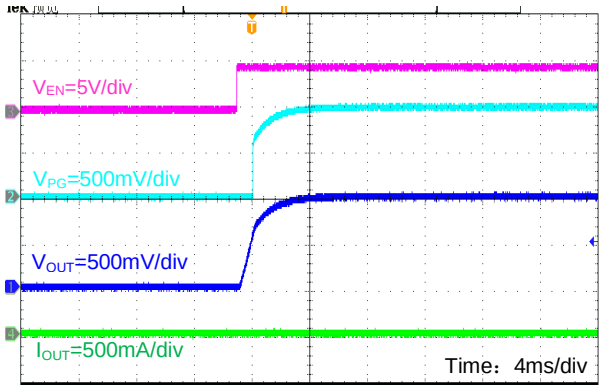

### EN Power Down

$V_{IN}$=1.3V, $V_{OUT}$=1V, $V_{EN}$=5V, $I_{OUT}$=3A



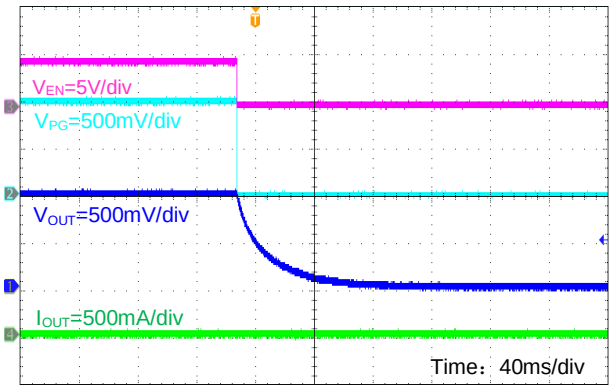

### PGOOD when EN Enable

$V_{IN}$=1.3V, $V_{OUT}$=1V, $V_{EN}$=5V, $I_{OUT}$=0mA



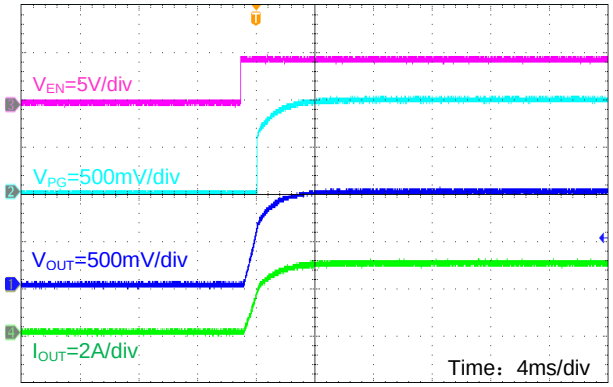

### PGOOD when EN Enable

$V_{IN}$=1.3V, $V_{OUT}$=1V, $V_{EN}$=5V, $I_{OUT}$=0mA



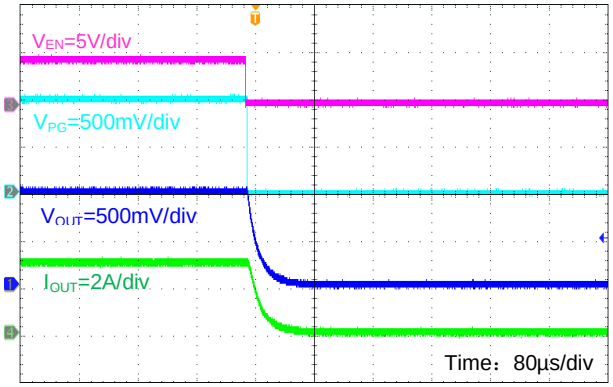

### PGOOD when EN Enable

$V_{IN}$=1.3V, $V_{OUT}$=1V, $V_{EN}$=5V, $I_{OUT}$=3A




### PGOOD when EN Enable

$V_{IN}$=1.3V, $V_{OUT}$=1V, $V_{EN}$=5V, $I_{OUT}$=3A

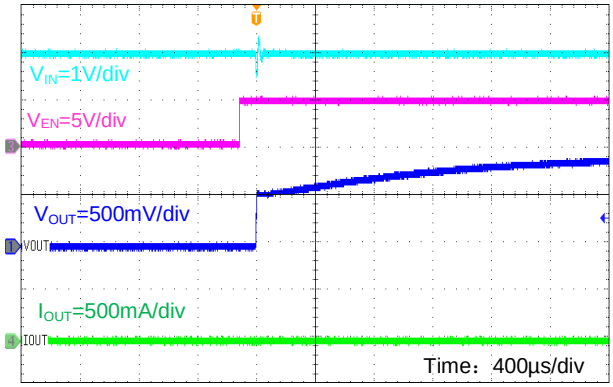


## Typical Performance Characteristics (continued)

**$C_{IN}$ = 47μF +10μF, $C_{OUT}$ = 47μF+10μF+10μF, $C_{fb}$= 10nF**

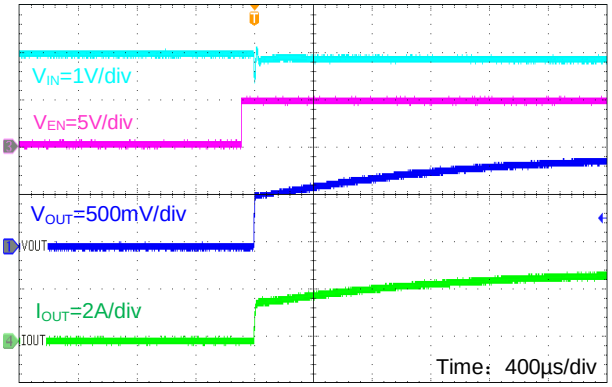
### Start-Up Time and $C_{NR/SS}$

$V_{IN}$=2V, $V_{OUT}$=1V, Io=0A, $C_{NR/SS}$=NC



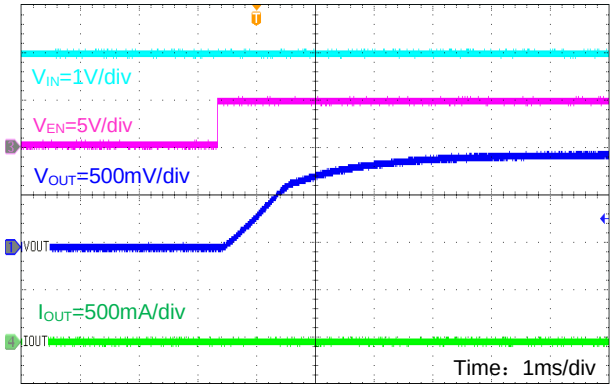

### Start-Up Time and $C_{NR/SS}$

$V_{IN}$=2V, $V_{OUT}$=1V, Io=3A, $C_{NR/SS}$=NC



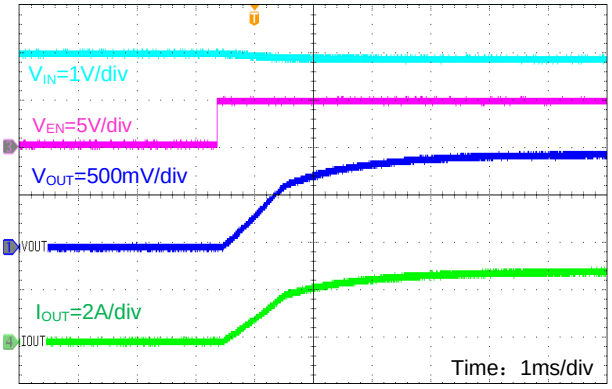

### Start-Up Time and $C_{NR/SS}$

$V_{IN}$=2V, $V_{OUT}$=1V, Io=0A, $C_{NR/SS}$=10nF



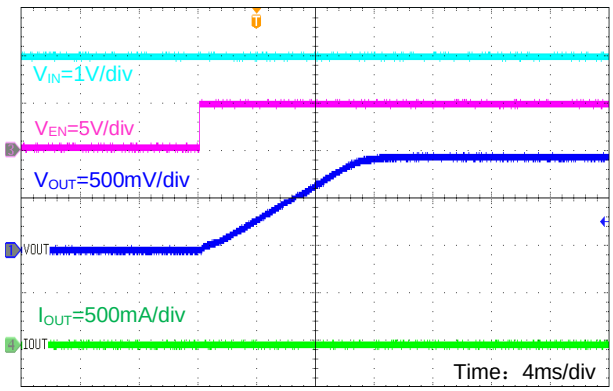

### Start-Up Time and $C_{NR/SS}$

$V_{IN}$=2V, $V_{OUT}$=1V, Io=3A, $C_{NR/SS}$=10nF



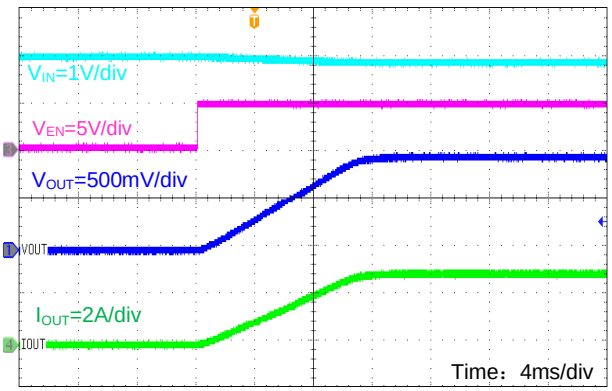

### Start-Up Time and $C_{NR/SS}$

$V_{IN}$=2V, $V_{OUT}$=1V, Io=0A, $C_{NR/SS}$=100nF



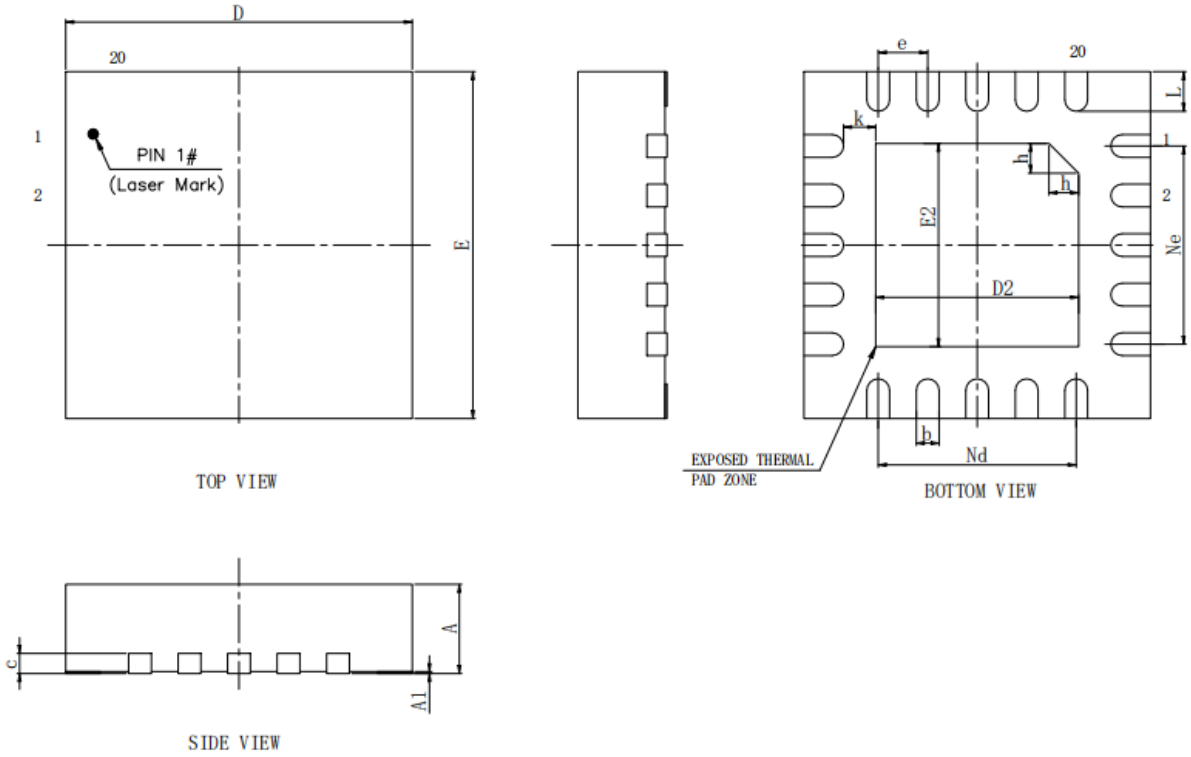

### Start-Up Time and $C_{NR/SS}$

$V_{IN}$=2V, $V_{OUT}$=1V, Io=3A, $C_{NR/SS}$=100nF



# Package Information

## QFN3.5x3.5-20




Unit: mm

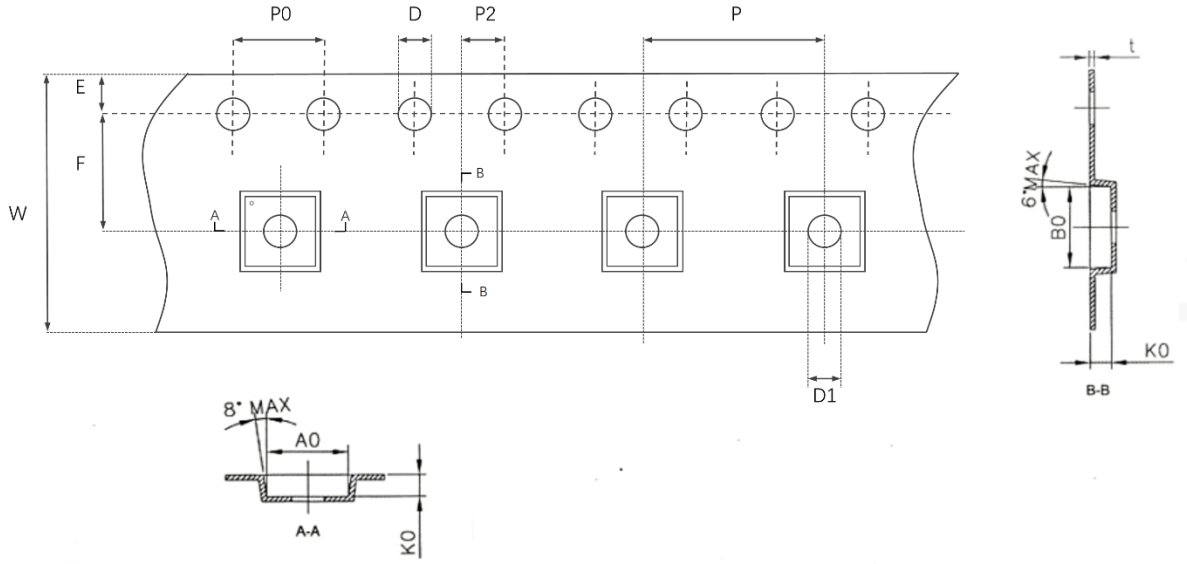
| Symbol | Dimensions In Millimeters | | | Symbol | Dimensions In Millimeters | | |
|---|---|---|---|---|---|---|---|
| | Min | Nom | Max | | Min | Nom | Max |
| A | 0.70 | 0.75 | 0.80 | Nd | 2.00 BSC | | |
| A1 | 0 | 0.02 | 0.05 | E | 3.40 | 3.50 | 3.60 |
| b | 0.18 | 0.23 | 0.30 | E2 | 1.95 | 2.05 | 2.15 |
| c | 0.203 REF | | | L | 0.35 | 0.40 | 0.45 |
| D | 3.40 | 3.50 | 3.60 | h | 0.25 | 0.30 | 0.35 |
| D2 | 1.95 | 2.05 | 2.15 | K | 0.275 | 0.325 | 0.375 |
| e | 0.50 BSC | | | Nd | 2.00 BSC | | |

**Note:**

1) All dimensions are in millimeters.
2) Package length does not include mold flash, protrusion or gate burr.
3) Package width does not include inter lead flash or protrusion.
4) Lead popularity (bottom of leads after forming) shall be 0.10 millimeters max.

# TAPE AND REEL INFORMATION

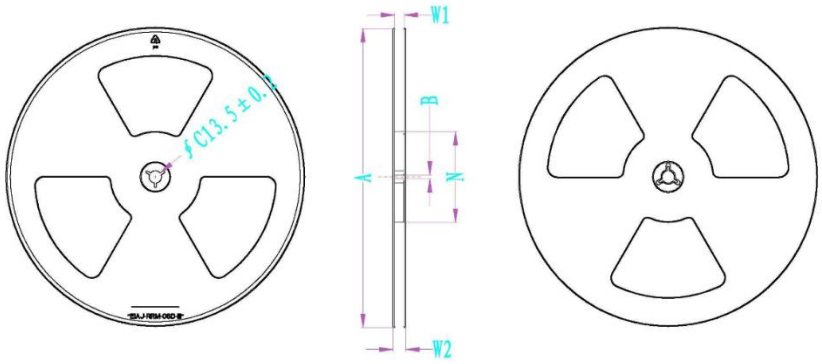
**TAPE DIMENSIONS:**




Unit: mm

| Symbol | Dimensions In Millimeters (mm) | Symbol | Dimensions In Millimeters (mm) | Symbol | Dimensions In Millimeters (mm) |
|---|---|---|---|---|---|
| E | 1.75±0.10 | P0 | 4.00±0.10 | B0 | 3.75±0.10 |
| F | 5.50 ± 0.05 | 10P0 | 40.0±0.20 | K0 | 1.00±0.05 |
| P2 | 2.00±0.05 | W | $12^{+0.30}_{-0.10}$ | t | 0.23±0.02 |
| D | $1.50^{+0.10}_{0}$ | P | 8.00±0.10 | | |
| D1 | $1.5^{+0.25}_{0}$ | A0 | 3.75±0.10 | | |

**REEL DIMENSIONS:**




Unit: mm

| Ø A | B | Ø C | Ø N | W1 | W2 |
|---|---|---|---|---|---|
| 330±1.0 | 4.7±0.5 | 13.5±0.2 | 100±0.5 | 12.8±0.5 | 17.4±0.5 |

**Note:**

1) All Dimensions are in Millimeter
2) Quantity of Units per Reel is 3000
3) MSL level is level 2.

## Important Notification

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