

FEATURE

- ◆ -30V/-4.3A, $R_{DS(ON)}=44m\Omega$ (typ.)@ $V_{GS}=-10V$
- ◆ -30V/-3.5A, $R_{DS(ON)}=50m\Omega$ (typ.)@ $V_{GS}=-4.5V$
- ◆ -30V/-2.5A, $R_{DS(ON)}=65m\Omega$ (typ.)@ $V_{GS}=-2.5V$
- ◆ Super high design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and Maximum DC current capability
- ◆ Full RoHS compliance
- ◆ SOT23-3 package design

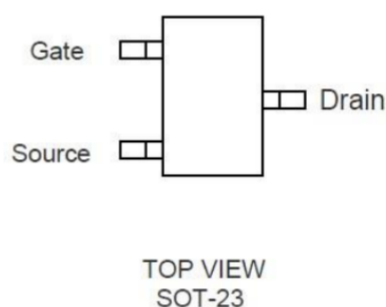
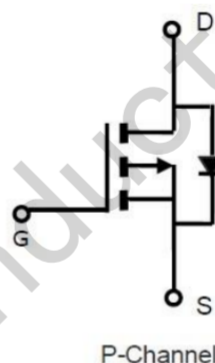
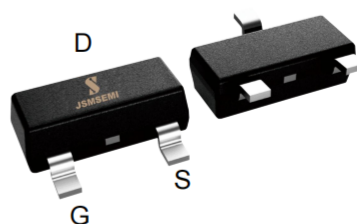
DESCRIPTION

The SSM3J02T is the P-Channel logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology..

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, and low in-line power loss are needed in a very small outline surface mount package.

APPLICATIONS

- ◆ Power Management
- ◆ Portable Equipment
- ◆ DC/DC Converter
- ◆ Load Switch
- ◆ DSC
- ◆ LCD Display inverter



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V _{DSS}	Drain-Source Voltage		-30	V
V _{GSS}	Gate-Source Voltage		±12	V
I _D	Continuous Drain Current (T _C =25℃)	V _{GS} =-10V	-4.3	A
	Continuous Drain Current (T _J =70℃)		-4.0	
I _{DM}	Pulsed Drain Current		-20	A
I _S	Continuous Source Current (Diode Conduction)		-1.5	A
P _D	Power Dissipation	T _A =25℃	1.5	W
		T _A =70℃	0.9	
T _J	Operation Junction Temperature		150	℃
T _{STG}	Storage Temperature Range		-55~+150	℃
R _{θJA}	Thermal Resistance Junction to Ambient		120	℃/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress rating only and functional device operation is not implied

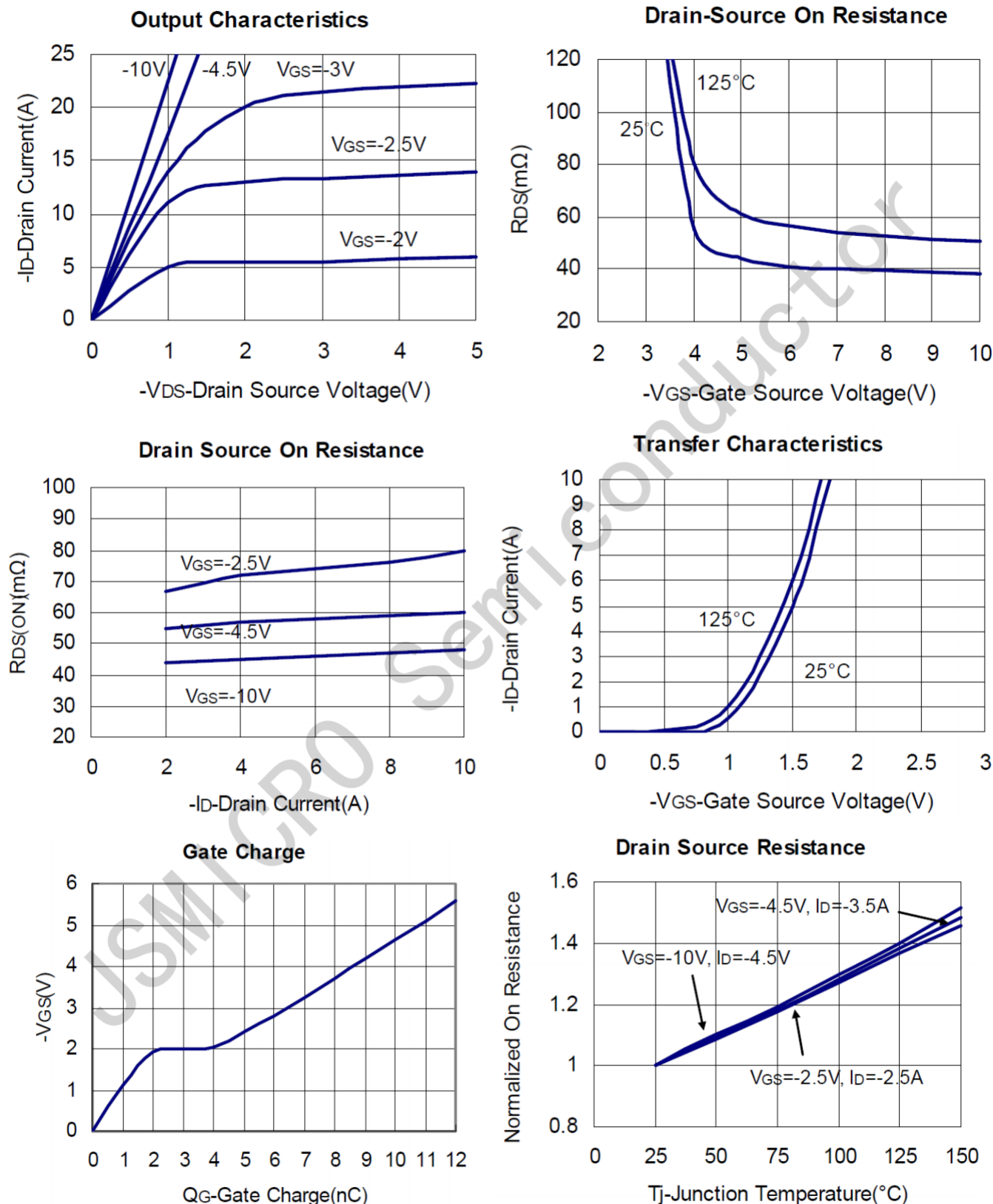
■ **ELECTRICAL CHARACTERISTICS** ($T_A=25^\circ\text{C}$ Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.6		-1.2	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 12V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-24V, V_{GS}=0$			-1	μA
		$V_{DS}=-24V, V_{GS}=0$ $T_J=55^{\circ}C$			-5	
$R_{DS(ON)}$	Drain-Source On-Resistance	$V_{GS}=-10V, I_D=-4.3A$		44	52	m Ω
		$V_{GS}=-4.5V, I_D=-3.5A$		50	58	
		$V_{GS}=-2.5V, I_D=-2.5A$		65	78	
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	$I_S=-1.0A, V_{GS}=0V$		-0.7	-1.0	V
Dynamic Parameters						
Q_g	Total Gate Charge	$V_{DS}=-20V$ $V_{GS}=-4.5V$ $I_D=-4.0A$		6.2		nC
Q_{gs}	Gate-Source Charge			2.8		
Q_{gd}	Gate-Drain Charge			3.0		
C_{iss}	Input Capacitance	$V_{DS}=-12V$ $V_{GS}=0V$ $f=1MHz$		672		pF
C_{oss}	Output Capacitance			280		
C_{rss}	Reverse Transfer Capacitance			102		
$T_{d(on)}$	Turn-On Time	$V_{DS}=-12V$ $I_D=-4A$ $V_{GEN}=-10V$ $R_G=3.3\Omega$		9		nS
T_r				15		
$T_{d(off)}$	Turn-Off Time			23		
T_f				21		

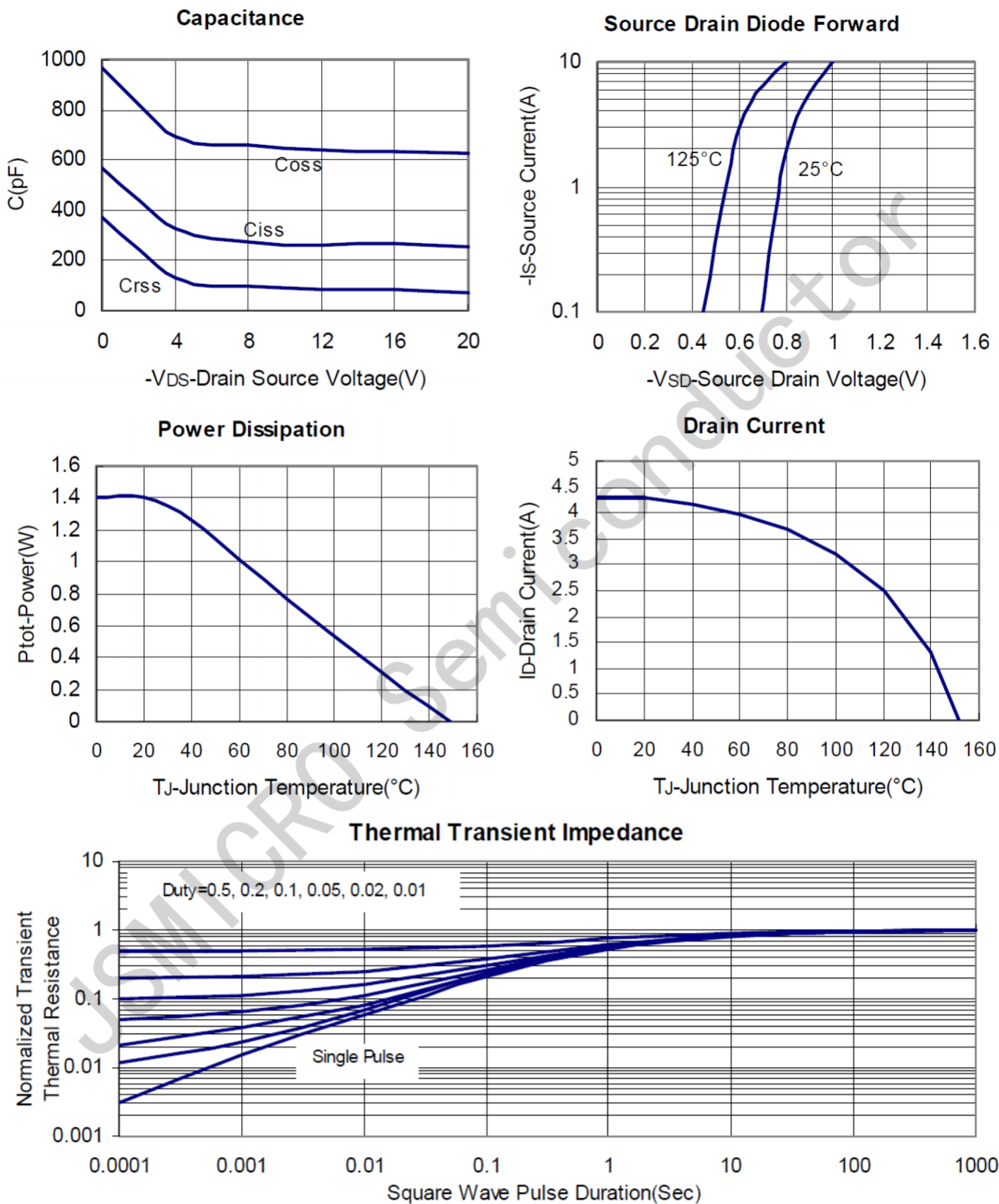
Note: 1. Pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

2. Static parameters are based on package level with recommended wire bonding

■ **TYPICAL CHARACTERISTICS** (25 °C Unless Note)

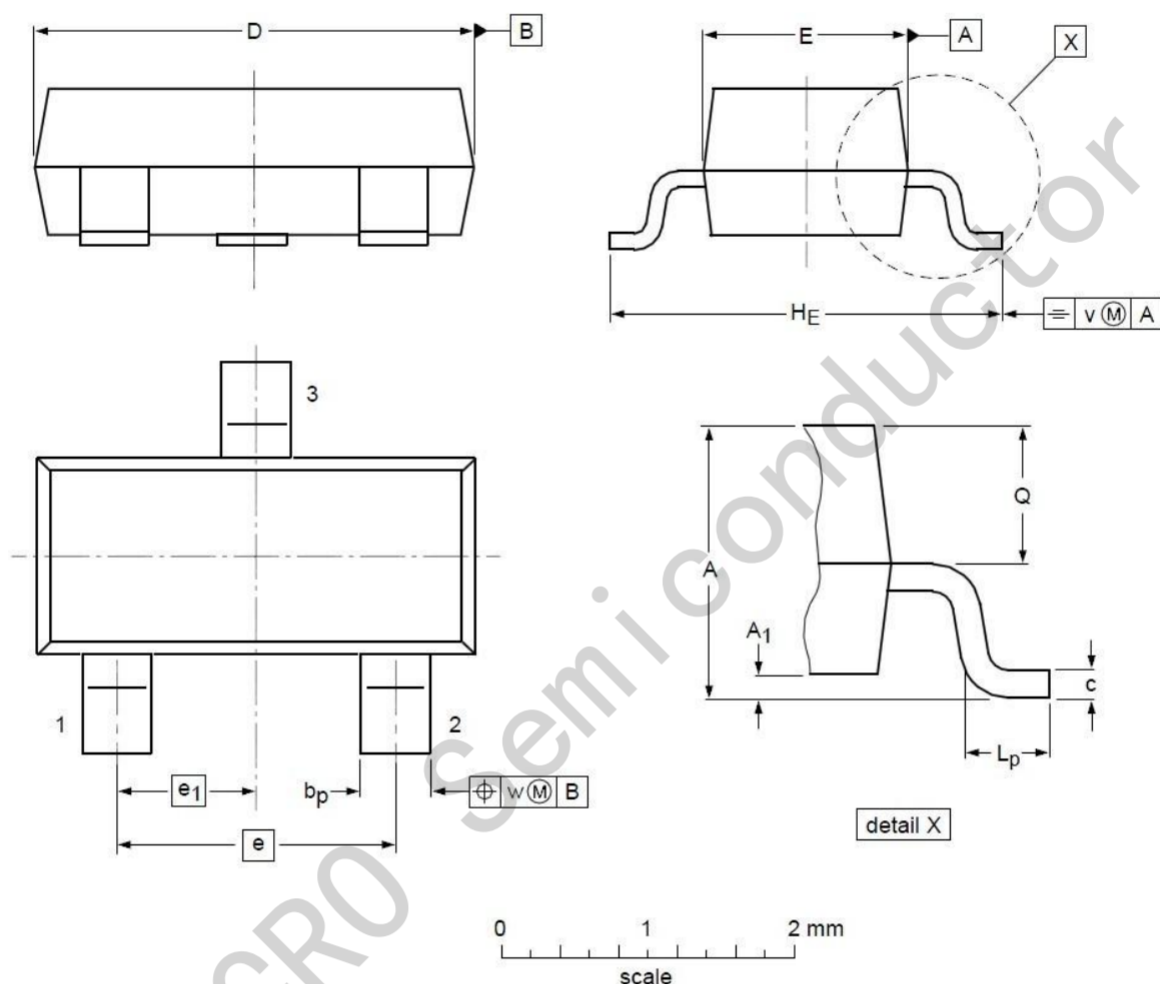


■ **TYPICAL CHARACTERISTICS** (continuous)



Package Information

SOT-23-3



DIMENSIONS (unit : mm)

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	0.90	1.01	1.15	A ₁	0.01	0.05	0.10
b _p	0.30	0.42	0.50	c	0.08	0.13	0.15
D	2.80	2.92	3.00	E	1.20	1.33	1.40
e	--	1.90	--	e ₁	--	0.95	--
H _E	2.25	2.40	2.55	L _p	0.30	0.42	0.50
Q	0.45	0.49	0.55	v	--	0.20	--
w	--	0.10	--				