

Description

The FDS8333C uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge.

The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

General Features

● N-Channel

$$V_{DS} = 40V, I_D = 8.0A$$

$$R_{DS(ON)} < 22m\Omega @ V_{GS}=10V$$

$$R_{DS(ON)} < 31m\Omega @ V_{GS}=4.5V$$

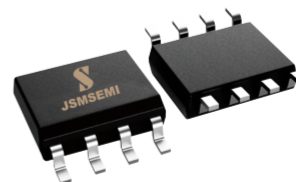
● P-Channel

$$V_{DS} = -40V, I_D = -7.0A$$

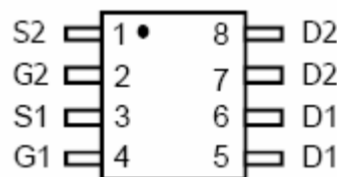
$$R_{DS(ON)} < 35m\Omega @ V_{GS}=-10V$$

$$R_{DS(ON)} < 48m\Omega @ V_{GS}=-4.5V$$

- High power and current handling capability
- Lead free product is acquired
- Surface mount package



Schematic diagram



Marking and pin assignment

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	40	-40	V
Gate-Source Voltage		V_{GS}	± 20	± 20	V
Continuous Drain Current	$T_A=25^\circ\text{C}$	I_D	8.0	-7.0	A
Pulsed Drain Current ^(Note 1)		I_{DM}	40	-30	A
Maximum Power Dissipation	$T_A=25^\circ\text{C}$	P_D	2.0	2.0	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 To 150	-55 To 150	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note2)	$R_{\theta JA}$	N-Ch	62.5	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient ^(Note2)	$R_{\theta JA}$	P-Ch	62.5	$^\circ\text{C/W}$

N-CH Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA

On Characteristics (Note 3)

Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.4	2.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=8A$	-	17	22	m Ω
		$V_{GS}=4.5V, I_D=6A$	-	21	31	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=8A$	15	-	-	S

Dynamic Characteristics (Note 4)

Input Capacitance	C_{iss}	$V_{DS}=20V, V_{GS}=0V,$ $F=1.0MHz$	-	415	-	PF
Output Capacitance	C_{oss}		-	112	-	PF
Reverse Transfer Capacitance	C_{rss}		-	11	-	PF

Switching Characteristics (Note 4)

Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=20V, R_L=2.5\Omega$ $V_{GS}=10V, R_{GEN}=3\Omega$	-	4.0	-	nS
Turn-on Rise Time	t_r		-	3.0	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	15	-	nS
Turn-Off Fall Time	t_f		-	2.0	-	nS
Total Gate Charge	Q_g	$V_{DS}=20V, I_D=8A,$ $V_{GS}=10V$	-	12	-	nC
Gate-Source Charge	Q_{gs}		-	3.5	-	nC
Gate-Drain Charge	Q_{gd}		-	3.1	-	nC

Drain-Source Diode Characteristics

Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=8A$	-	0.75	1.0	V
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Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

N- Channel Typical Electrical and Thermal Characteristics (Curves)

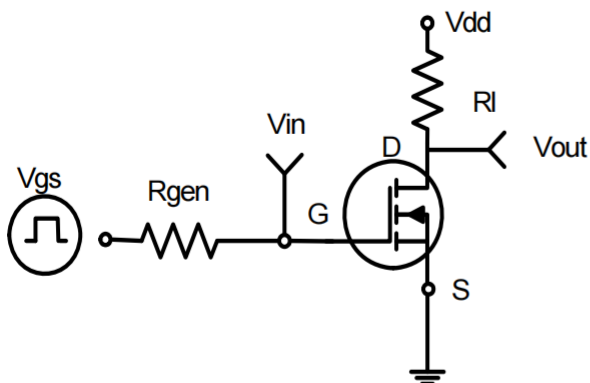


Figure 1: Switching Test Circuit

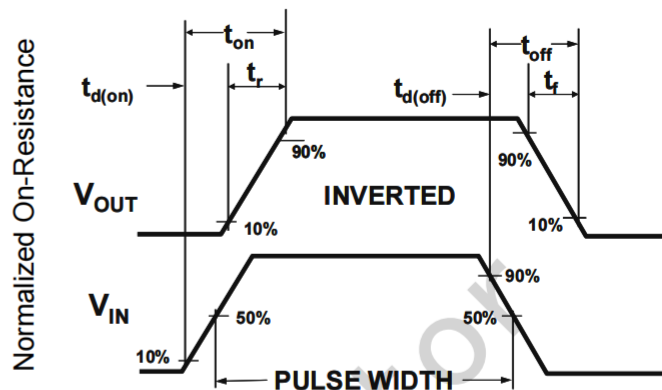


Figure 2: Switching Waveforms



Figure 3 Output Characteristics



Figure 4 Transfer Characteristics



Figure 5 Drain-Source On-Resistance



Figure 6 Drain-Source On-Resistance



V_{GS} Gate-Source Voltage (V)
Figure 7 Rdson vs Vgs



T_J-Junction Temperature(°C)
Figure 8 Power Dissipation



Q_g Gate Charge (nC)
Figure 9 Gate Charge



V_{DS} Drain-Source Voltage (V)
Figure 10 Source- Drain Diode Forward



V_{DS} Drain-Source Voltage (V)
Figure 11 Capacitance vs Vds



V_{DS} Drain-Source Voltage (V)
Figure 12 Safe Operation Area



Figure 13 Normalized Maximum Transient Thermal Impedance

P-CH Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-40V, V_{GS}=0V$	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA

On Characteristics (Note 3)

Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.1	-1.8	-2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-7.0A$	-	30	35	m Ω
		$V_{GS}=-4.5V, I_D=-4.0A$	-	43	48	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-5V, I_D=-7.0A$	15	-	-	S

Dynamic Characteristics (Note4)

Input Capacitance	C_{iss}	$V_{DS}=-20V, V_{GS}=0V,$ $F=1.0MHz$	-	520	-	PF
Output Capacitance	C_{oss}		-	100	-	PF
Reverse Transfer Capacitance	C_{rss}		-	65	-	PF

Switching Characteristics (Note 4)

Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-20V, R_L=2.3\Omega$ $V_{GS}=-10V, R_{GEN}=6\Omega$	-	7.5	-	nS
Turn-on Rise Time	t_r		-	5.5	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	19	-	nS
Turn-Off Fall Time	t_f		-	7	-	nS
Total Gate Charge	Q_g	$V_{DS}=-20V, I_D=-7.0A$ $V_{GS}=-10V$	-	13	-	nC
Gate-Source Charge	Q_{gs}		-	3.8	-	nC
Gate-Drain Charge	Q_{gd}		-	3.1	-	nC

Drain-Source Diode Characteristics

Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=-7.0A$	-	0.75	-1.0	V
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Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

P- Channel Typical Electrical and Thermal Characteristics (Curves)



Figure 1 Output Characteristics

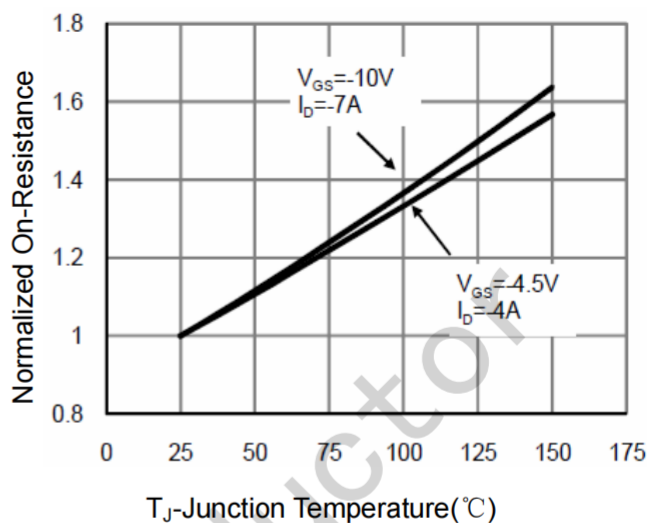


Figure 4 Rdson-Junction Temperature

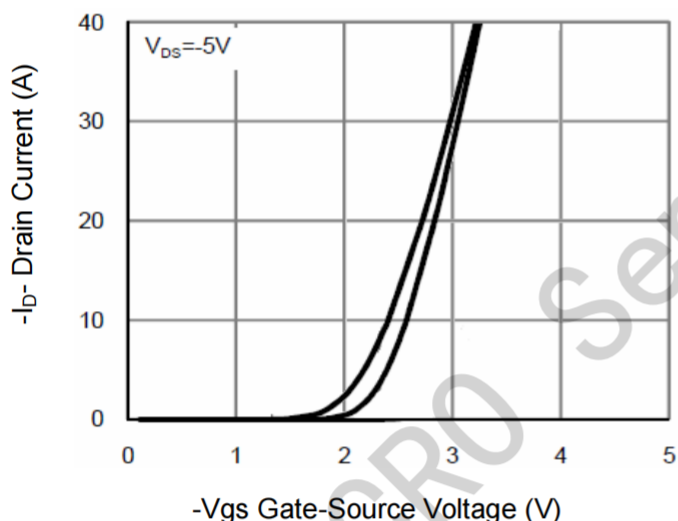


Figure 2 Transfer Characteristics

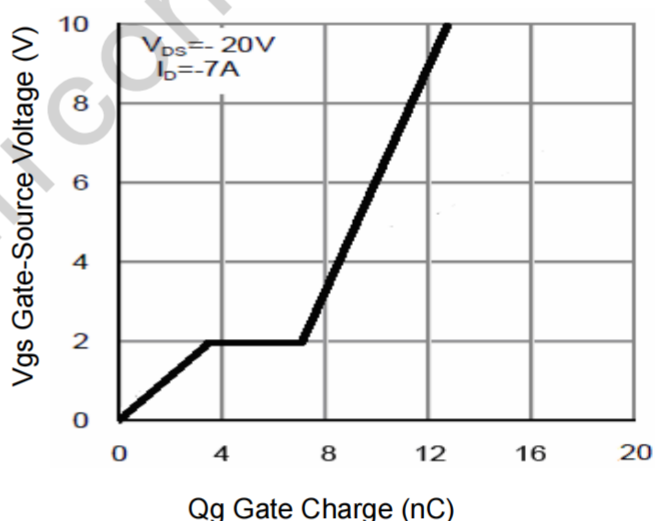


Figure 5 Gate Charge

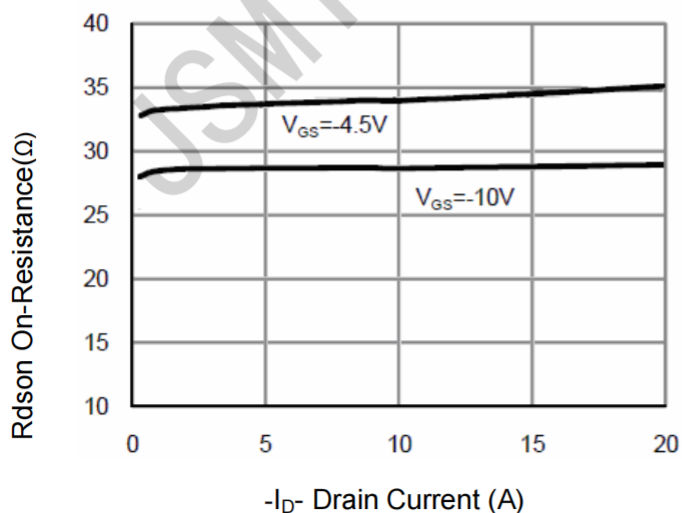


Figure 3 Rdson- Drain Current

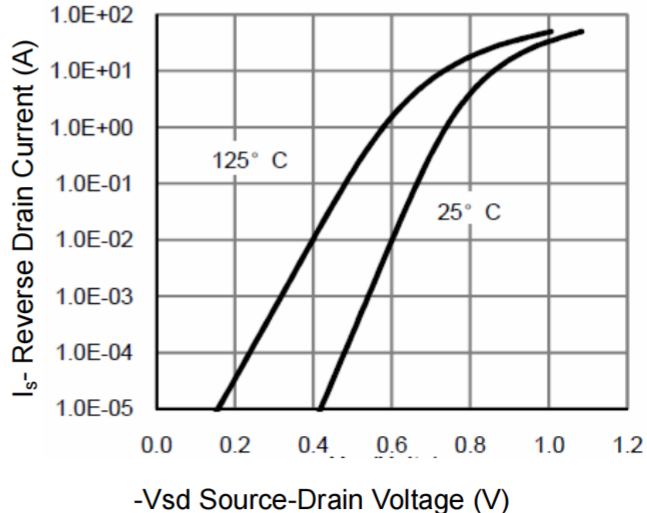


Figure 6 Source- Drain Diode Forward



-Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



Tj Junction Temperature(°C)
Figure 9 Power Dissipation



-Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



Tj Junction Temperature(°C)
Figure 10 VGS(th) vs Junction Temperature



Figure 11 Normalized Maximum Transient Thermal Impedance



Package Information

SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

RECOMMENDED LAND PATTERN

