



Description

The APM4532KC uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge.

The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

General Features

● N-Channel

$$V_{DS} = 30V, I_D = 6.9A$$

$$R_{DS(ON)} < 21m\Omega @ V_{GS}=10V$$

$$R_{DS(ON)} < 32m\Omega @ V_{GS}=4.5V$$

● P-Channel

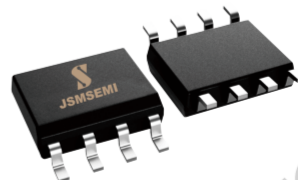
$$V_{DS} = -30V, I_D = -6.0A$$

$$R_{DS(ON)} < 45m\Omega @ V_{GS}=-10V$$

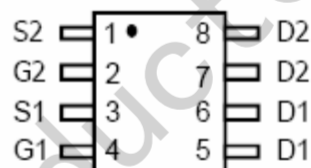
$$R_{DS(ON)} < 60m\Omega @ V_{GS}=-4.5V$$

- High power and current handling capability
- Lead free product is acquired
- Surface mount package

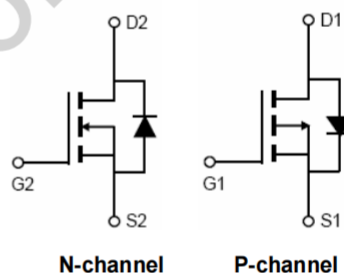
■ PIN CONFIGURATION



Schematic diagram



Marking and pin assignment



Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	± 20	± 20	V
Continuous Drain Current	$T_A=25^{\circ}C$	I_D	6.9	-6.0	A
Pulsed Drain Current	(Note 1)	I_{DM}	28	-26	A
Maximum Power Dissipation	$T_A=25^{\circ}C$	P_D	2.0	2.0	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 To 150	-55 To 150	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient	(Note 2)	$R_{\theta JA}$	N-Ch	63.5	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient	(Note 2)	$R_{\theta JA}$	P-Ch	63.5	$^{\circ}C/W$


N-CH Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=24V, V_{GS}=0V$	-	-	50	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA

On Characteristics (Note 3)

Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.6	2.4	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=6.9A$	-	19	21	m Ω
		$V_{GS}=4.5V, I_D=5A$	-	29	32	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=5.0A$	5	-	-	S

Dynamic Characteristics (Note4)

Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V,$ $F=1.0MHz$	-	398	-	PF
Output Capacitance	C_{oss}		-	67	-	PF
Reverse Transfer Capacitance	C_{rss}		-	61	-	PF

Switching Characteristics (Note 4)

Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=15V, R_L=15\Omega$ $V_{GS}=10V, R_{GEN}=6\Omega$ $I_D=1.0A$	-	8.0	-	nS
Turn-on Rise Time	t_r		-	11.5	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	17	-	nS
Turn-Off Fall Time	t_f		-	7.5	-	nS
Total Gate Charge	Q_g	$V_{DS}=10V, I_D=1.0A,$ $V_{GS}=10V$	-	7.5	-	nC
Gate-Source Charge	Q_{gs}		-	1.7	-	nC
Gate-Drain Charge	Q_{gd}		-	1.3	-	nC

Drain-Source Diode Characteristics

Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=2A$	-	0.75	1.0	V
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Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production



Characteristics Curve(N-Channel)

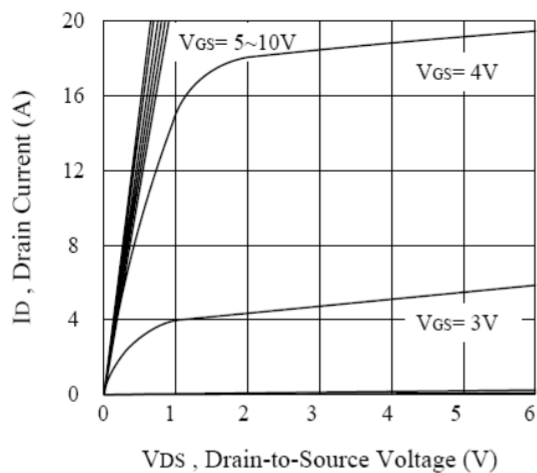


Figure 1. Output Characteristics

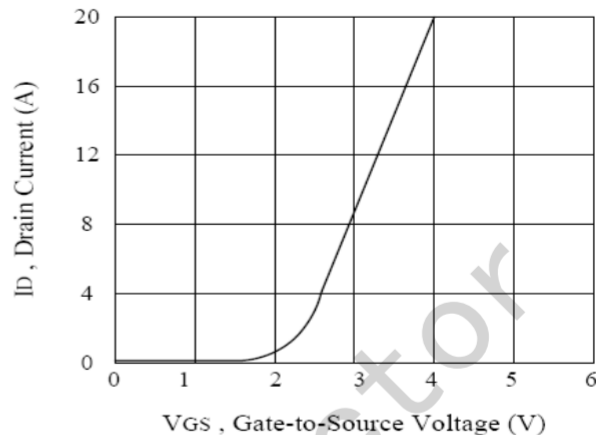


Figure 2. Transfer Characteristics

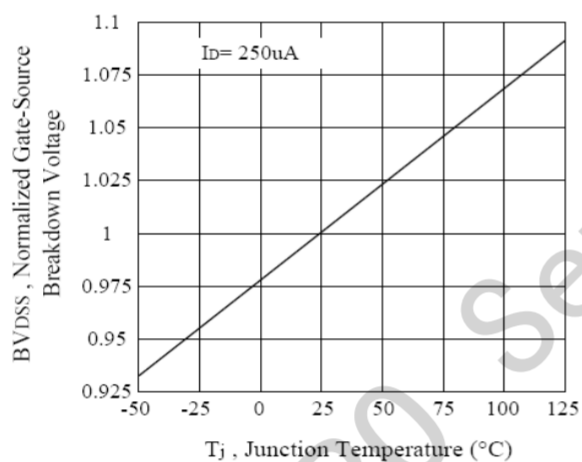


Figure 3. Breakdown Voltage Variation with Temperature

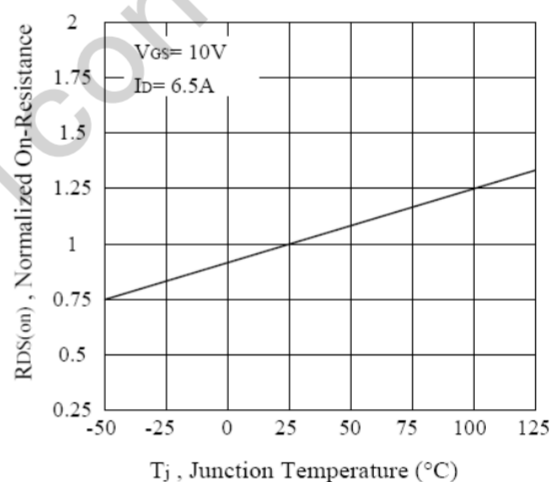


Figure 4. On-Resistance Variation with Temperature

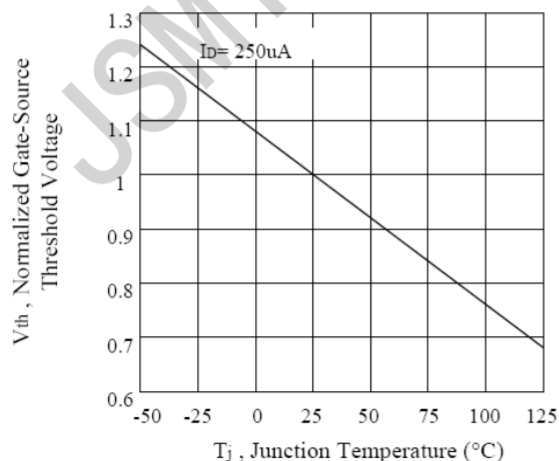
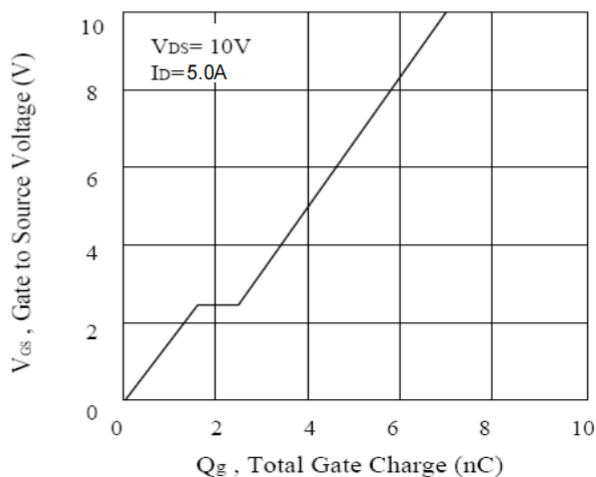
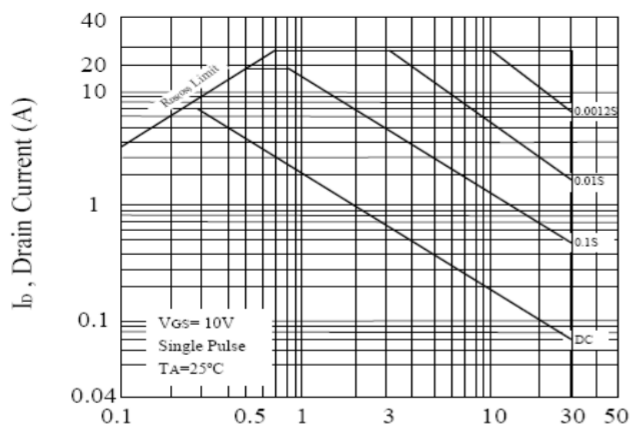


Figure 5. Gate Threshold Variation with Temperature

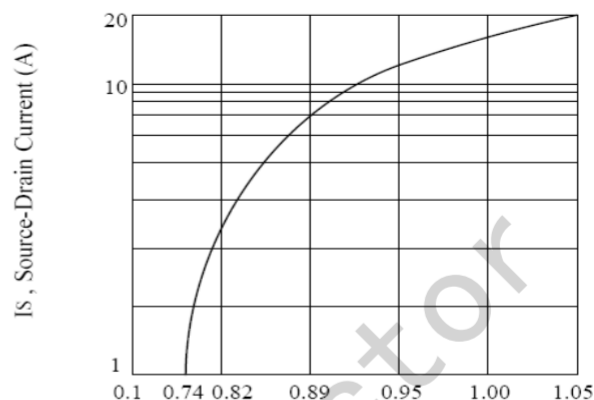




Characteristics Curve(N-Channel)



VDS, Drain-Source Voltage (V)
Figure 7. Maximum Safe Operating Area



VSD, Body Diode Forward Voltage (V)
Figure 8. Body Diode Forward Voltage Variation with Source Current

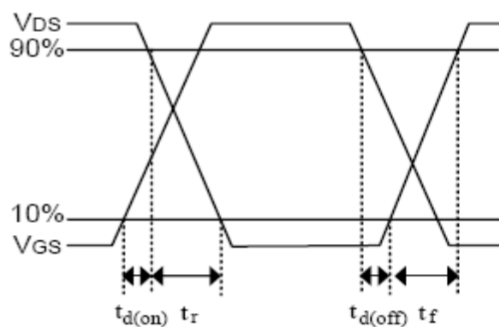
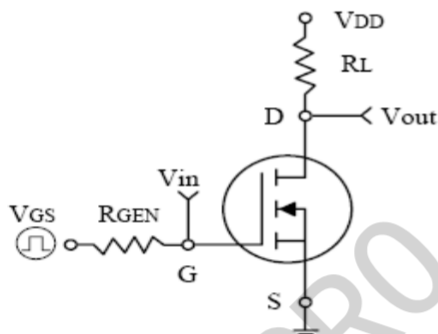


Figure 9. Switching Test Circuit and Switching Waveforms


P-CH Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-24V, V_{GS}=0V$	-	-	-50	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA

On Characteristics (Note 3)

Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0	-1.3	-2.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-6.0A$	-	42	45	m Ω
		$V_{GS}=-4.5V, I_D=-5.0A$	-	55	60	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-5V, I_D=-5.0A$	10	-	-	S

Dynamic Characteristics (Note 4)

Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V,$ $F=1.0MHz$	-	930	-	PF
Output Capacitance	C_{oss}		-	121	-	PF
Reverse Transfer Capacitance	C_{rss}		-	102	-	PF

Switching Characteristics (Note 4)

Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-15V, R_L=5.0\Omega$ $V_{GS}=-10V, R_{GEN}=6\Omega$ $I_D=-3.0A$	-	9.5	-	nS
Turn-on Rise Time	t_r		-	5.4	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	42.5	-	nS
Turn-Off Fall Time	t_f		-	13.6	-	nS
Total Gate Charge	Q_g	$V_{DS}=-15V, I_D=-3.0A$ $V_{GS}=-10V$	-	20	-	nC
Gate-Source Charge	Q_{gs}		-	4.1	-	nC
Gate-Drain Charge	Q_{gd}		-	2.6	-	nC

Drain-Source Diode Characteristics

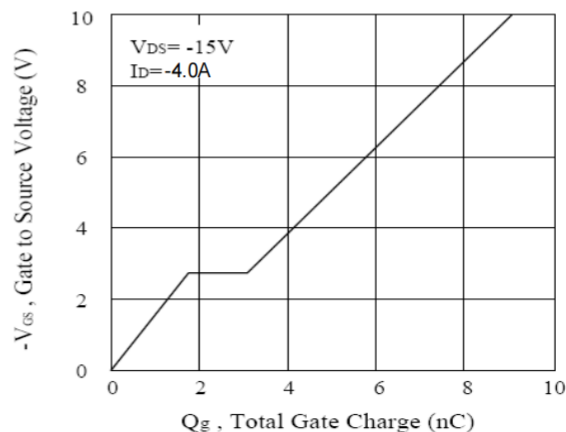
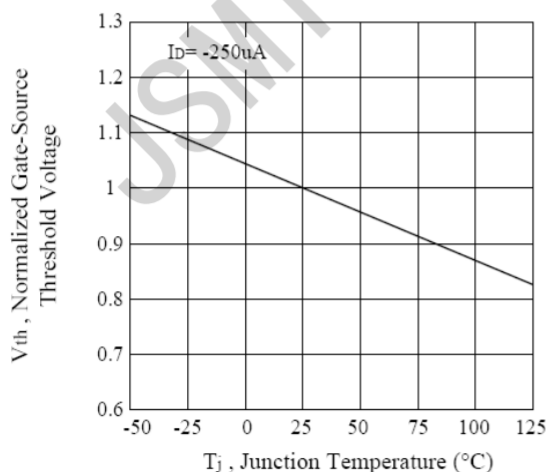
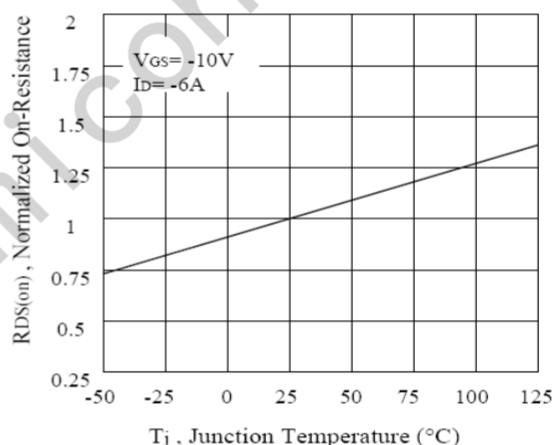
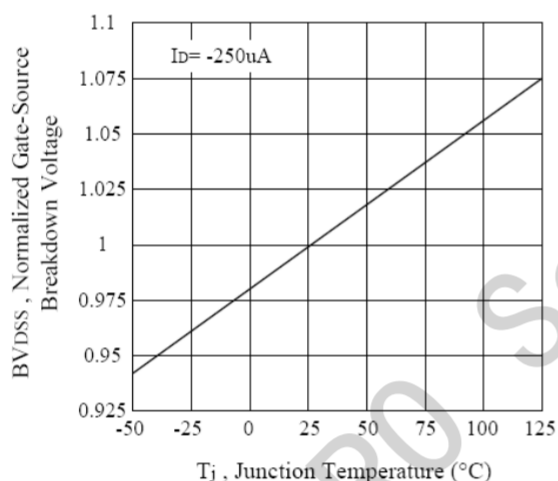
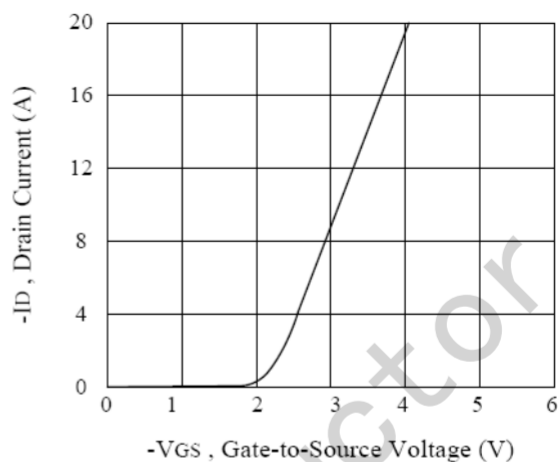
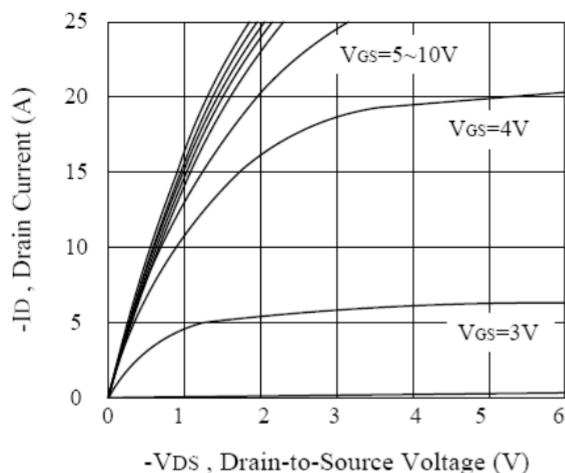
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=-2.0A$	-	0.75	-1.0	V
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Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production



Characteristics Curve(P-Channel)





Characteristics Curve(P-Channel)

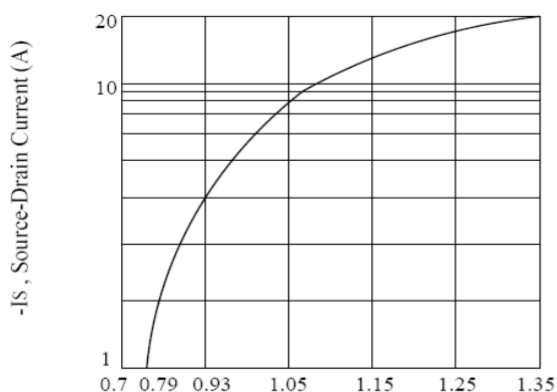


Figure 16 Body Diode Forward Voltage Variation with Source Current

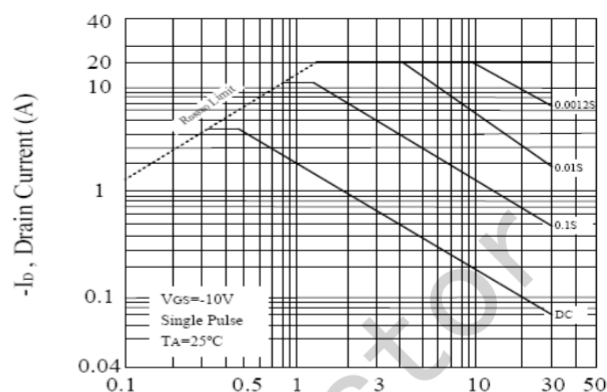


Figure 17. Maximum Safe Operating Area

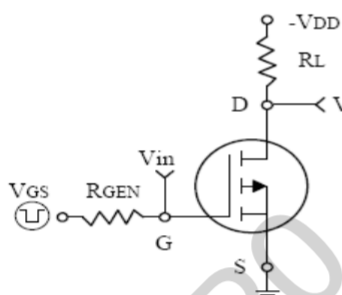
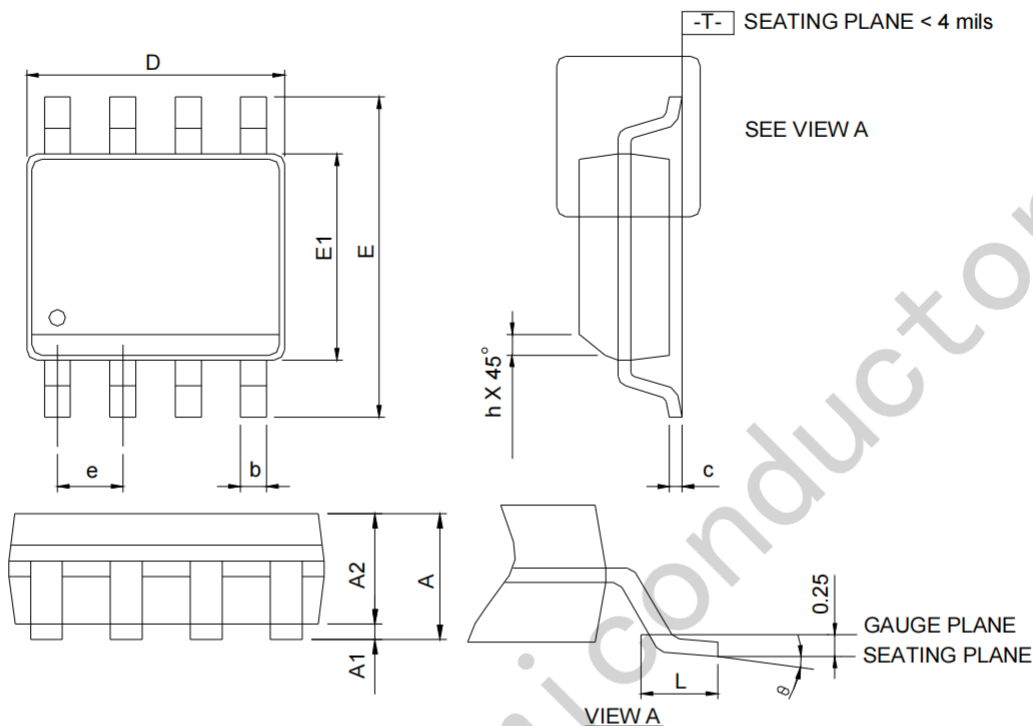


Figure 18 Switching Test Circuit and Switching Waveforms



Package Information

SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

RECOMMENDED LAND PATTERN

