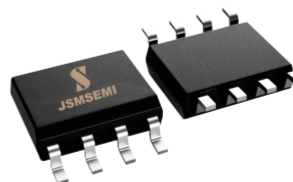


Description:

This N-Channel MOSFET uses advanced trench technology and

design to provide excellent $R_{DS(on)}$ with low gate charge.

It can be used in a wide variety of applications.



Features:

- 1) $V_{DS}=30V, I_D=12A, R_{DS(on)} < 8m\Omega @ V_{GS}=10V$
- 2) Low gate charge.
- 3) Green device available.
- 4) Advanced high cell density trench technology for ultra low $R_{DS(on)}$.
- 5) Excellent package for good heat dissipation.



Absolute Maximum Ratings: ($T_a=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current- $T_A=25^\circ\text{C}$	12	A
	Continuous Drain Current- $T_A=100^\circ\text{C}$	9	
I_{DM}	Drain Current-Pulsed ^{note1}	60	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}	39	mJ
P_D	Power Dissipation	3	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics:

Symbol	Parameter	Max	Units
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	41	$^\circ\text{C}/\text{W}$

Electrical Characteristics: ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μ A	30	---	---	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{GS} =0V, V _{DS} =30V	---	---	1	μ A
I _{GSS}	Gate-Source Leakage Current	V _{GS} =± 20V, V _{DS} =0A	---	---	±100	nA
On Characteristics						
V _{GS(th)}	GATE-Source Threshold Voltage	V _{GS} =V _{DS} , I _D =250 μ A	1	1.5	2.5	V
R _{DS(ON)}	Drain-Source On Resistance ^{note3}	V _{GS} =10V, I _D =15A	---	6.5	8	m Ω
		V _{GS} =4.5V, I _D =10A	---	10	14	
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	1110	---	pF
C _{oss}	Output Capacitance		---	180	---	
C _{rss}	Reverse Transfer Capacitance		---	150	---	
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DS} =15V, I _D =12A R _{GEN} =3 Ω . V _{GS} =10V,	---	15	---	ns
t _r	Rise Time		---	19	---	ns
t _{d(off)}	Turn-Off Delay Time		---	35	---	ns
t _f	Fall Time		---	21	---	ns
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =8A	---	21	---	nC
Q _{gs}	Gate-Source Charge		---	2.35	---	nC
Q _{gd}	Gate-Drain “Miller” Charge		---	5.9	---	nC
Drain-Source Diode Characteristics						
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =12A	---	---	1.2	V
I _S	Continuous Drain to Source Diode Forward Current		---	---	12	A

I_{SM}	Pulsed Drain to Source Diode Forward Current		---	---	60	A
t_{rr}	Reverse Recovery Time	I _F =12A,dI/dt=100A/ μ s	---	14	---	ns
Q_{rr}	Reverse Recovery Charge		---	4.1	---	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: T_J=25℃, V_{GS}=15V, R_G=25Ω, L=0.5mH, I_{AS}=12.6A
3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

Typical Characteristics: (T_C=25℃ unless otherwise noted)



Figure 1: Output Characteristics



Figure 2: Typical Transfer Characteristics

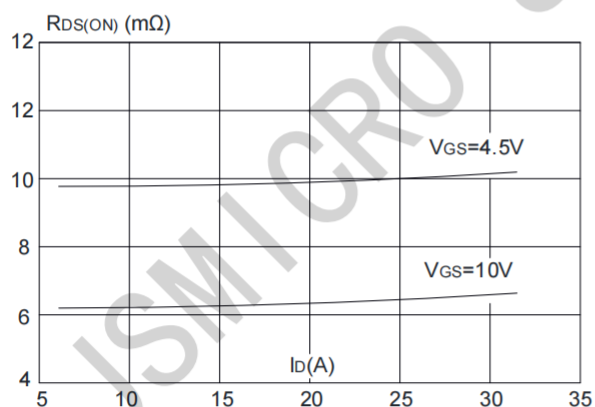


Figure 3: On-resistance vs. Drain Current



Figure 4: Body Diode Characteristics



Figure 5: Gate Charge Characteristics



Figure 6: Capacitance Characteristics



Figure 7: Normalized Breakdown Voltage vs. Junction Temperature



Figure 8: Normalized on Resistance vs. Junction Temperature



Figure 9: Maximum Safe Operating Area



Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

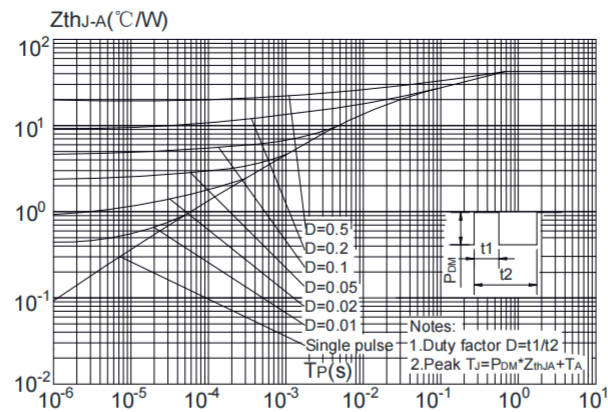


Figure.11: Maximum Effective
Transient Thermal Impedance, Junction-to-Ambient

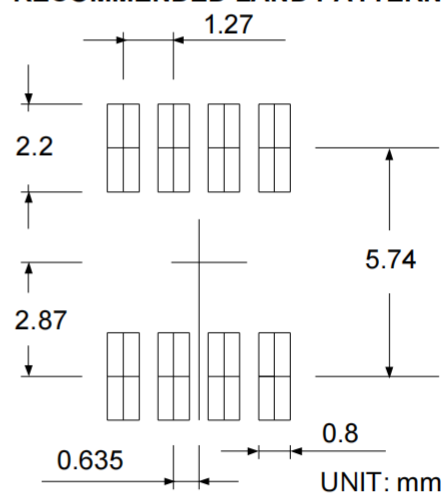
Package Information

SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

RECOMMENDED LAND PATTERN



Note: 1. Follow JEDEC MS-012 AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.